IBM / FE Supplement

System/Unit 1401 25000 Series

Re: Form No. 229-2038-1

This Supplement No. S29-0002-0

Date: 9/1/65

Previous Supplement Nos. None

These revised pages are to be distributed to all 25000 series 1401's. They are to update the original B/M Index (229-2038-1) which is found at the front of ALD book #1.

The following pages have been updated:

Cross reference -	1, 2, 3, 4, 5
IFC -	11, 12, 13, 14, 15, 16
IFCX -	6, 7, 8, 11, 12, 13, 14
CF -	3, 4, 5, 10, 11, 12, 13
TAU -	1, 2, 3, 4
Mech -	1, 2, 3

The Prerequisite Charts have also been updated and assigned a separate supplement number to facilitate ordering.

IBM Corporation, F.E. Technical Operations, Endicott, New York 13760

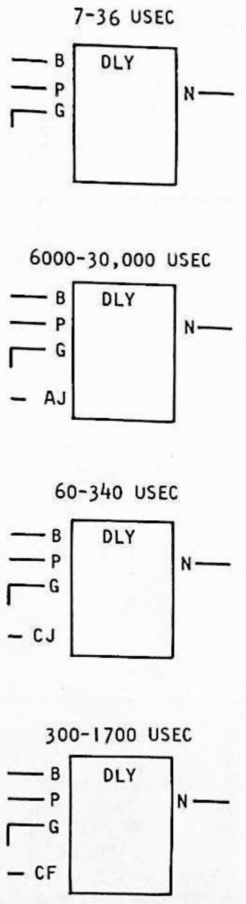
PRINTED IN U.S.A.

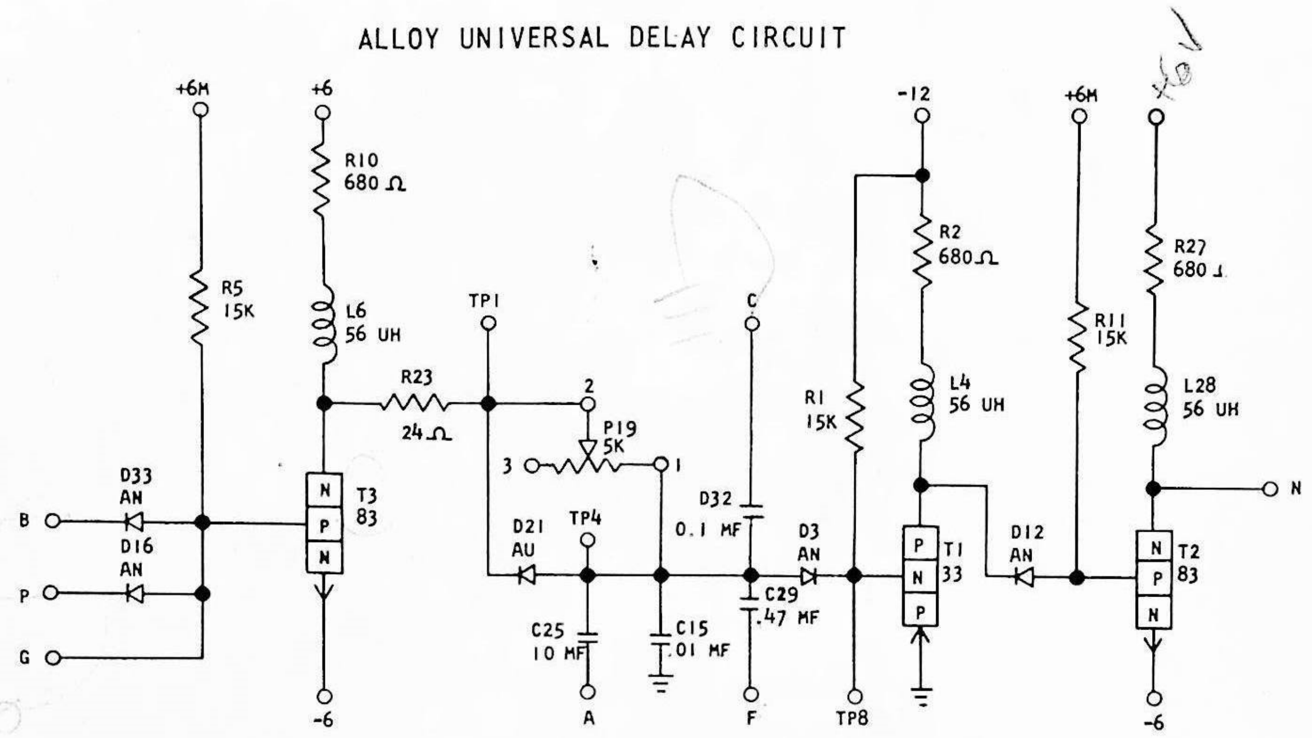
CARD CODE	729800
A A F -	

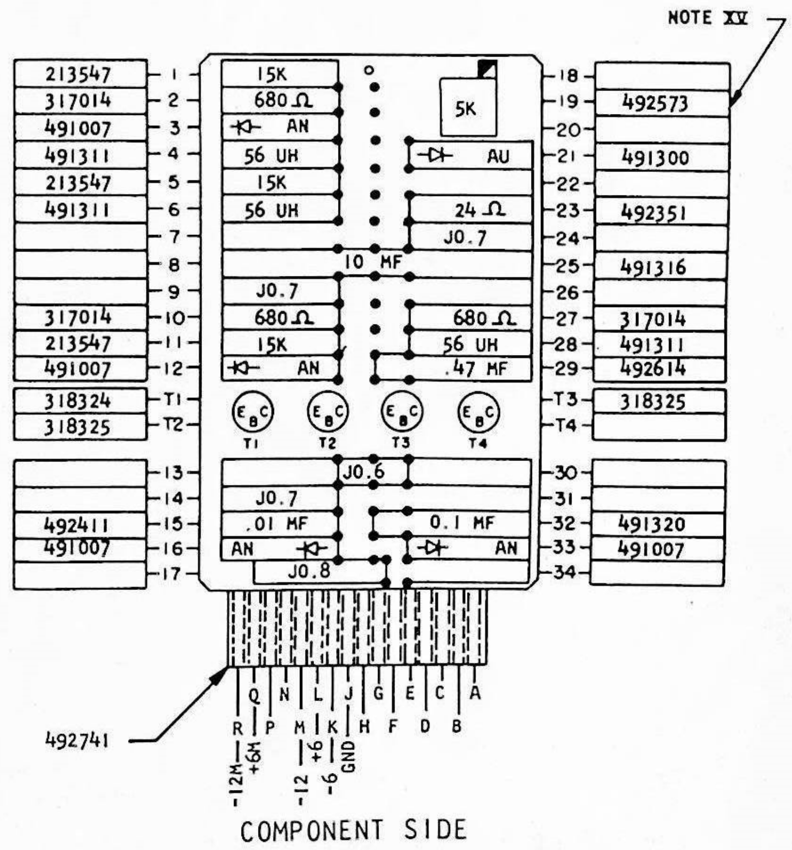
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371884

ALLOY UNIVERSAL DELAY CIRCUIT







SEQUENCE OF OPERATION

1. ALL INPUTS UP ALL TRANSISTORS ARE ON OUTPUT IS DOWN
2. ANY DOWN INPUT WILL CAUSE T3 TO GO OFF; T1 AND T2 WILL REMAIN ON UNTIL RC CAPACITOR IS CHARGED. WHEN THE CAPACITOR IS CHARGED T1 AND T2 WILL BE OFF AND THE OUTPUT WILL BE UP

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
P	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
N	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
B		EXTENDER INPUT		UP		-6
				DOWN		-12

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY UNIVERSAL DELAY CIRCUIT			-62	115599					729800
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

C

STANDARDS CODE

729801

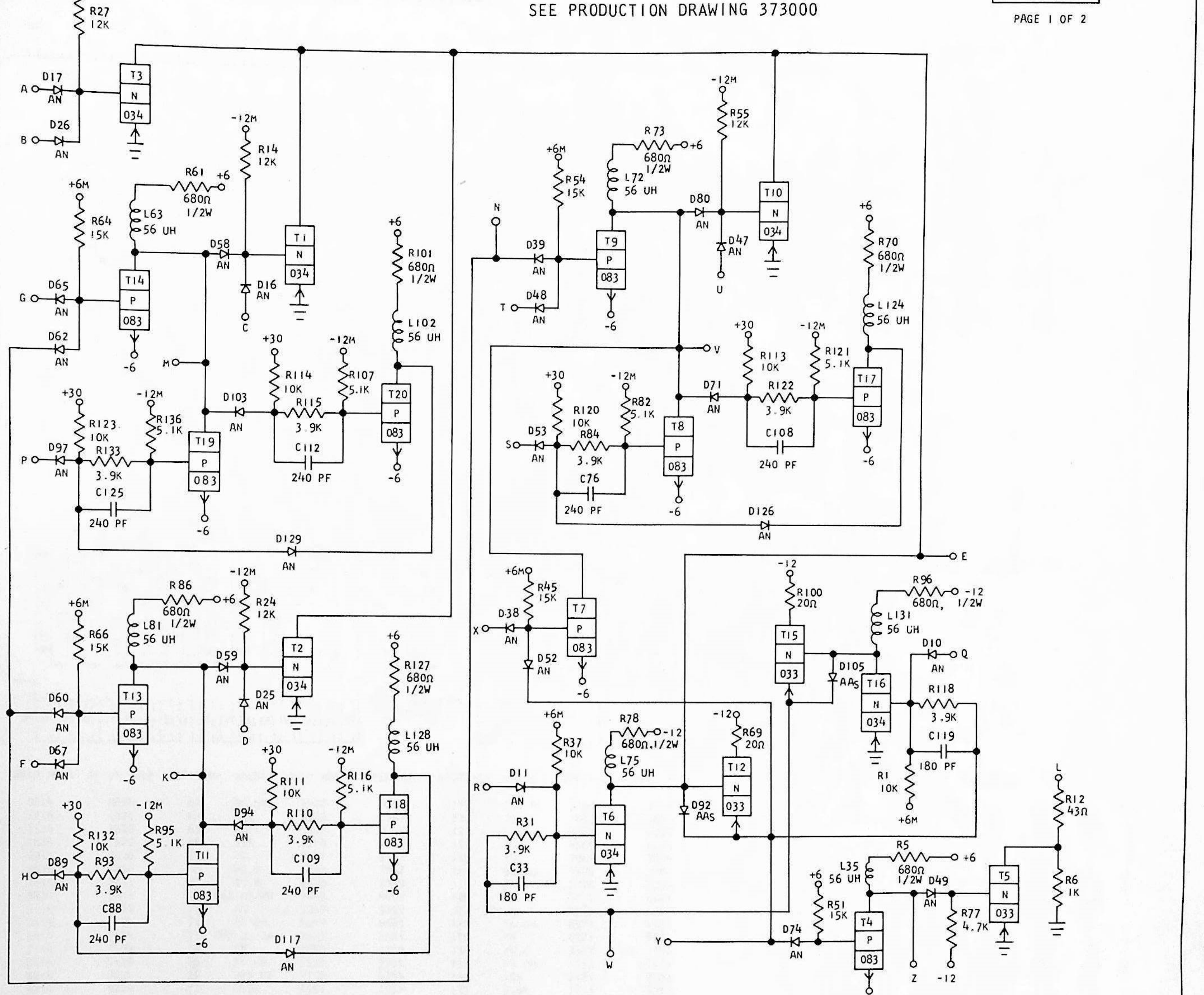
REFERENCE DRAWING

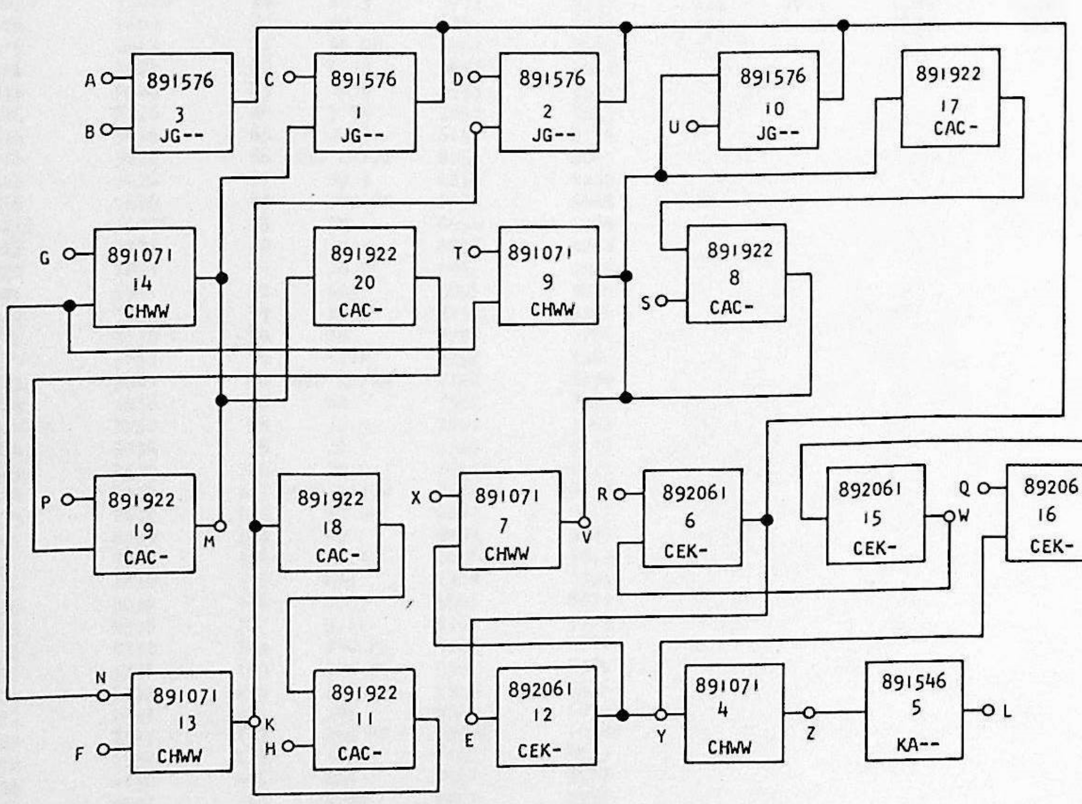
SEE PRODUCTION DRAWING 373000

CARD CODE	729801
A D B -	

PAGE 1 OF 2

SHEET 1 OF 2





VOLTAGE	PIN
GROUND	1
-6	2
+6	3
-12	4
+30	5
+6M	7
-12M	8

SEQUENCE OF OPERATION

1. THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF THE BLOCK DIAGRAM REFER TO A TRANSISTOR OF THE SAME NUMBER IN THE DETAILED SCHEMATIC
2. THE 800,000 SERIES NUMBER IN EACH BLOCK REFERS TO THE ENGINEERING SPECIFICATION FOR THAT PARTICULAR CIRCUIT
3. THE CARD AND CAP CODE IN EACH BLOCK REFERS TO THE RESPECTIVE PORTION OF THE DETAILED CIRCUITRY
4. FOR INFORMATION PERTAINING TO WAVE FORMS OF EACH INDIVIDUAL CIRCUIT, REFER TO THE CARD AND CAP CODE OF THE CIRCUIT

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.

NAME	TWIN CARD ASSEMBLY- ALLOY		
	STORAGE ADDRESS REGISTER		
DESIGN		MODEL	SMS
DETAIL	RJ 3-1-62	SCALE	NONE
CHECK	WH 3-1-62	DRAW	LIG 3-17-62
APPRO		CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
/ /-62	115599					

729801

C

STANDARDS CODE
2-7045

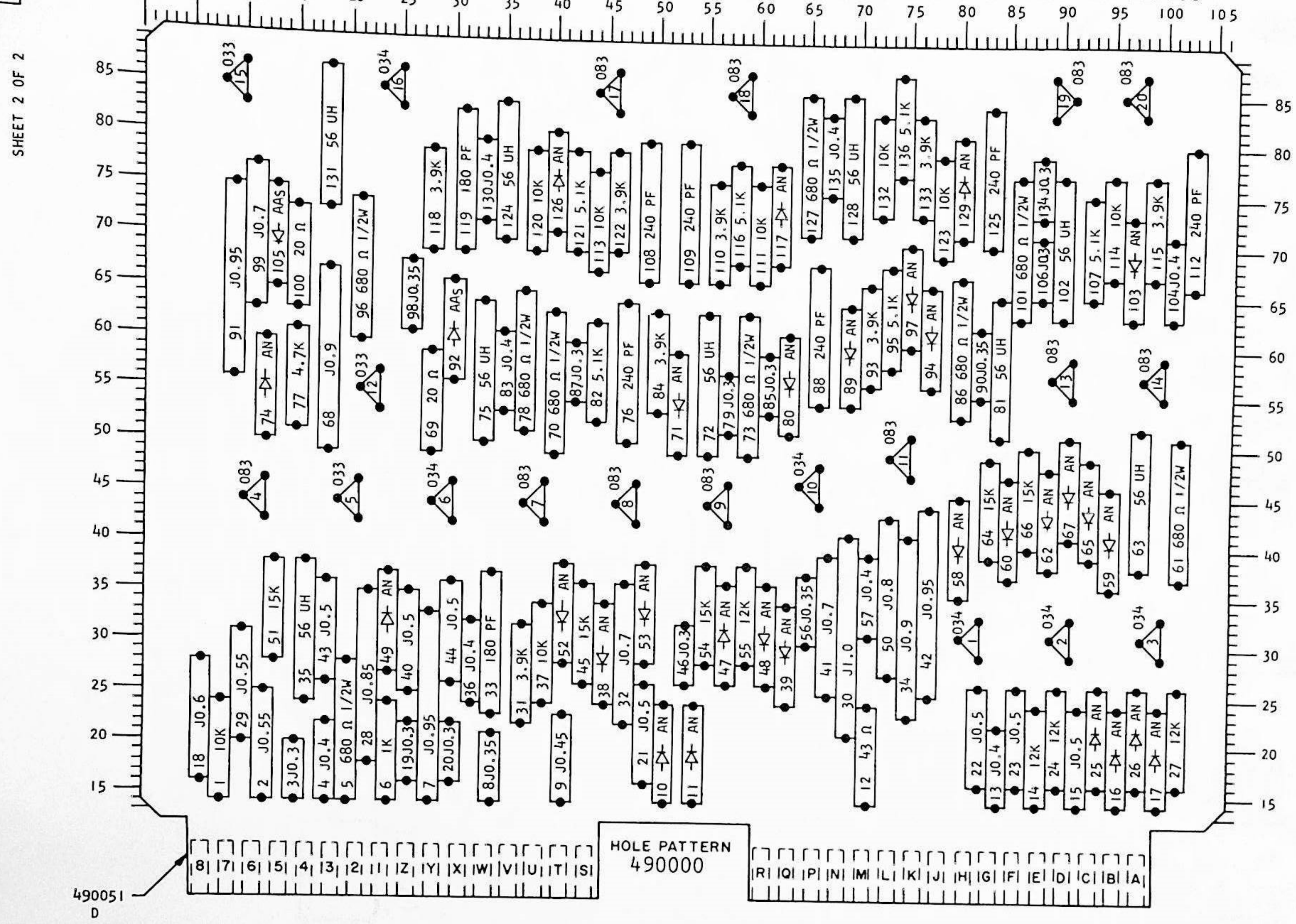
729801

SHEET 2 OF 2

REFERENCE DRAWING

CARD CODE	729801
A D B -	

SEE PRODUCTION DRAWING 373000



PAGE 2 OF 2

PART NO	VALUE	QTY.
216445	1K	1
216458	3.9K	8
216460	4.7K	1
216461	5.1K	6
216468	10K	8
216470	12K	4
216472	15K	5
317014	680 Ω1/2W	9
350437	240 PF	6
483051	43 Ω	1
483052	20 Ω	2
491007	AN	29
491008	AAs	2
350434	180 PF	2
491311	56 UH	9
318324	033	3
318325	083	11
535009	034	6

POSITION	VALUE	LOWER HOLE	UPPER HOLE	POSITION	VALUE	LOWER HOLE	UPPER HOLE	POSITION	VALUE	LOWER HOLE	UPPER HOLE
1	10K	0814	0824	63	56 UH	9838	9852	119	180 PF	3169	3183
2	J0.55	1214	1225	64	15K	8339	8349	120	10K	3869	3879
3	J0.3	1514	1520	65	AN	9339	9349	121	5.1K	4269	4279
4	J0.4	1814	1822	66	15K	8740	8750	122	3.9K	4669	4679
5	680 Ω1/2	2014	2028	67	AN	9141	9151	123	10K	7869	7879
6	1K	2414	2424	68	J0.9	1849	1867	124	56 UH	3570	3584
7	J0.95	2814	2833	69	20 Ω	2849	2859	125	240 PF	8370	8384
8	J0.35	3414	3421	70	680 Ω1/2W	4049	4063	126	AN	4071	4081
9	J0.45	4114	4123	71	AN	5249	5259	127	680 Ω1/2W	6571	6585
10	AN	5114	5124	72	56 UH	6549	6563	128	56 UH	6971	6985
11	AN	5414	5424	73	680 Ω1/2W	5949	5963	129	AN	8071	8081
12	43 Ω	7114	7124	74	AN	1250	1260	130	J0.4	3372	3380
13	J0.4	8414	8422	75	56 UH	3350	3364	131	56 UH	1873	1887
14	12K	8814	8824	76	240 PF	4750	4764	132	10K	7273	7283
15	J0.5	9214	9224	77	4.7K	1551	1561	133	3.9K	7673	7683
16	AN	9614	9624	78	680 Ω1/2W	3751	3765	134	J0.3	8873	8879
17	AN	10014	10024	79	J0.3	5751	5757	135	J0.4	6775	6783
18	J0.6	0616	0628	80	AN	6351	6361	136	5.1K	7477	7487
19	J0.3	2616	2622	81	56 UH	8451	8465				
20	J0.3	3016	3022	82	5.1K	4452	4462				
21	J0.5	4916	4926	83	J0.4	3553	3561				
22	J0.5	8216	8226	84	3.9K	5053	5063				
23	J0.5	8616	8626	85	J0.3	6153	6159				
24	12K	9016	9026	86	680 Ω1/2W	8053	8067				
25	AN	9416	9426	87	J0.3	4254	4260				
26	AN	9816	9826	88	240 PF	6654	6668				
27	12K	10216	10226	89	AN	6954	6964				
28	J0.85	2218	2235	90	J0.35	8255	8262				
29	J0.55	1020	1031	91	J0.95	0956	0975				
30	J1.0	6921	6941	92	AAs	3056	3066				
31	3.9K	3722	3732	93	3.9K	7156	7166				
32	J0.7	4722	4736	94	AN	7756	7766				
33	180 PF	3423	3437	95	5.1K	7358	7368				
34	J0.9	7523	7541	96	680 Ω1/2W	2160	2174				
35	56 UH	1624	1638	97	AN	7560	7570				
36	J0.4	3224	3232	98	J0.35	2661	2668				
37	10K	3924	3934	99	J0.7	1163	1177				
38	AN	4524	4534	100	20 Ω	1563	1573				
39	AN	6324	6334	101	680 Ω1/2W	8663	8677				
40	J0.5	2625	2635	102	56 UH	9063	9077				
41	J0.7	6725	6739	103	AN	9763	9773				
42	J0.95	7725	7744	104	J0.4	10163	10171				
43	J0.5	1826	1836	105	AAs	1365	1375				
44	J0.5	3026	3036	106	J0.3	8865	8871				
45	15K	4326	4336	107	5.1K	9365	9375				
46	J0.3	5326	5332	108	240 PF	4966	4980				
47	AN	5726	5736	109	240 PF	5366	5380				
48	AN	6126	6136	110	3.9K	5666	5676				
49	AN	2427	2437	111	10K	6066	6076				
50	J0.8	7327	7343	112	240 PF	10366	10380				
51	15K	1328	1338	113	10K	4467	4477				
52	AN	4128	4138	114	10K	9567	9577				
53	AN	4928	4938	115	3.9K	9967	9977				
54	15K	5528	5538	116	5.1K	5868	5878				
55	12K	5928	5938	117	AN	6268	6278				
56	J0.35	6530	6537	118	3.9K	2869	2879				
57	J0.4	7131	7139								
58	AN	8035	8045								
59	AN	9536	9546								
60	AN	8537	8547								
61	680 Ω1/2W	10237	10251								
62	AN	8938	8948								

POSITION	TYPE	E	B	C
1	034	8233	8031	8229
2	034	9133	8931	9129
3	034	10033	9831	10029
4	083	1246	1044	1242
5	033	2146	1944	2142
6	034	3046	2844	3042
7	083	3946	3744	3942
8	083	4846	4644	4842
9	083	5746	5544	5742
10	034	6648	6446	6644
11	083	7551	7349	7547
12	033	2357	2155	2353
13	083	9159	8957	9155
14	083	10059	9857	10055
15	033	1087	0885	1083
16	034	2587	2385	2583
17	083	4687	4485	4683
18	083	5987	5785	5983
19	083	8983	9185	8987
20	083	9887	9685	9883

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	TWIN CARD ASSEMBLY-ALLOY				6 19 62	115599					729801
STORAGE ADDRESS REGISTER											
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

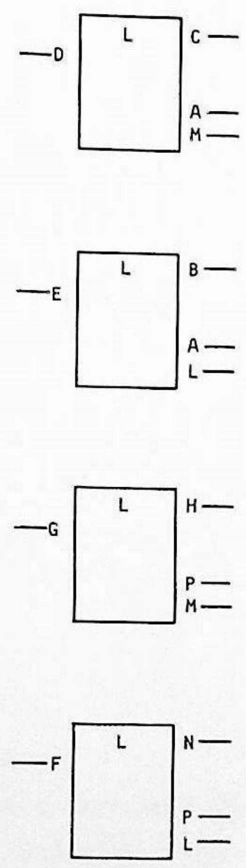
STANDARDS CODE

729802

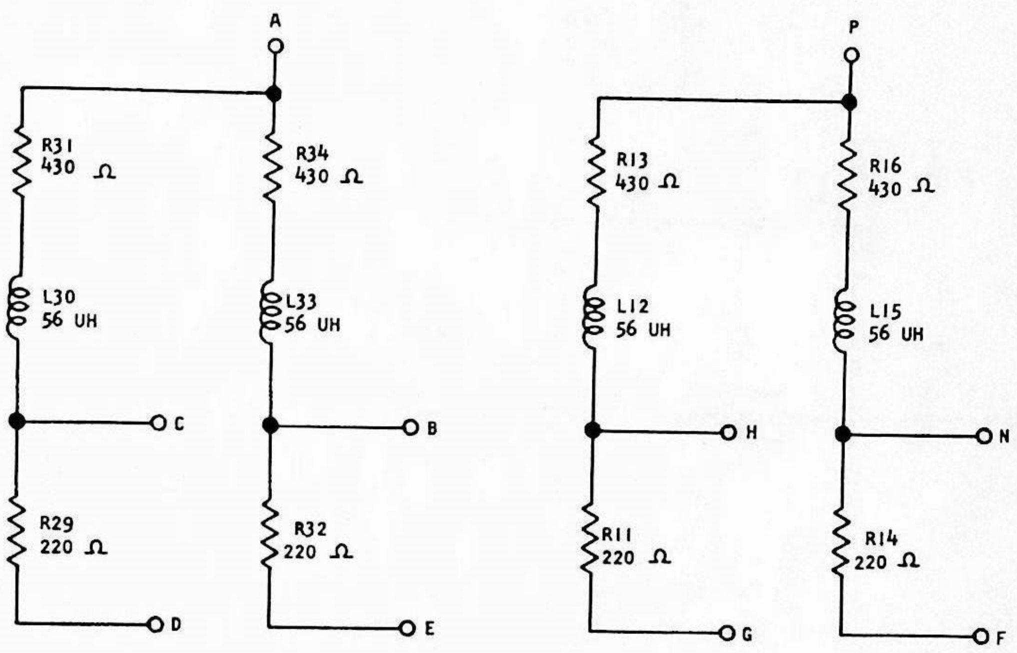
CARD CODE	729802
A E A -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371929

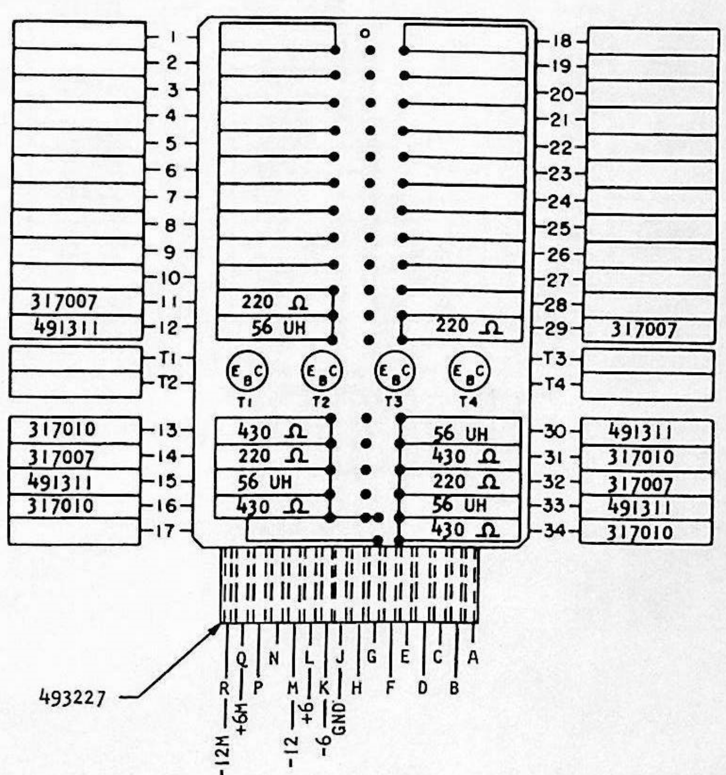


CTDL LOAD CARD



SEQUENCE OF OPERATION

1. AS COLLECTOR LOAD FOR CTDL BLOCK TO PROVIDE CURRENT MODE OUTPUT
2. A AND P CONNECTED TO +6 VOLTS; D, E, G, F ARE T LEVEL INPUTS AND C, B, H, N ARE N LEVEL OUTPUTS
3. A AND P CONNECTED TO -12 VOLTS; D, E, G, F ARE U LEVEL INPUTS AND C, B, H, N ARE P LEVEL OUTPUTS



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL LOAD CARD				6 -62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729802

C

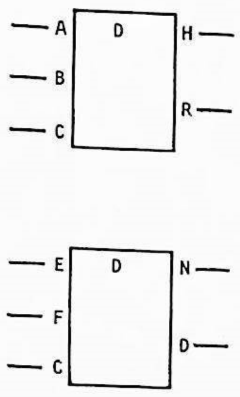
STANDARDS CODE
729803

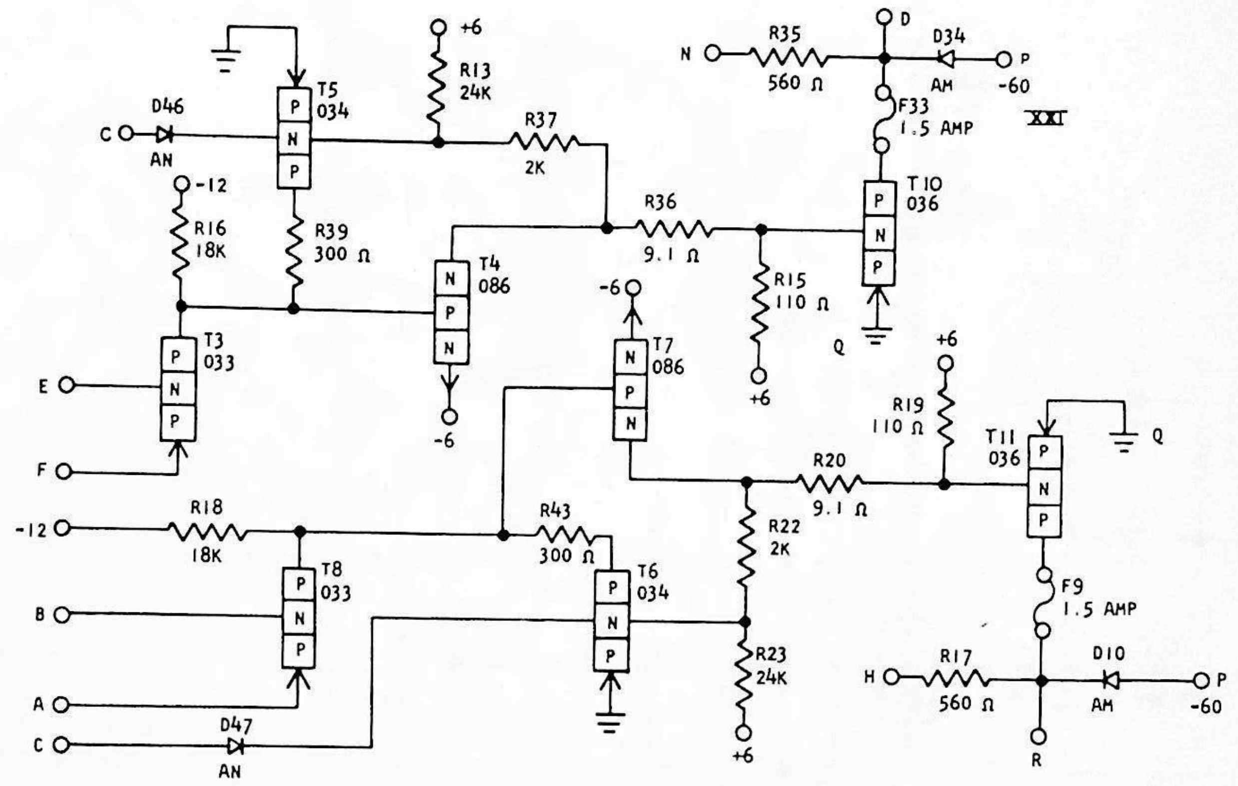
CARD CODE	729803
A E C -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371940

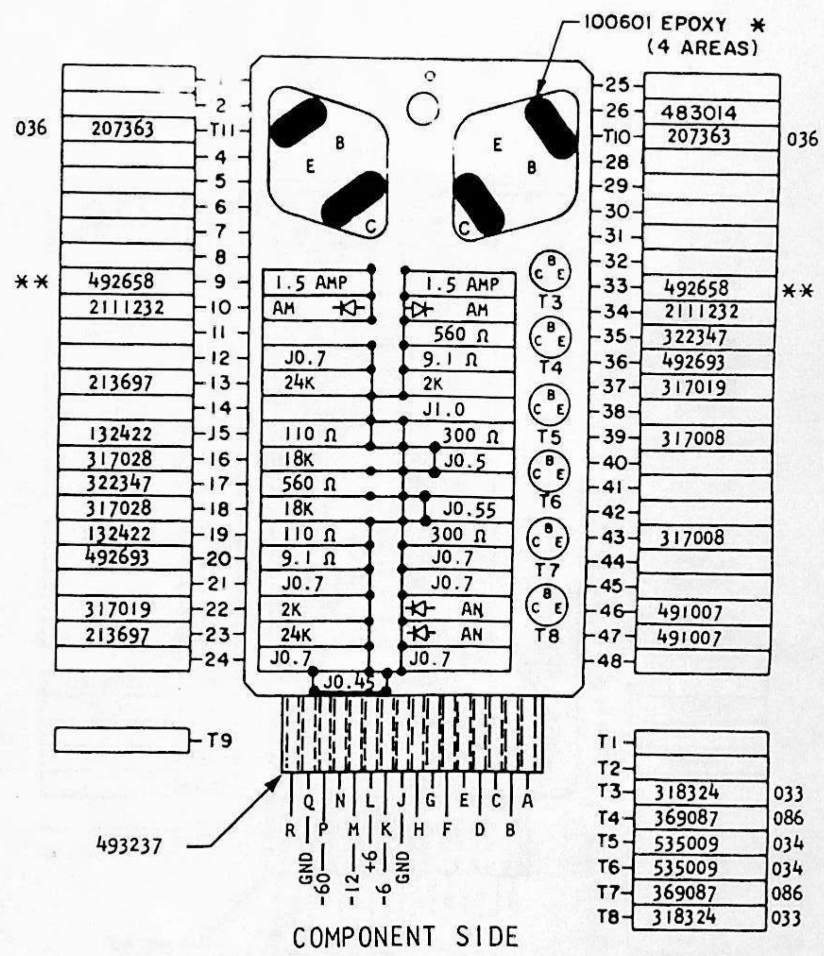
ALLOY HAMMER DRIVER LATCH





SEQUENCE OF OPERATION

1. WHEN INPUTS AT E (GATE) AND F (SET) ARE IN COINCIDENCE T3 TURNS ON
2. WITH T3 ON, T4 TURNS ON, T5 TURNS ON AND LATCHES T4
3. T10 TURNS ON THE OUTPUT IS GND
4. WHEN C (RESET) IS UP T5, T4, T10 TURN OFF AND THE OUTPUT IS -60V
5. FAILURE TO RESET PROPERLY WILL RESULT IN BLOWN FUSE



PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
E,B	N	GATE		UP	+5.61	+6.24
				DOWN	-1.19	-3.91
A,F	T	SET		UP	-3.91	-.71
				DOWN	-5.46	-6.24
C	T	RESET		UP	+1.44	+6.24
				DOWN	-.81	-6.24
H,N			HAMMER CHECK DRIVE	UP		
				DOWN		
D,R	V	OUTPUT		UP	-2.5	-0
				DOWN	-54	-60

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

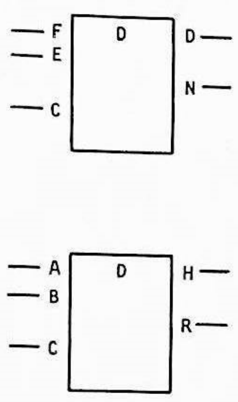
INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR - ALLOY HAMMER DRIVER LATCH				4-11-62	115599					
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW LIG	3-17-62							
APPRO		CHECK								

729803

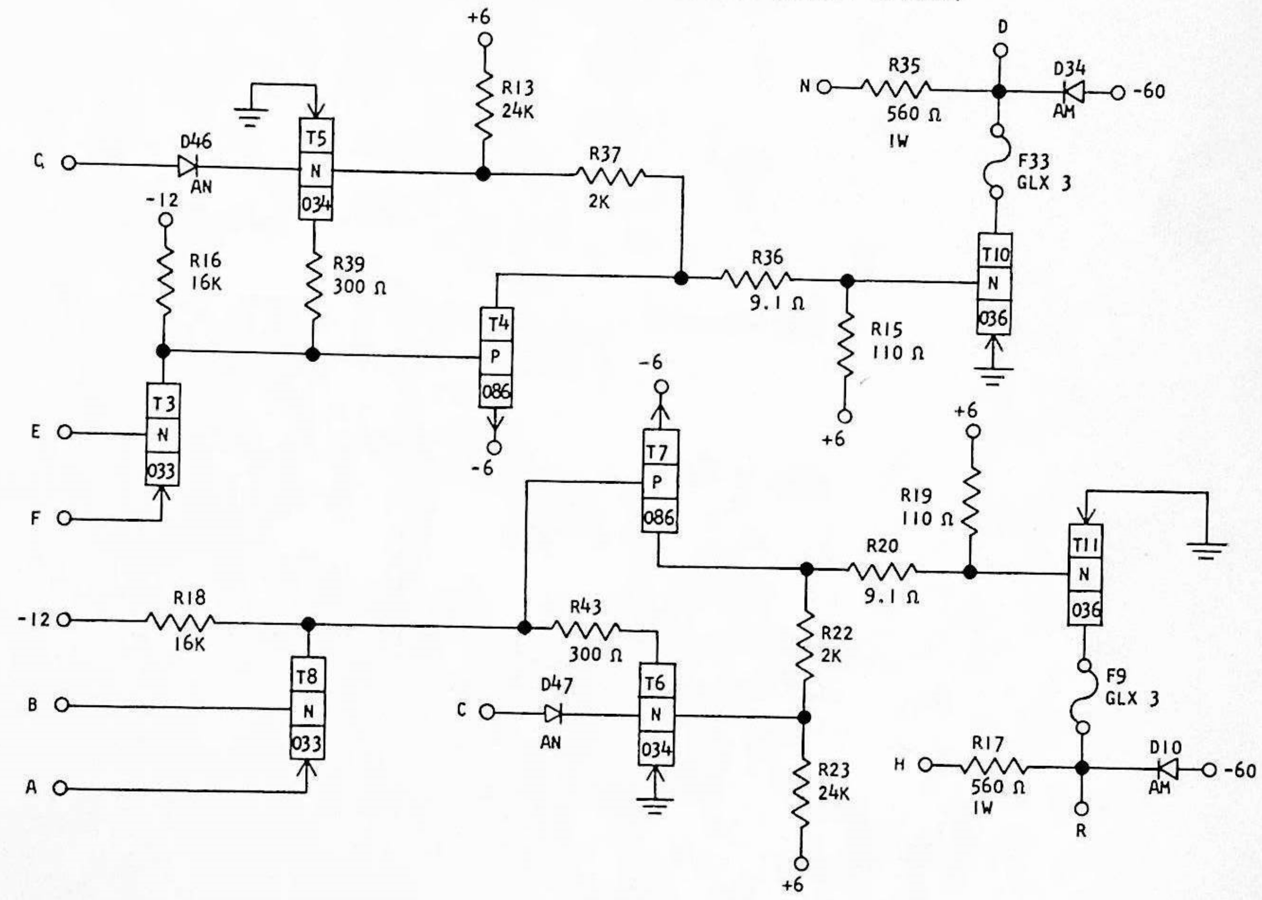
C

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371415



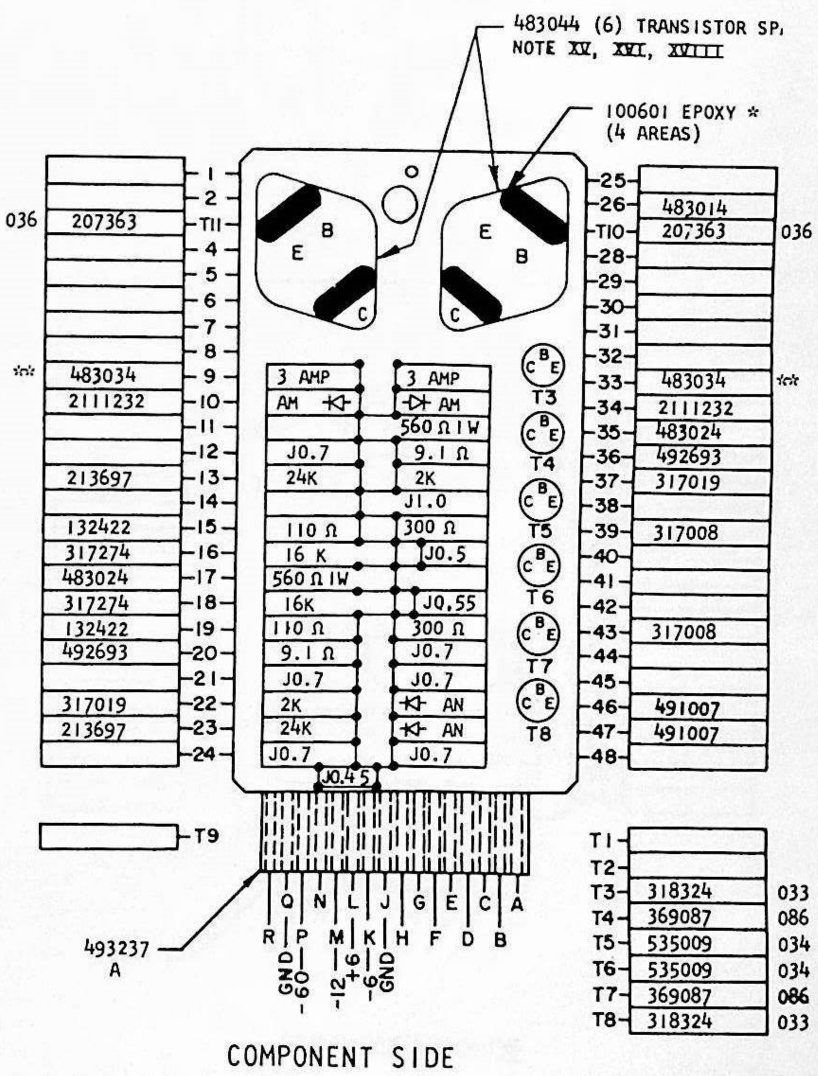
ALLOY HAMMER DRIVER LATCH (HIGH SPEED)



SEQUENCE OF OPERATION

1. WHEN INPUTS AT E (GATE) AND F (SET) ARE IN COINCIDENCE T3 TURNS ON
2. WITH T3 ON, T4 TURNS ON, T5 TURNS ON, AND LATCHES T4
3. T10 TURNS ON, THE OUTPUT IS GROUND
4. WHEN C (RESET) IS UP, T5 TURNS OFF, T4 TURNS OFF, T10 TURNS OFF AND THE OUTPUT IS -60V

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
F,A	T	SET		UP	-3.91	-.71
				DOWN	-5.46	-6.24
E,B	N	GATE		UP	5.71	6.24
				DOWN	-1.19	-3.91
C	T	RESET		UP	1.44	6.24
				DOWN	-.81	-6.24
N,H		HAMMER CHECK DRIVE		UP		
				DOWN		
R,D	V	OUTPUT		UP	-2.5	0
				DOWN	-54	-60



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY HAMMER DRIVER LATCH (HIGH SPEED)				6-29-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

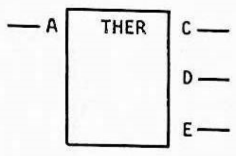
STANDARDS CODE
729806

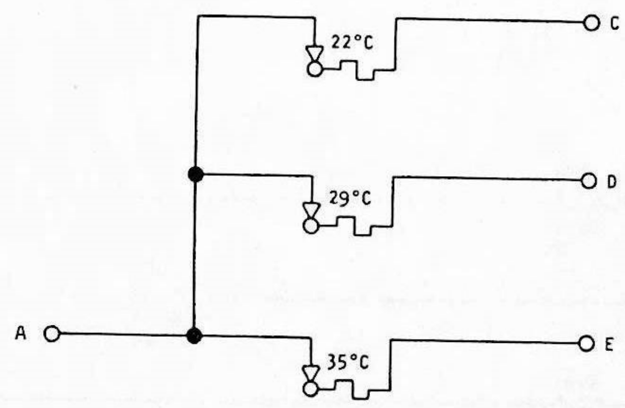
CARD CODE	729806
A K B -	

REFERENCE DRAWING

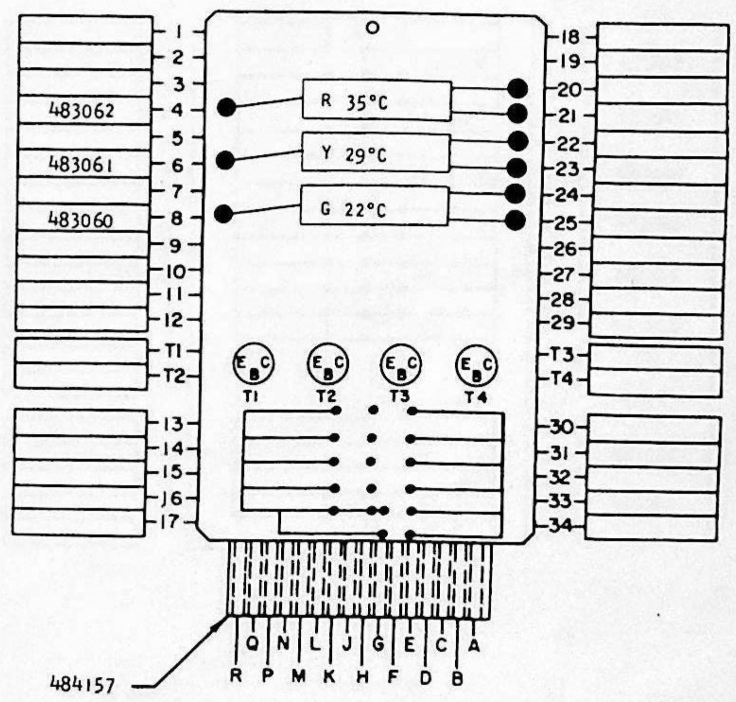
SEE PRODUCTION DRAWING 370425

ALLOY-MEMORY THERMAL SWITCHES





1. CARD CONTROLS DRIVE CURRENT BY DECREASING CURRENT FOR AN INCREASE IN MEMORY AMBIENT TEMPERATURE



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR -ALLOY- MEMORY THERMAL SWITCHES				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-[illegible]-62	115599					

729806

C

STANDARDS CODE

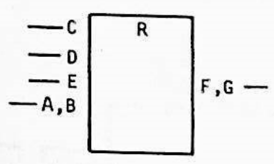
729807

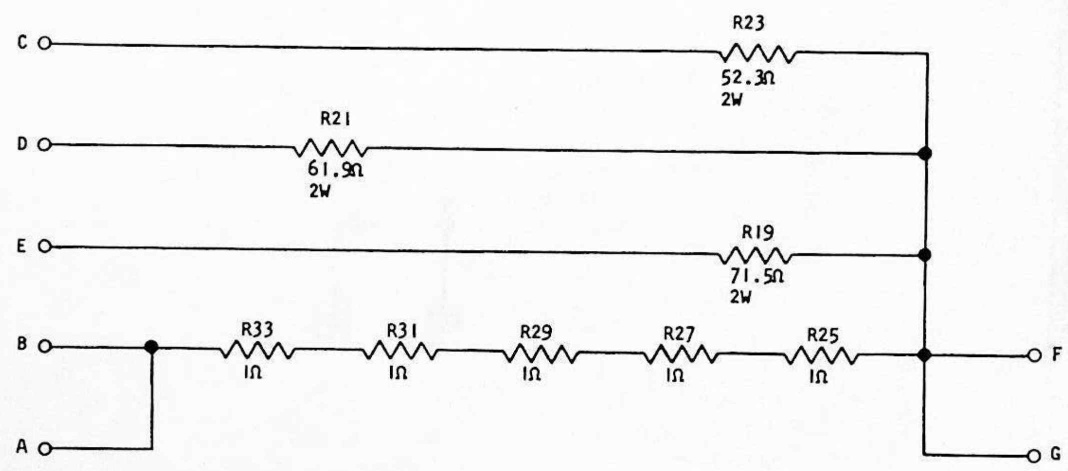
CARD CODE	729807
A K C -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370426

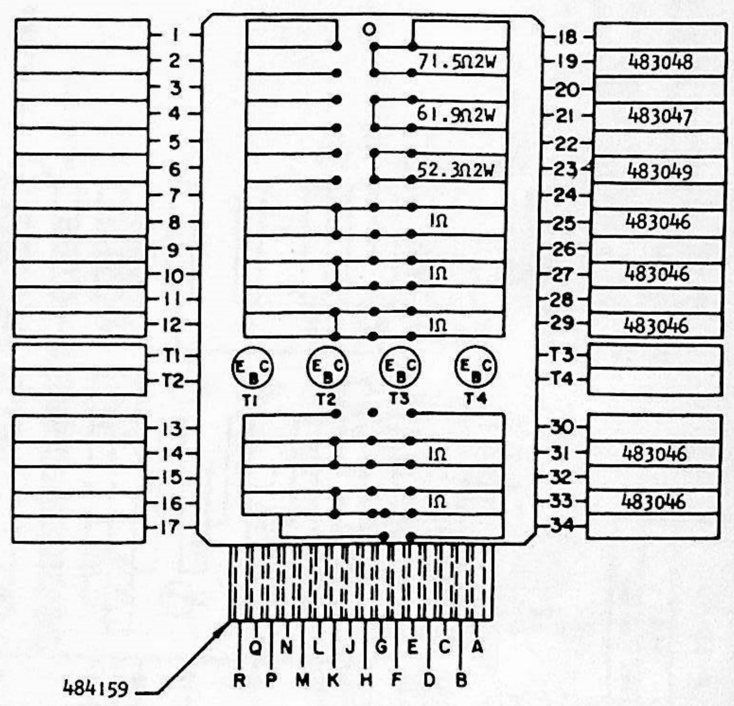
MEMORY EMITTER RESISTORS





SEQUENCE OF OPERATION

1. CARD CONTAINS PORTION OF EMITTER RESISTANCE OF A MEMORY CONSTANT CURRENT DRIVE SOURCE
2. RESISTORS LOCATED BETWEEN EMITTER AND EMITTER RETURN VOLTAGE ARE SWITCHED OUT OF CIRCUIT AS TEMPERATURE INCREASES



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR - MEMORY EMITTER RESISTORS				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6 24 -62	115599					

729807

FORM 82-001

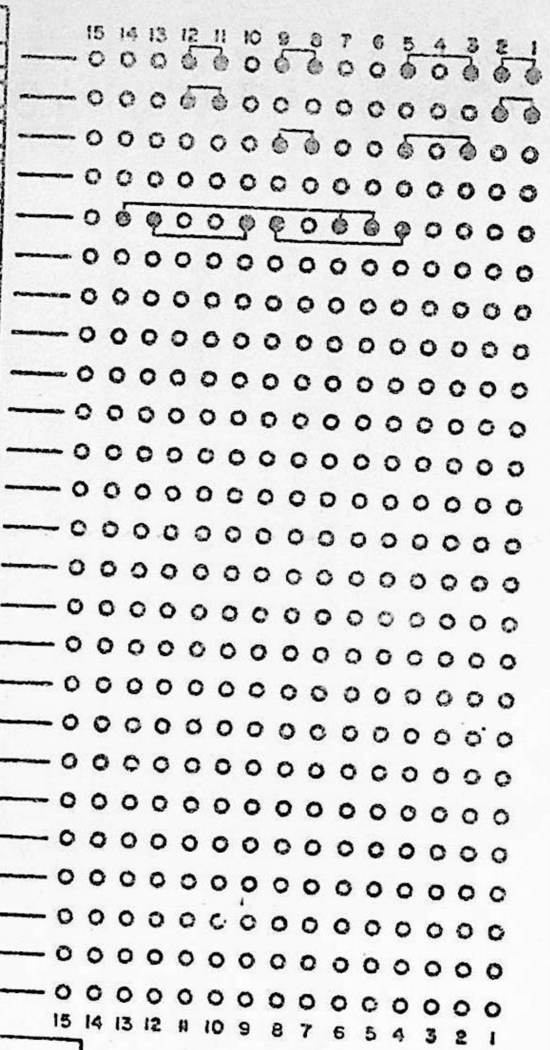
C

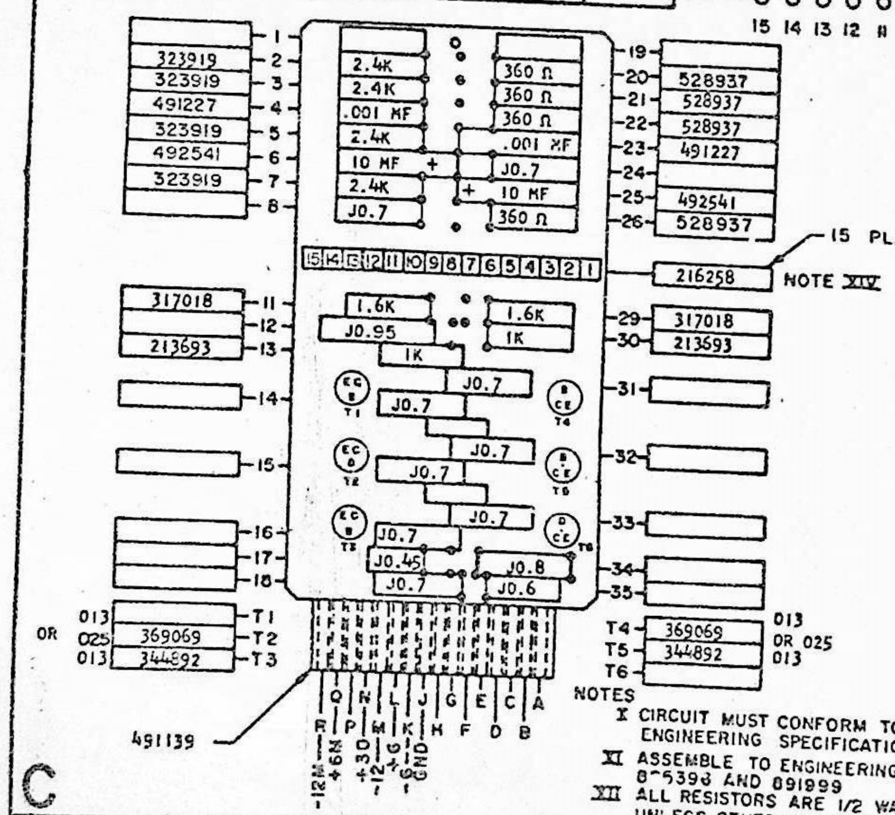
ALLOY - FIELD REPLACEMENT, AM CARD

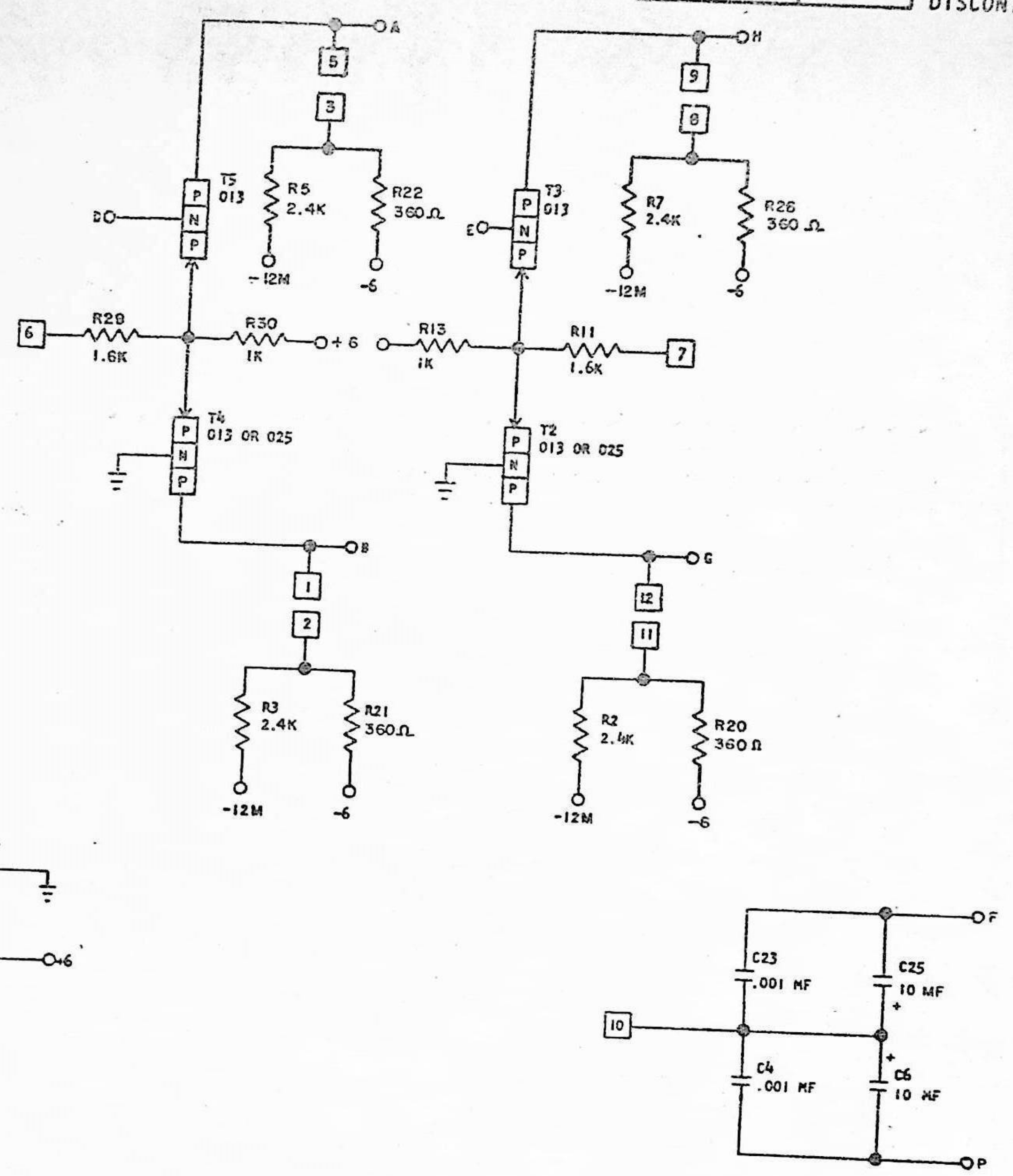
CARD CODE	STANDARDS CODE	370904
AM **	2-7045	DISCONTINUED

CAP CONFIGURATION

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC
ONE WAY N BLOCKS ALL LOADS	ZZ	371200	891200
ONE WAY N BLOCKS IN ϕ LOADS	ZY	371201	891201
ONE WAY N BLOCKS OUT ϕ LOADS	ZX	371202	891202
ONE WAY N BLOCKS NO LOADS	- -	371203	891203
N TRANSMISSION LINE DRIVER	WX	371208	891208







NOTES

I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATIONS 891200 AND 891208

XI ASSEMBLE TO ENGINEERING SPECIFICATION 8-5393 AND 891999

XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED

XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491296

XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
KMT NPB	5-12-60

370904

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- ALLOY			7-14-60	108989	JWB				2547-1109
FIELD REPLACEMENT, AM CARD				11-15-60	110511	IWB				
DESIGN	TPA 5-5-60	TYPE	SMS							
DETAIL	TPA 5-5-60	SCALE	NONE							
CHECK	TJ 7-14-60	DRAW	VE 5-24-60							
APPRO	[illegible] 7-14-60	CHECK	[illegible] 5-24-60							

370904

729808

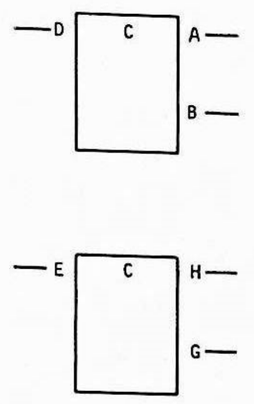
STANDARDS CODE

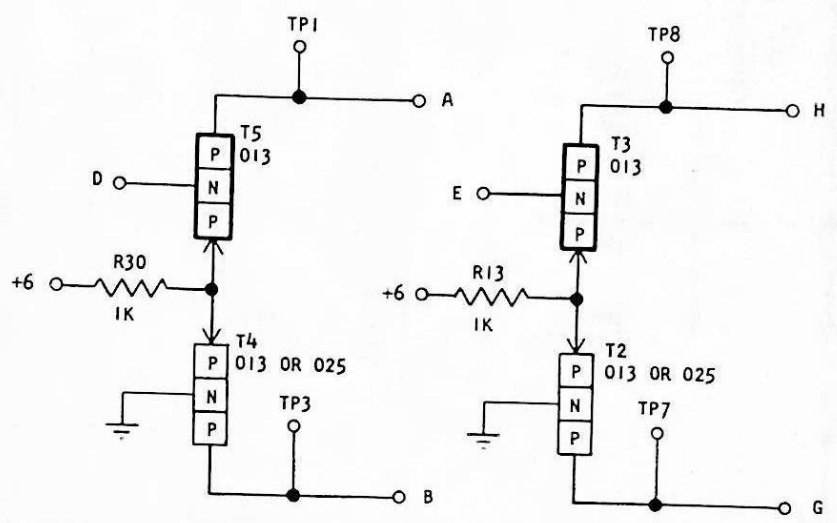
CARD CODE	729808
AM --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371203

ALLOY-ONE WAY "N" BLOCK





SEQUENCE OF OPERATION

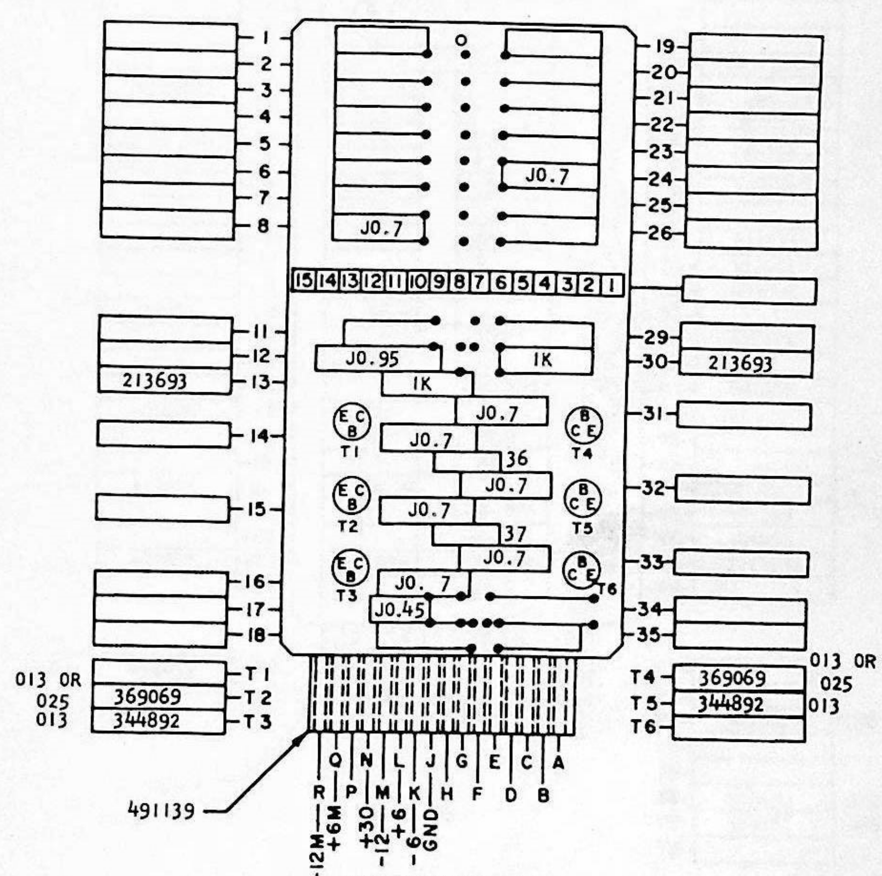
1. INPUT DOWN T5, T3 ON; T4, T2 OFF
2. INPUT UP T5, T3 OFF; T4,T2 ON
3. IN & OUT OF PHASE OUTPUTS AVAILABLE
4. COLLECTORS TIED TO COUPLING NETWORK

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D,E	N	INPUT		UP	+0.4	3.0
				DOWN	-0.4	-3.0
A,H	P	OUTPUT		UP	-5.6	-3.0
				DOWN	-6.4	-7.1
B,G	P	OUTPUT		UP	-5.6	-3.5
				DOWN	-6.4	-7.1

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	.17	.35
TURN OFF	.17	.35

NOTE: THE DELAYS WERE MEASURED AS THE TIME INTERVAL FROM THE CROSSING OF THE INPUT REFERENCE BY THE INPUT SIGNAL TO THE CROSSING OF THE OUTPUT REFERENCE BY THE OUTPUT SIGNAL.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.														
NAME	CARD ASM TSTR-ALLOY-ONE WAY "N" BLOCK				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
DESIGN			MODEL	SMS	6-27-62	115599					
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729808

C

STANDARDS CODE

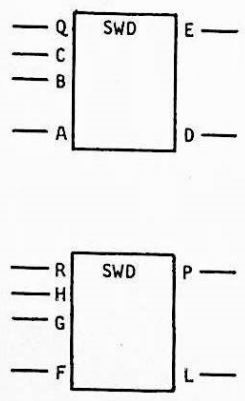
729809

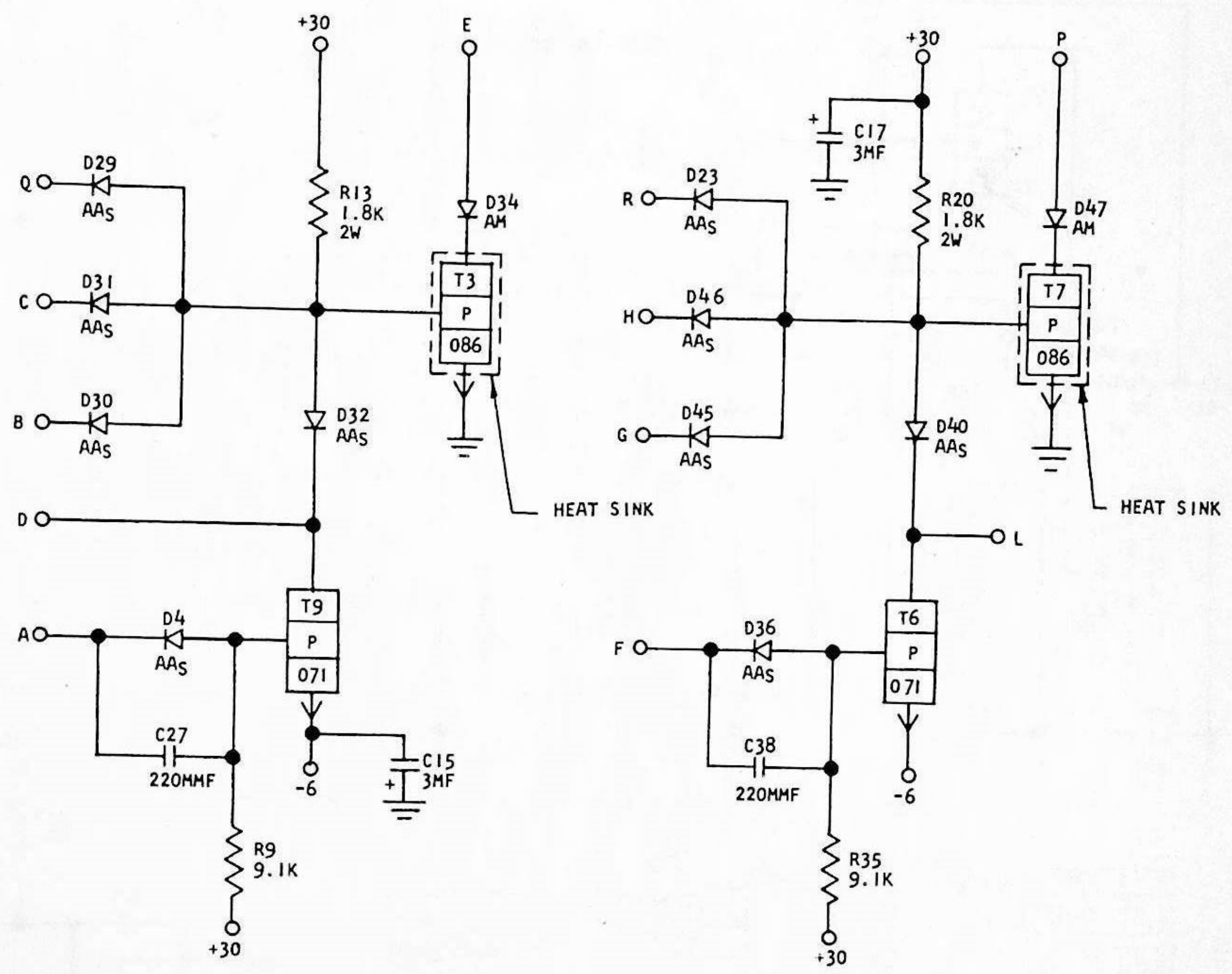
CARD CODE	729809
A Q U -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370833

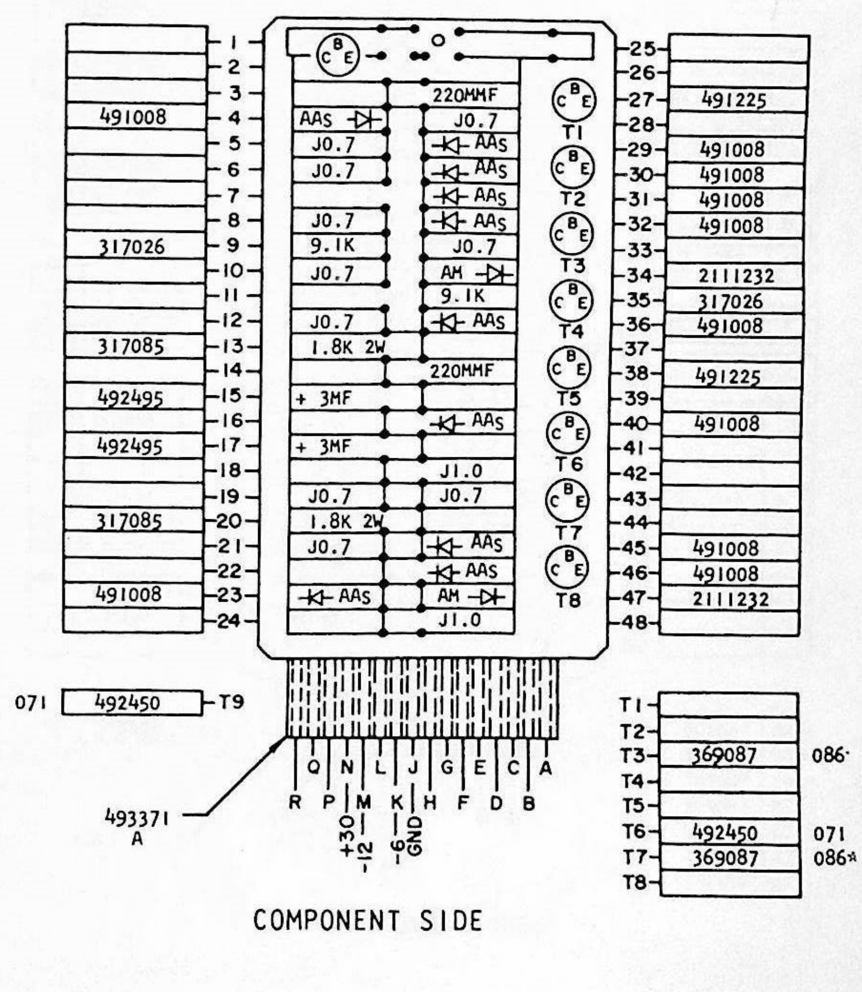
ALLOY SWITCH, DECODER NUMBER 2





SEQUENCE OF OPERATION

1. UP INPUTS TO T3, DOWN INPUT T9, T3 ON, T9 OFF MAX. CURRENT FLOWS IN T3
2. UP INPUTS TO T3, UP INPUT T9, T3 OFF T9 ON MIN CURRENT FLOWS IN T3
3. T6, T7 CONDITIONED BY SAME SEQUENCE
4. WHEN IN OFF CONDITION, OUTPUT ON T3 AND T7 WILL REFLECT THE VOLTAGES INDUCED FROM CORES.



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE (A → B)		LEVELS MIN	LEVELS MAX
A,F	U	INPUT		UP	-4.56	0.24
				DOWN	-6.84	-12.5
Q,R	T	INPUT		UP	1.74	14.76
				DOWN	-5.46	-6.24
C,H	T	INPUT		UP	1.74	14.76
				DOWN	-5.46	-6.24
B,G	T	INPUT		UP	1.74	14.76
				DOWN	-5.46	-6.24
D,L	T	OUTPUT		UP	1.74	14.76
				DOWN	-5.46	-6.24
E,P	Z	OUTPUT		UP	0.74	0.24
				DOWN		
T3 T7		INPUT		UP	1.74	14.76
				DOWN	-1.14	-9.76

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	----	0.36
TURN OFF	----	0.45

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-ALLOY SWITCH, DECODER NUMBER 2			6-27-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729809

FORM 01-001

C

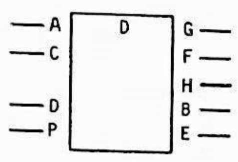
STANDARDS CODE
729810

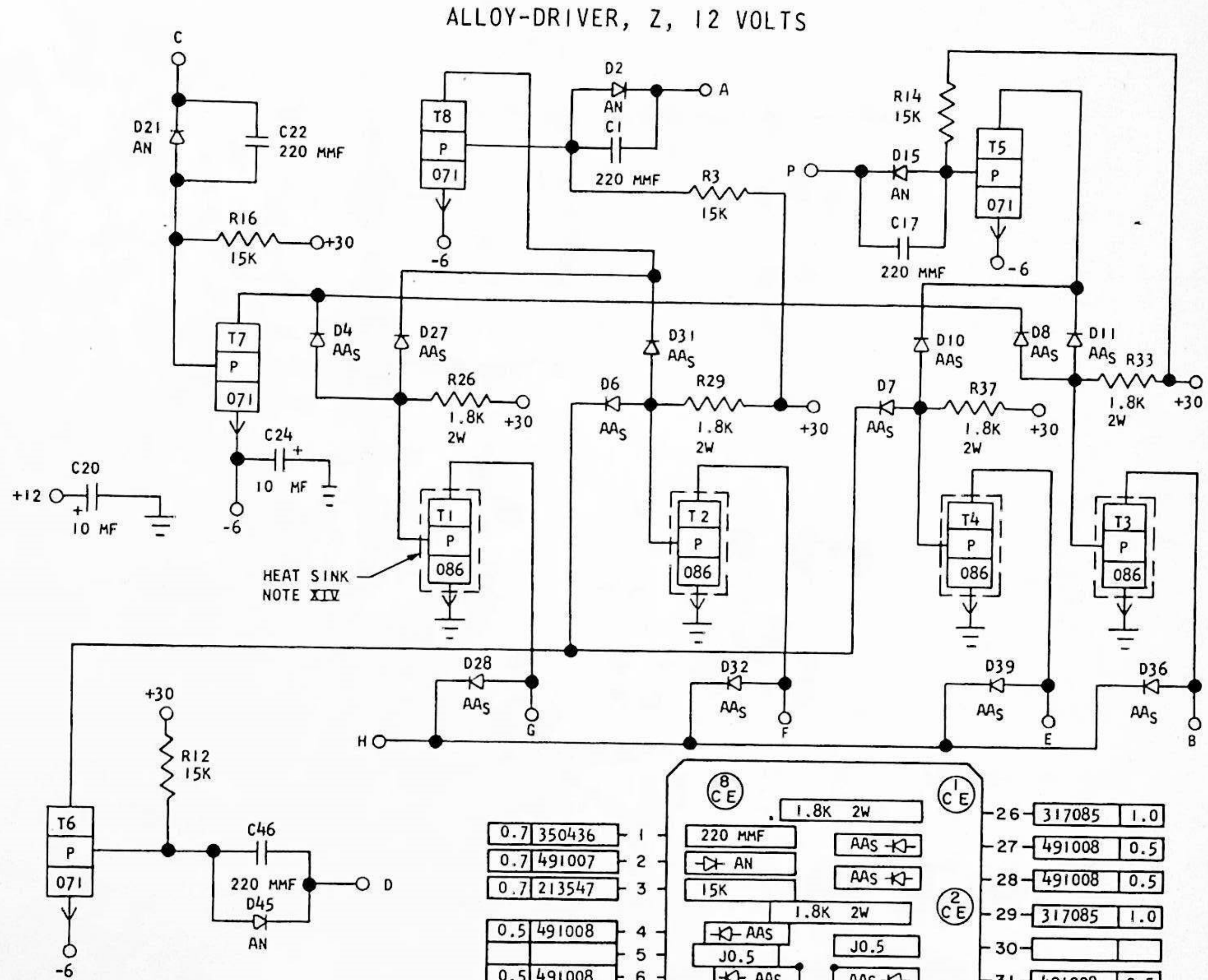
CARD CODE	729810
A Q V -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370834

ALLOY-DRIVER, Z, 12 VOLTS

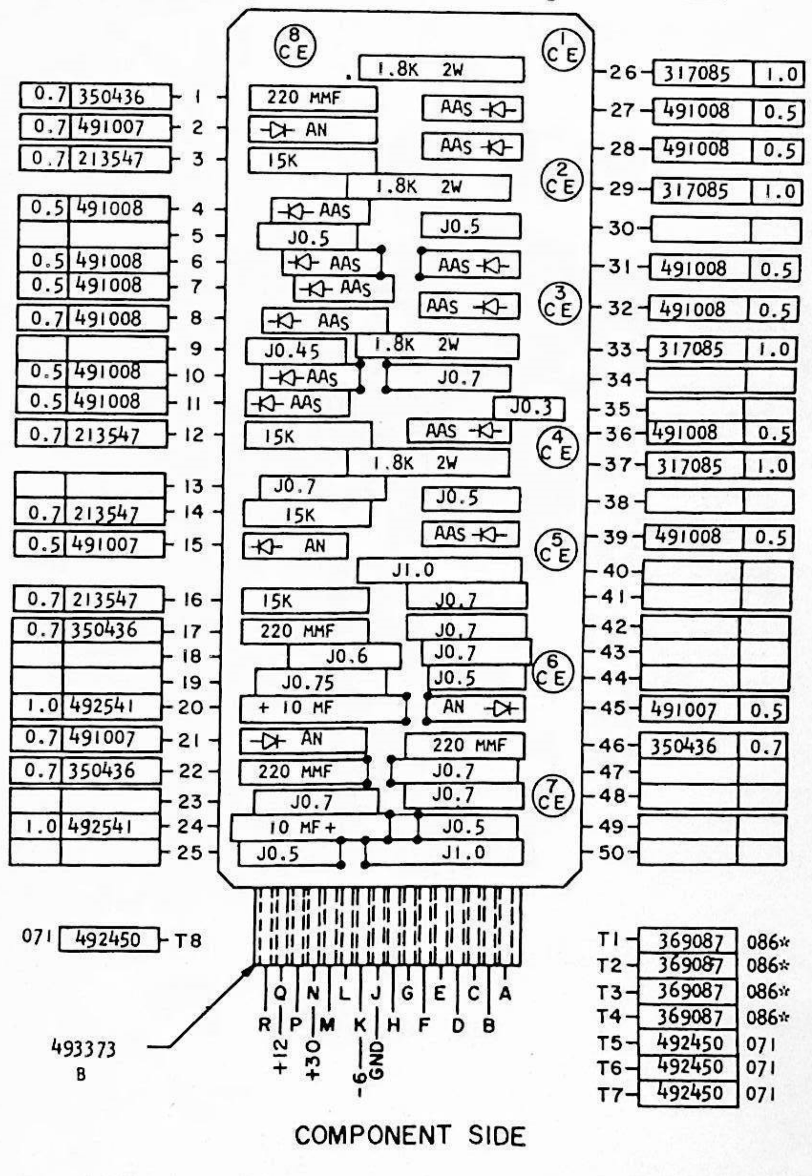




SEQUENCE OF OPERATION

1. PIN H TIED TO Q (+12)
2. WAVE SHAPE A T8,T5,T6,ON; T1,T2,T3,T4, T7 OFF
3. DOWN INPUT AT A, T8 OFF T1 ON, OUTPUT AT G DOWN
4. T7, T8 OFF, INPUT AT T1, +3. TO 4. VOLTS
5. DELAYS FROM INPUT TO OUTPUT, MEASURED FROM -6 VOLT LEVEL ON INPUT TO +6 VOLT LEVEL ON OUTPUT.
   TURN ON 0.9 USEC MAX
   TURN OFF 0.35 USEC MAX

PINS		SIGNAL NAME	WAVE SHAPE A	WAVE SHAPE B	LEVELS	MIN	MAX
A	U	INPUT			UP	-4.66	0.24
					DOWN	-7.44	-12.5
P	U	INPUT			UP	-4.66	0.24
					DOWN	-7.44	-12.5
C	U	INPUT			UP	-4.66	0.24
					DOWN	-7.44	-12.5
D	U	INPUT			UP	-4.66	0.24
					DOWN	-7.44	-12.5
G	U	OUTPUT			UP	+12	+12
					DOWN	-0.74	+0.24
F	U	OUTPUT			UP	+12	+12
					DOWN	-0.74	+0.24
B	U	OUTPUT			UP	+12	+12
					DOWN	-0.74	+0.24
E	U	OUTPUT			UP	+12	+12
					DOWN	-0.74	+0.24



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.			
NAME	CARD ASM TSTR - ALLOY-DRIVER, Z, 12 VOLTS		
DESIGN		MODEL	SMS
DETAIL	RQ 3-1-62	SCALE	NONE
CHECK	WH 3-1-62	DRAW	LIG 3-17-62
APPRO		CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-27-62	115599					

729810

C

STANDARDS CODE

729811

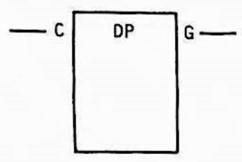
CARD CODE	729811
A Q W -	

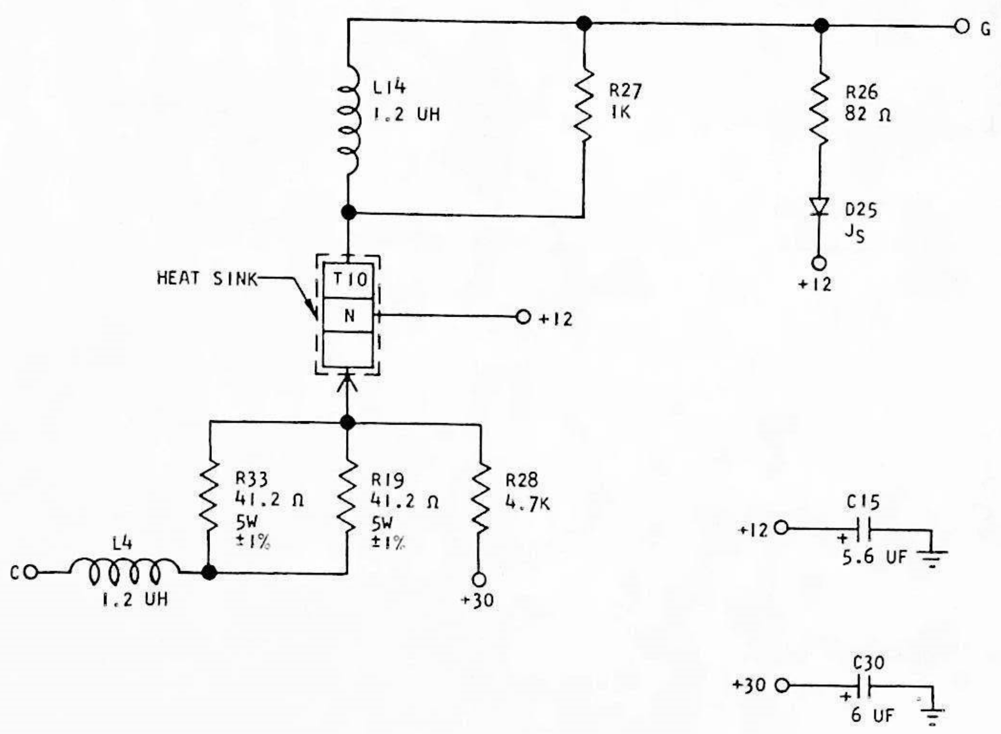
REFERENCE DRAWING

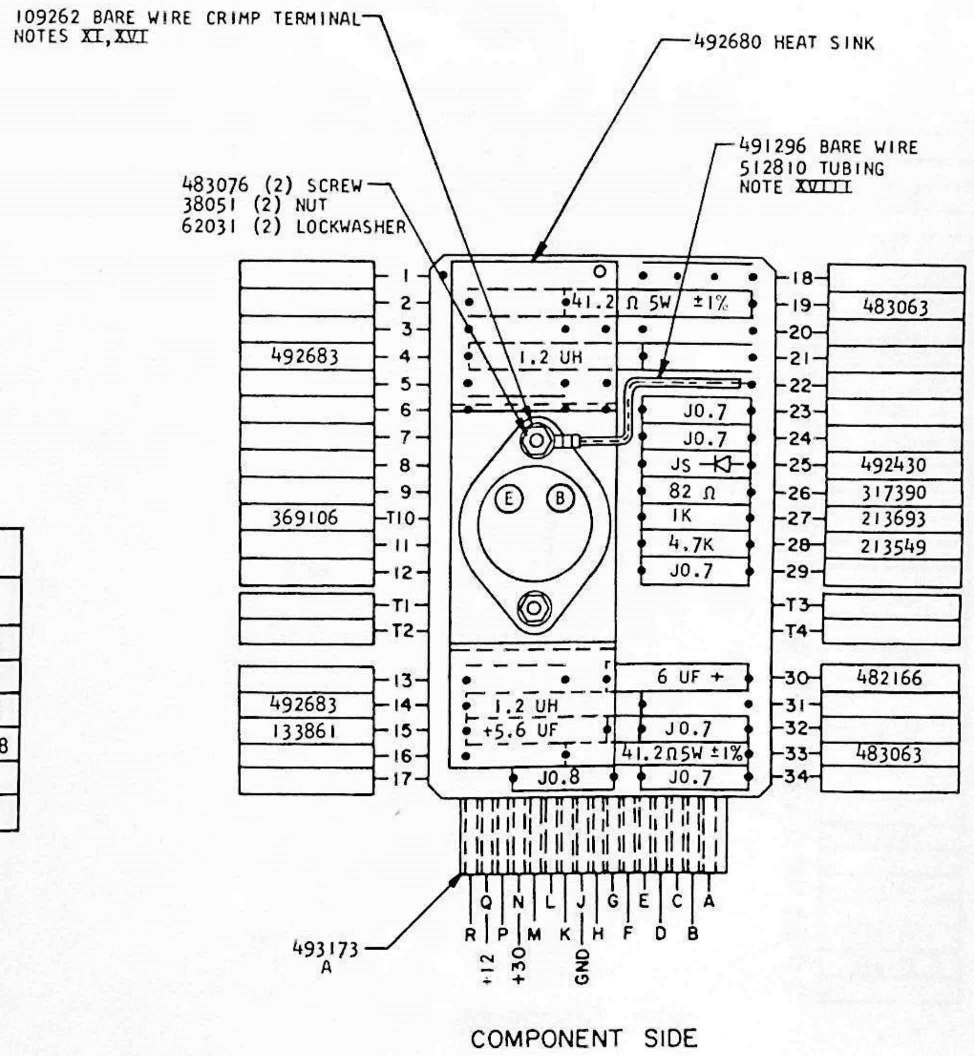
SEE PRODUCTION DRAWING 370835

ALLOY-CURRENT SOURCE #2

RECOMMEND MOUNT ON ONE INCH CENTERS NOTE XVII







SEQUENCE OF OPERATION

1. THIS CIRCUIT PROVIDES A CONSTANT CURRENT SOURCE WHEN POWER IS UP. TRANSISTOR IS ON WHEN POWER IS ON

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
C			VOLTAGE PIN	UP	+28.8	+31.2
				DOWN		
G		OUTPUT		UP		+11.0
				DOWN	-10.52	-11.48

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY - CURRENT SOURCE #2			/ /-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729811

C

STANDARDS CODE

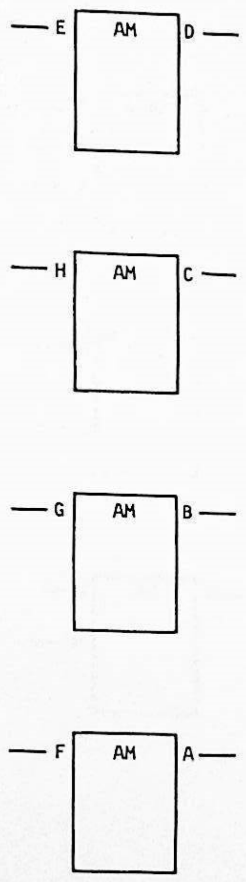
729812

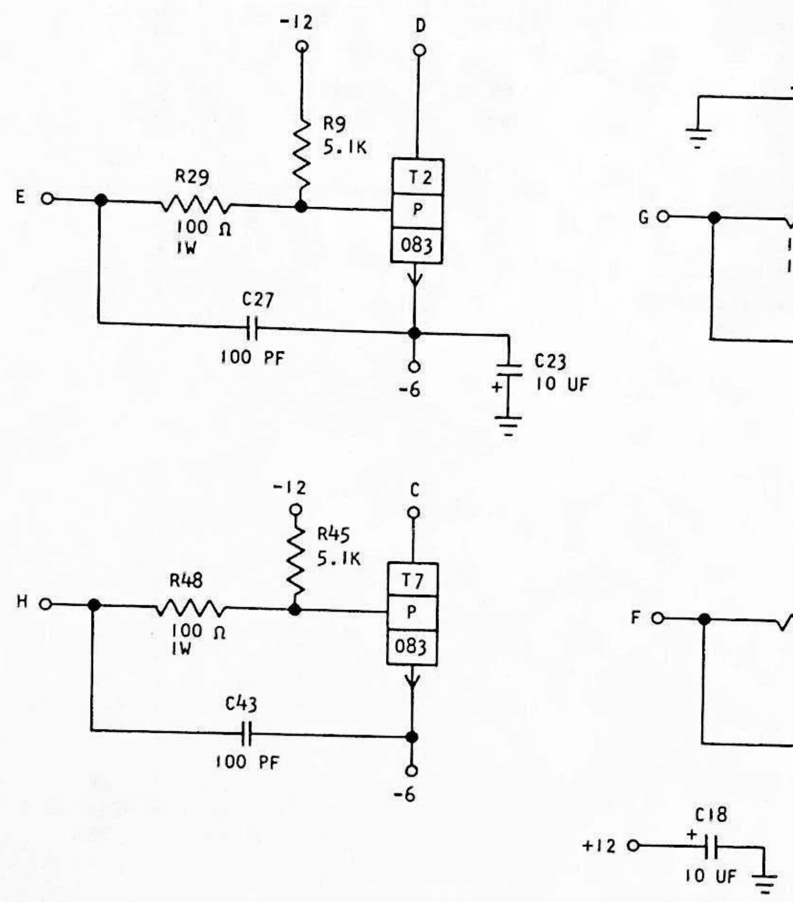
CARD CODE	729812
A Q X -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370836

SENSE - FINAL AMPLIFIER

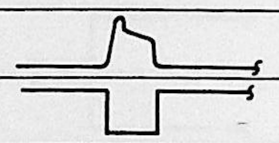


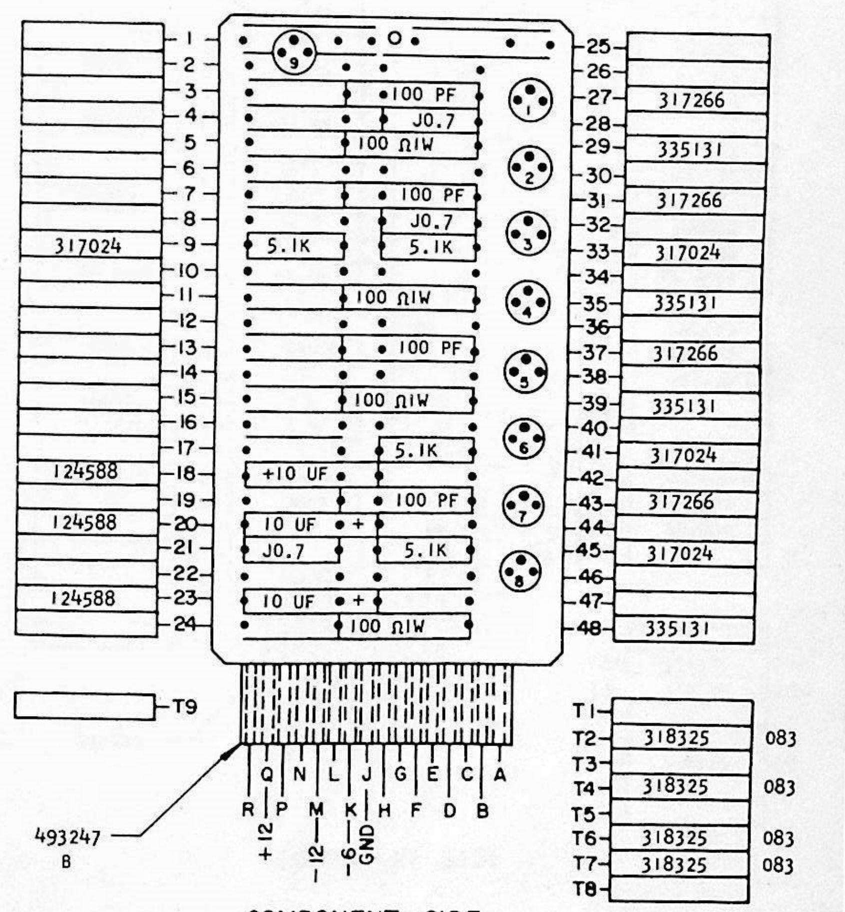


SEQUENCE OF OPERATION

1. INPUT UP, TRANSISTOR ON, OUTPUT DOWN. THIS CIRCUIT PROVIDES A -T LINE FROM A +U LINE INPUT. THE OFF OUTPUT VOLTAGE DEPENDS ON LOAD DRIVEN
2. DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.09	0.19
TURN OFF	0.44	2.00

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
E,H, G,F	U	INPUT		UP	-5.2	+.24
				DOWN	-11.52	-12.48
D,C, B,A	-T	OUTPUT		UP		
				DOWN	-5.46	-6.24



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - SENSE, FINAL AMPLIFIER				-62	115599					729812
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

STANDARDS CODE

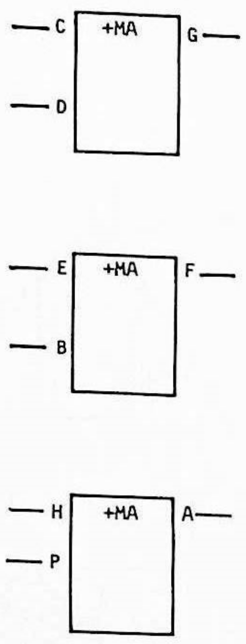
729813

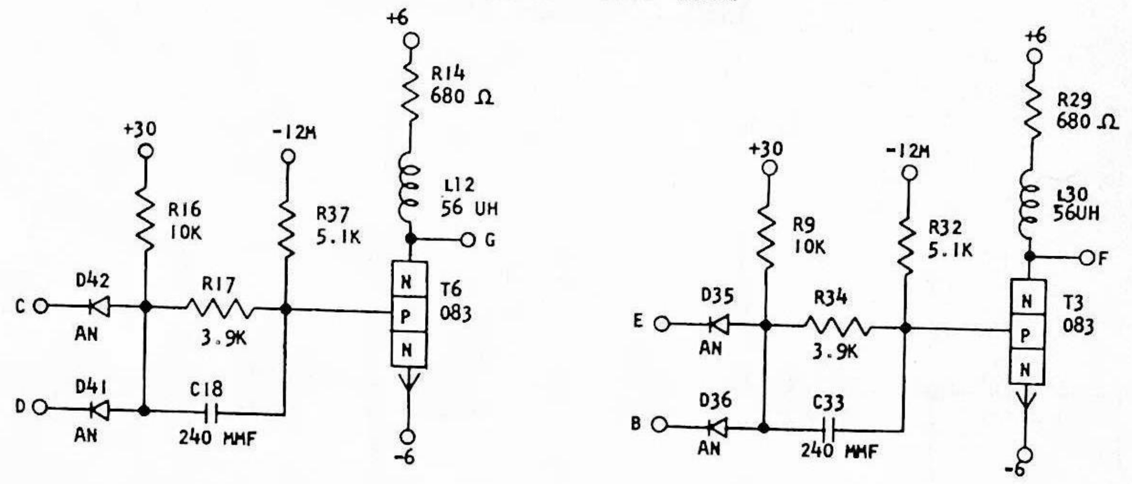
CARD CODE	729813
C A C -	

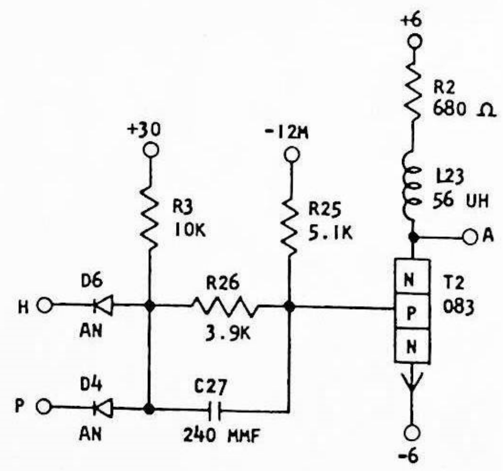
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371922

CTDL + AND GATE



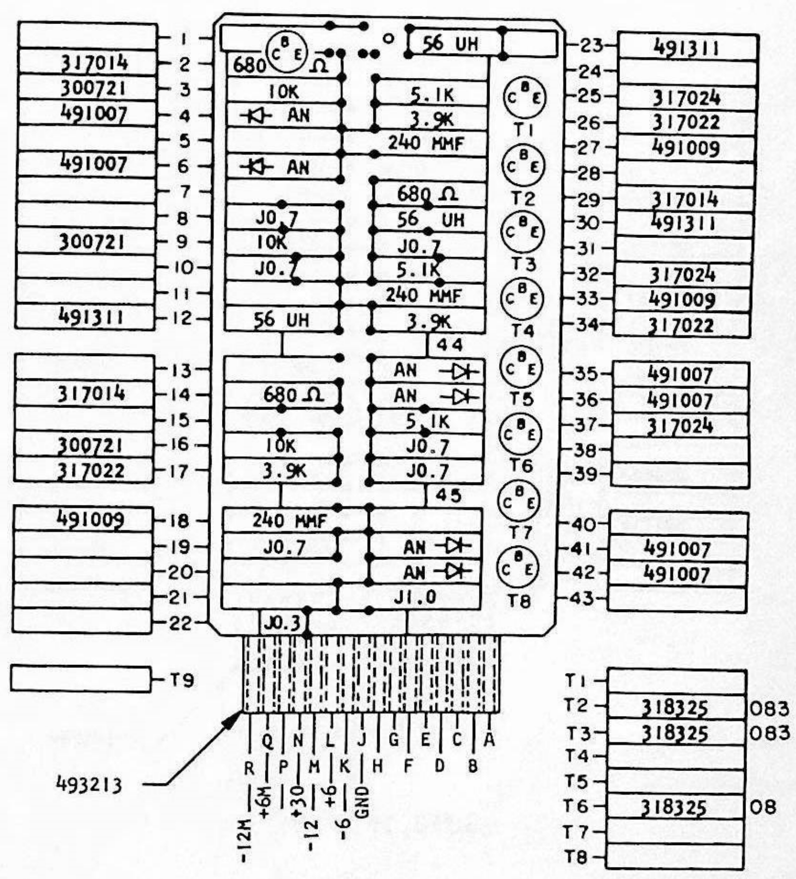




SEQUENCE OF OPERATION

1. ALL INPUTS UP TRANSISTOR ON OUTPUT DOWN
2. EITHER OR BOTH INPUTS DOWN TRANSISTOR OFF OUTPUT UP
3. DELAY WHEN DRIVING CTDL LOADS
   TURN ON .1 USEC MAX
   TURN OFF .25 USEC MAX
4. DELAY WHEN DRIVING CLOCK LOAD
   TURN ON .26 USEC MAX
   TURN OFF .12 USEC MAX

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
C,D H,P E,B	T	INPUTS		UP	+3.68	+6.24
				DOWN	-4.46	-6.24
G A F	T	OUTPUTS		UP	+1.44	+6.24
				DOWN	-4.62	-6.24



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL + AND GATE			6-27-62	115599					729813
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

C

STANDARDS CODE

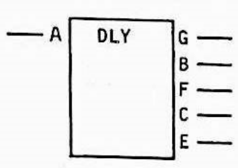
729814

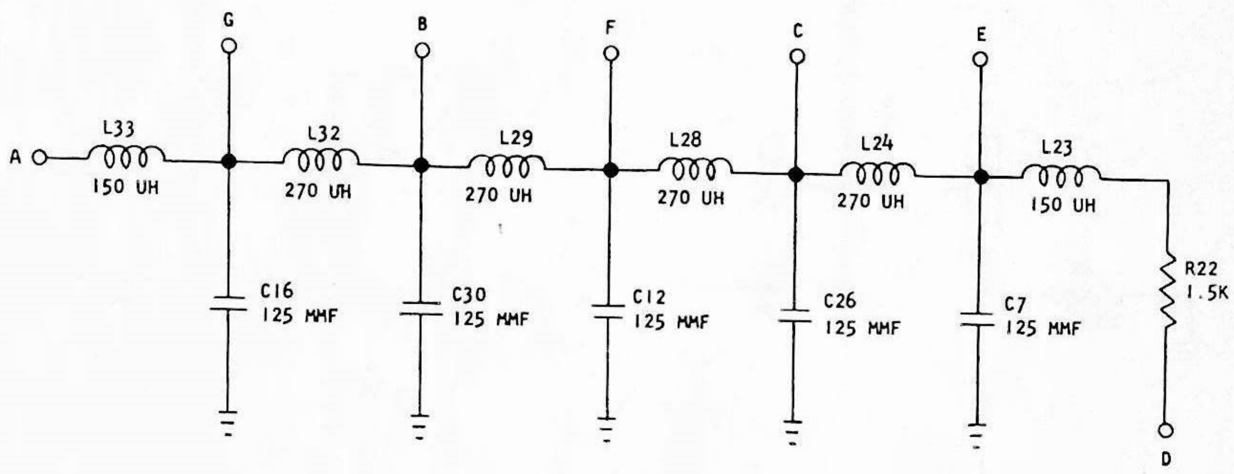
CARD CODE	729814
C E A -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371944

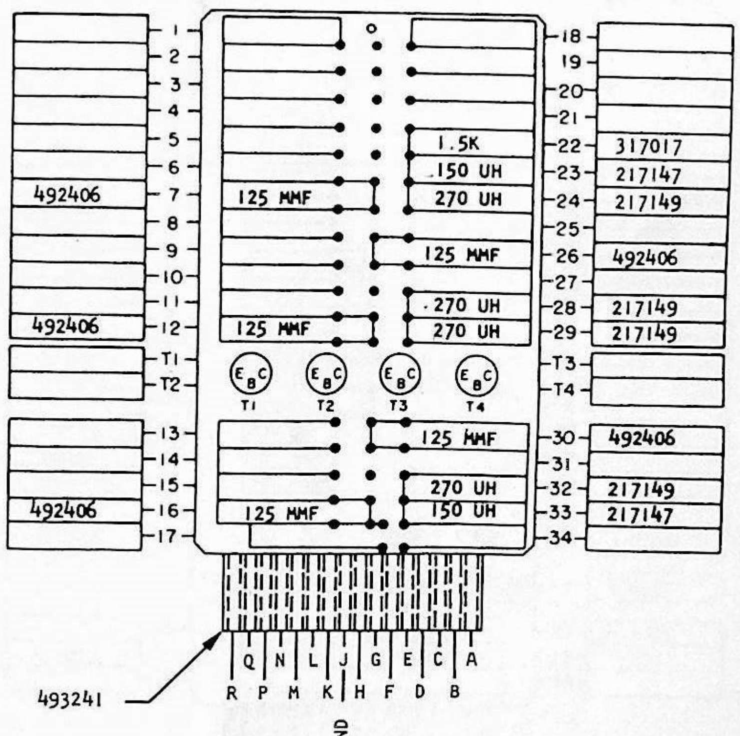
DELAY LINE LUMPED, 1 USEC





SEQUENCE OF OPERATION

1. INPUT UP, OUTPUT UP AFTER DELAY
2. DELAYS: G - 0.2 U SEC
   B - 0.4 U SEC
   F - 0.6 U SEC
   C - 0.8 U SEC
   E - 1.0 U SEC
3. TIE 1.5K RESISTOR (PIN D) TO -6 WHEN DRIVING MESA - AND GATE. TIE RESISTOR TO GROUND WHEN DRIVING + AND GATE



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A	T	INPUT		UP	+3.85	+6.24
				DOWN	-4.46	-6.24
G	T	OUTPUT		UP	+3.45	+5.82
				DOWN	-4.48	-6.24
B	T	OUTPUT		UP	+3.45	+5.82
				DOWN	-4.48	-6.24
F	T	OUTPUT		UP	+3.45	+5.82
				DOWN	-4.48	-6.24
C	T	OUTPUT		UP	+3.45	+5.82
				DOWN	-4.48	-6.24
E	T	OUTPUT		UP	+3.45	+5.82
				DOWN	-4.48	-6.24

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - DELAY LINE LUMPED, 1 USEC				1-27-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729814

C

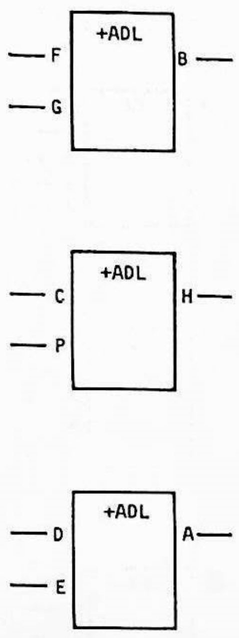
STANDARDS CODE
729901

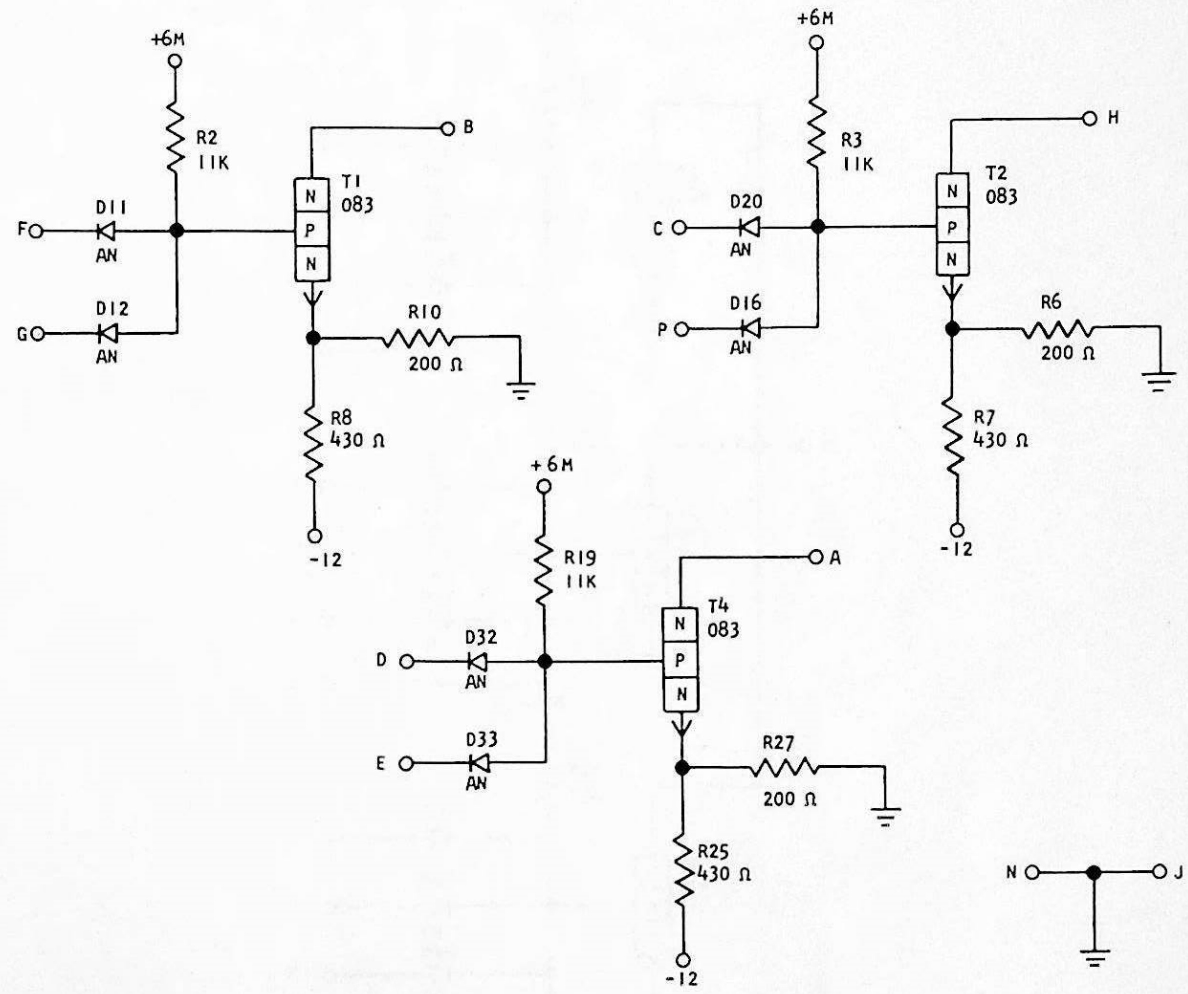
CARD CODE	729901
6J XD	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370089

CTDL STANDARD CABLE DRIVER

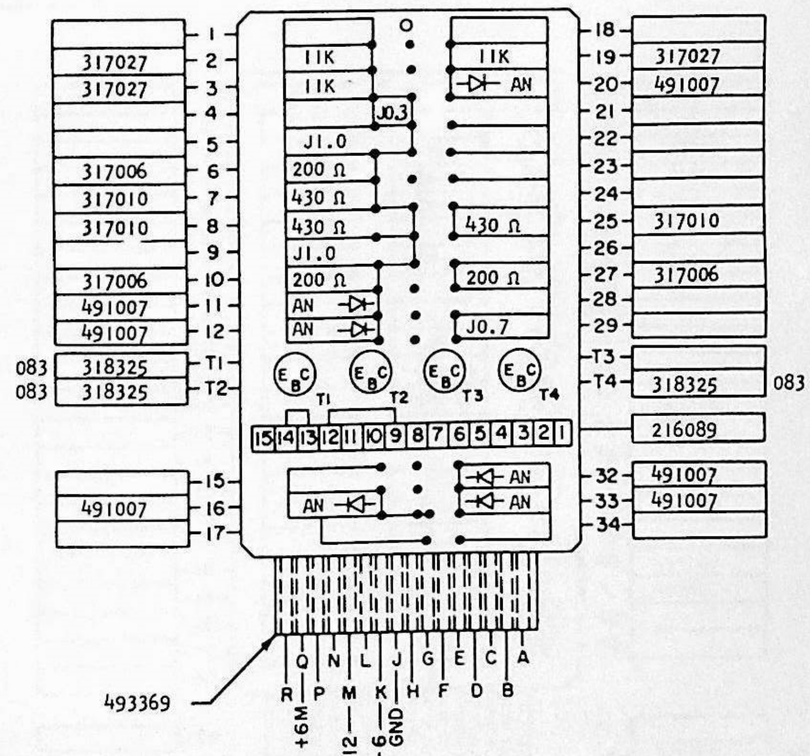




SEQUENCE OF OPERATION

1. ALL INPUTS UP TRANSISTOR ON OUTPUT DOWN
2. ANY INPUT DOWN TRANSISTOR OFF OUTPUT UP

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
F, C, D	U	INPUT		UP	-0.98	0.24
				DOWN	-7.44	-12.5
G, P, E	U	INPUT		UP	-0.98	0.24
				DOWN	-7.44	-12.5
B, H, A	N	OUTPUT		UP		
				DOWN	-1.25	-2.66
N, J		GROUND		UP		
				DOWN		



COMPONENT SIDE

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	455	652
TURN OFF	48	94

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL DRIVER			-62	115599					729901
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

C

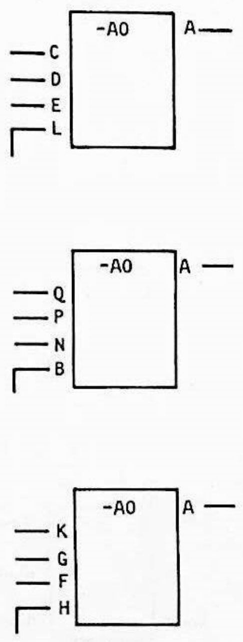
STANDARDS CODE

729816

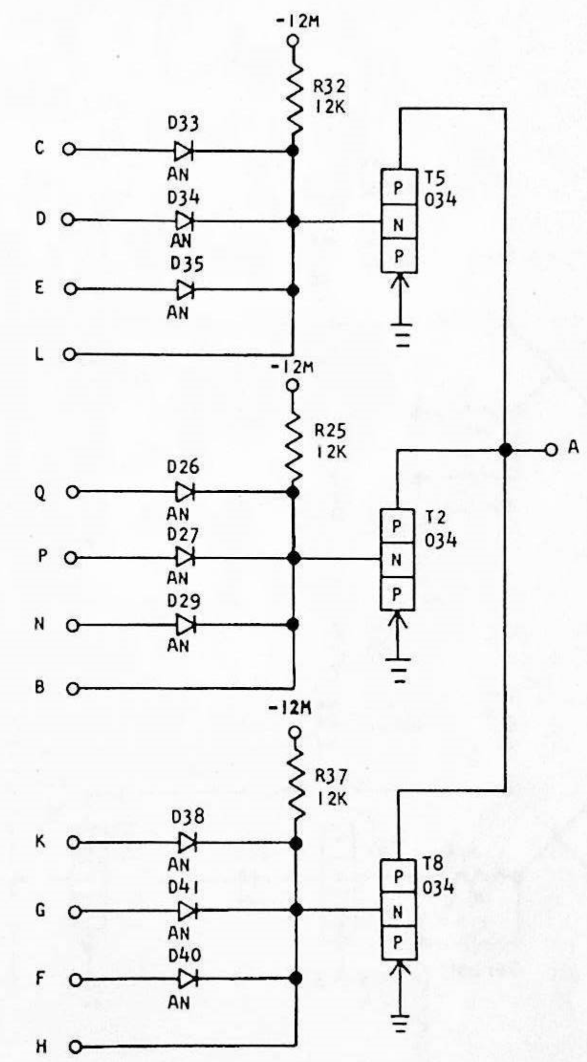
CARD CODE	729816
C E E -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370140



CTDL PNP-3 WAY AND GATE



SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTOR LOADING REQUIRED
4. INPUTS ON EXTENDER CARD MUST BE DOWN IN COINCIDENCE WITH INPUTS ON CARD FOR UP OUTPUT
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

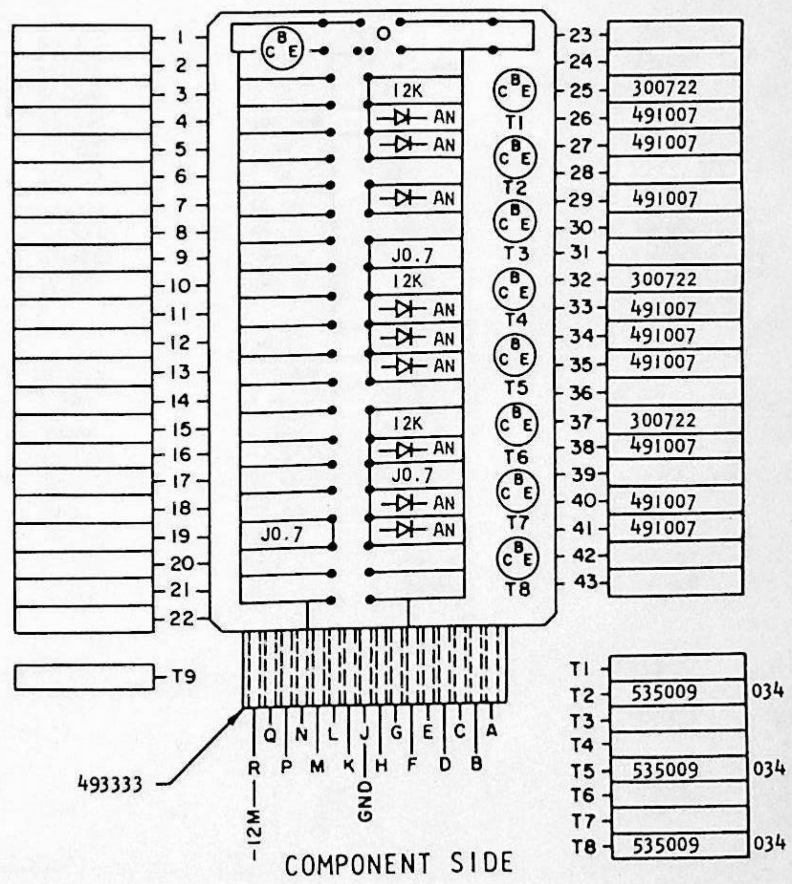
PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
C,D, E	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
Q,P, N	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
K,G, F	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
L,B, H		EXTENDER INPUT		UP	1.44	6.24
				DOWN	0	0
A	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR -CTDL PNP 3 WAY AND GATE				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6 -62	115599					

729816

C

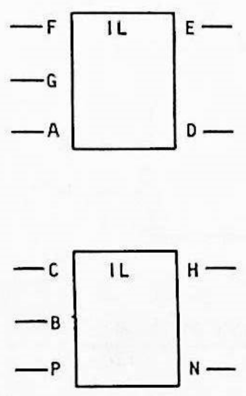
STANDARDS CODE

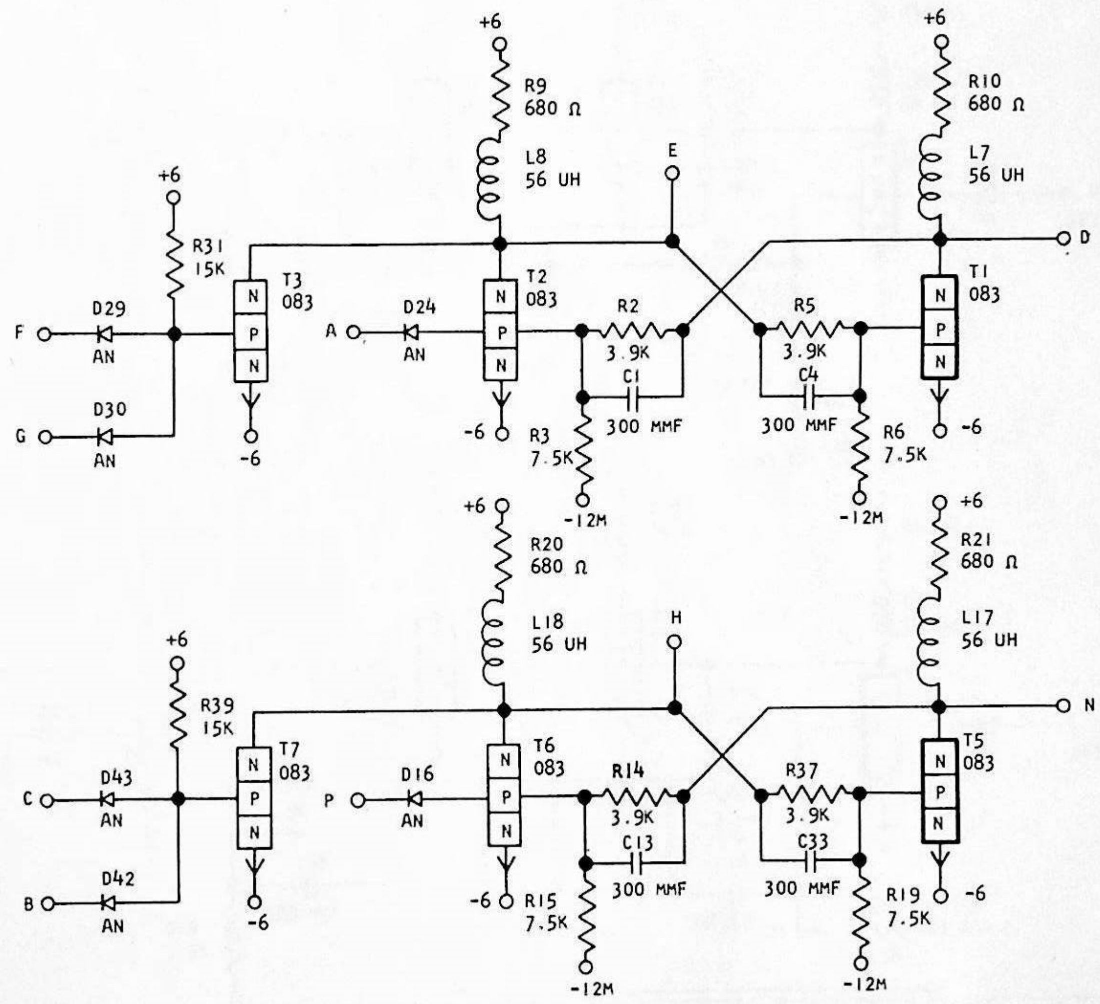
CARD CODE	729817
C E H -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370139

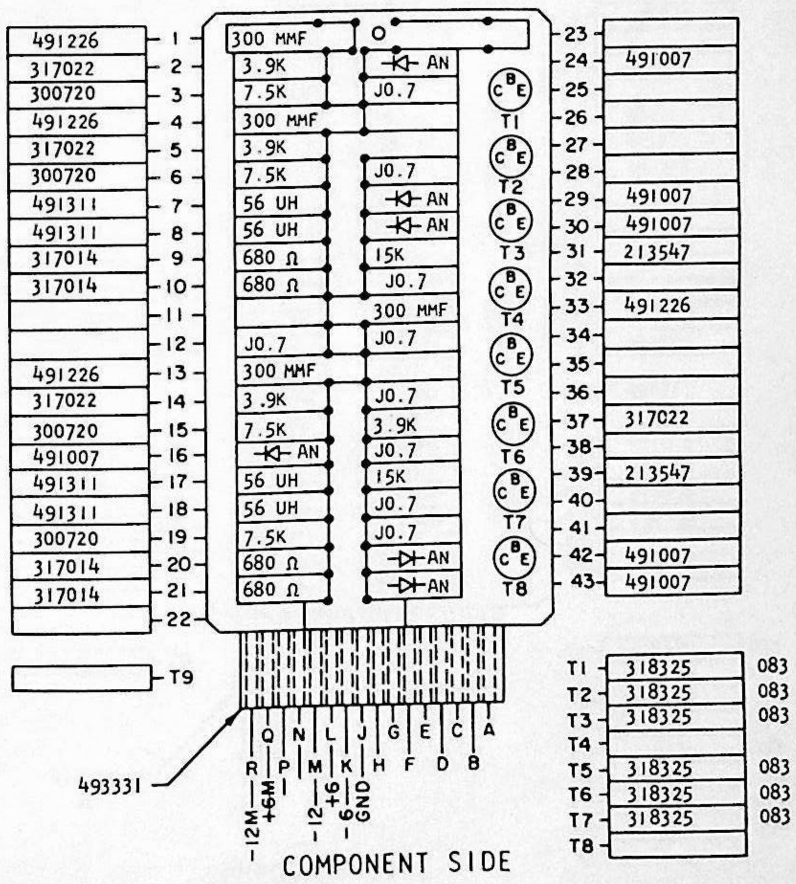
CTDL INVERTER LATCH NPN





SEQUENCE OF OPERATION

1. T1 ON, T2, T3 OFF
2. UP LEVEL AT F & G TURNS T3 ON, T1 OFF, T2 ON BY COLLECTIVE PULLOVER
3. DOWN LEVEL AT A WILL RETURN CIRCUIT TO CONDITION (1)



PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
F,G, C,B	U	SET		UP	-5.26	+.24
				DOWN	-7.44	-12.48
A,P	U	RESET		UP	-5.26	+.24
				DOWN	-7.44	-12.48
E,H	T	ON OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
D,N	T	OFF OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24

DELAY - SET

1. CONSIDER PIN D OR N AS OUTPUT
   TURN OFF 1.26 USEC MAXIMUM
   TURN ON 1.50 USEC
2. CONSIDER PIN E OR H AS OUTPUT
   TURN OFF 1.66 USEC MAXIMUM
   TURN ON .86 USEC MAXIMUM

RESET

1.. PIN D OR N AS OUTPUT
   TURN OFF 0.45
   TURN ON 0.45
2. PIN E OR H AS OUTPUT
   TURN OFF 0.40
   TURN ON 0

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL				6 ?? -62	·115599					
	INVERTER LATCH NPN										
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729817

FORM 88-001

C

STANDARDS CODE

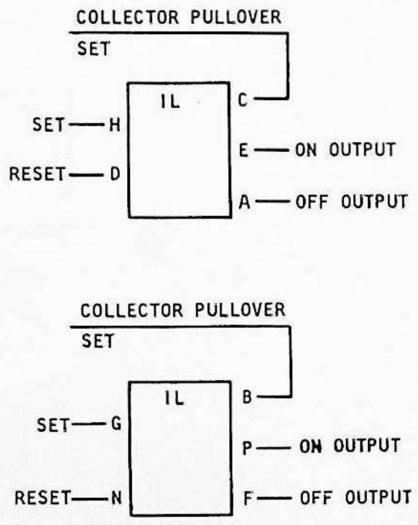
729818

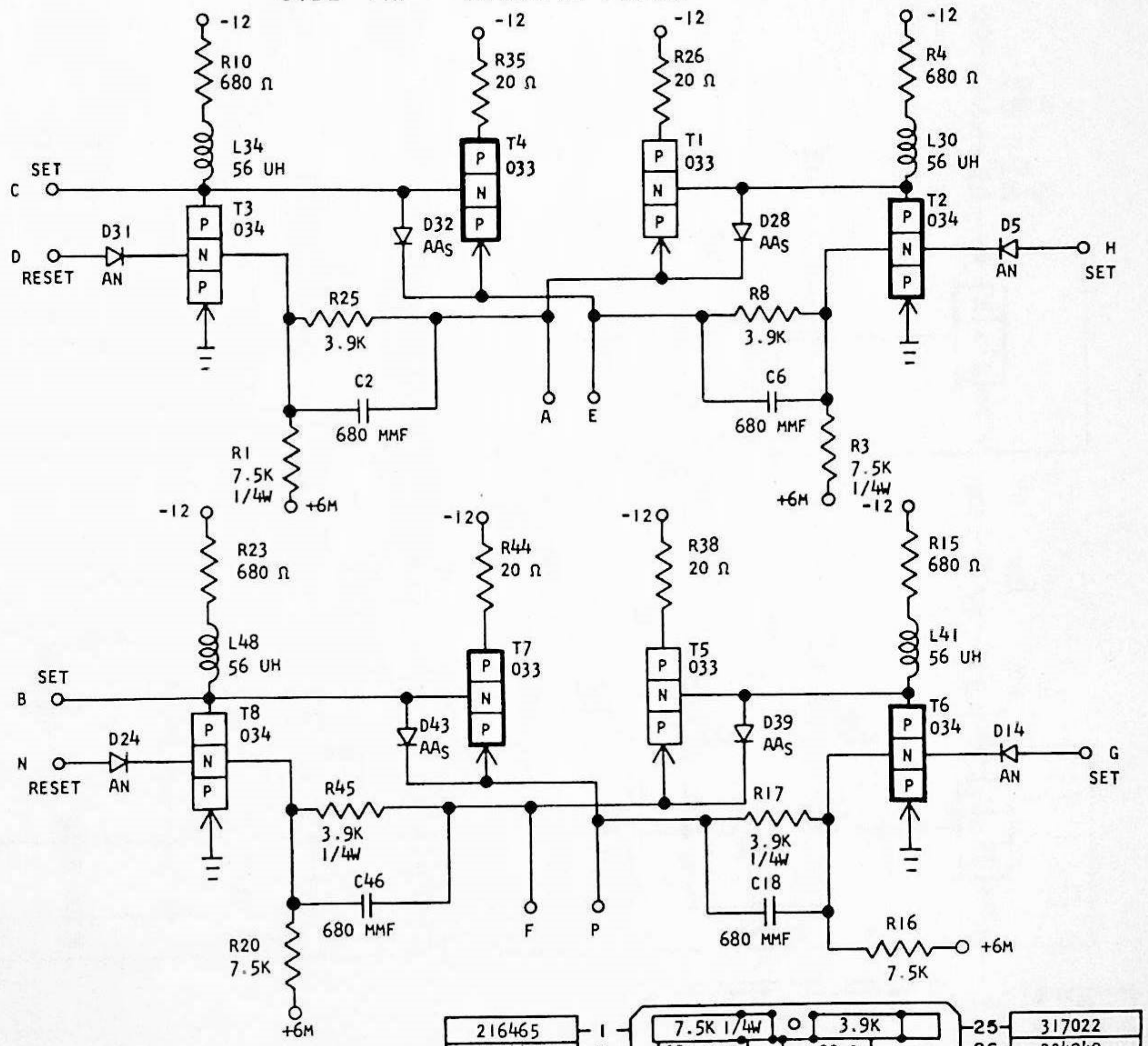
CARD CODE	729818
CEK-	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370143

CTDL PNP - INVERTER LATCH



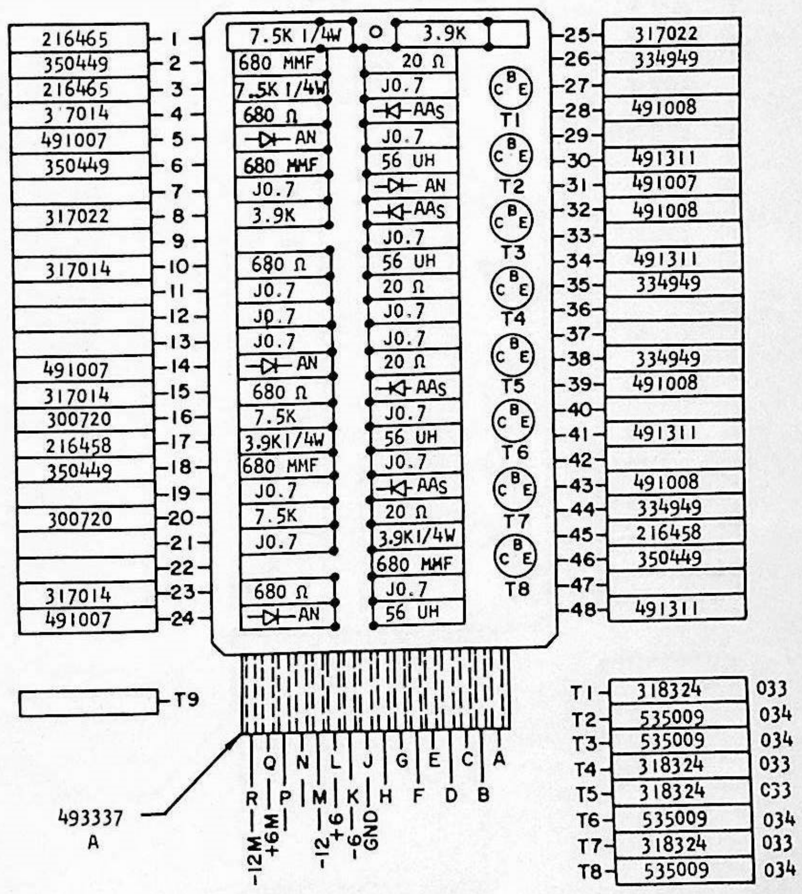


SEQUENCE OF OPERATION

1. T2 & T4 ON T1 & T3 OFF
2. 0V SET AT H OR C TURNS T2 OFF AND T1 ON T3 TURNS ON AND T4 TURNS OFF
3. 6V RESET AT D RETURNS CIRCUIT TO CONDITION (1)

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
G,H	T	SET		UP	1.44	6.24
				DOWN	-5.46	-6.24
D,N	T	RESET		UP	1.44	6.24
				DOWN	-5.46	-6.24
E,P	U	ON OUTPUT		UP	-1.24	.24
				DOWN	-9.29	-12.48
A,F	U	OFF OUTPUT		UP	-1.24	.24
				DOWN	-9.29	-12.48
B,C	U	COLLECTOR PULLOVER SET		UP	-.54	.24
				DOWN	-7.44	-12.48

DELAY
1. SET AND RESET DELAY:
TURN ON -.15 USEC FOR SET TO OUTPUT AT OFFSIDE (PIN A, F) AND FOR RESET TO OUTPUT OF ONSIDE (PIN E, P).
2. TURN ON .40 USEC FOR SET TO OUTPUT AT ONSIDE (PIN E, P) AND FOR RESET TO OUTPUT OF OFFSIDE (PIN A, F).



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL-PNP					6- -62	115599					
	INVERTER LATCH											
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729818

C

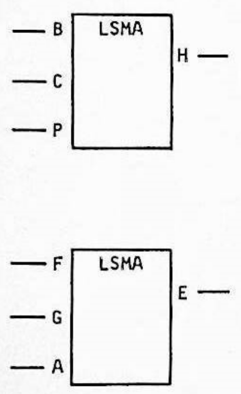
STANDARDS CODE	

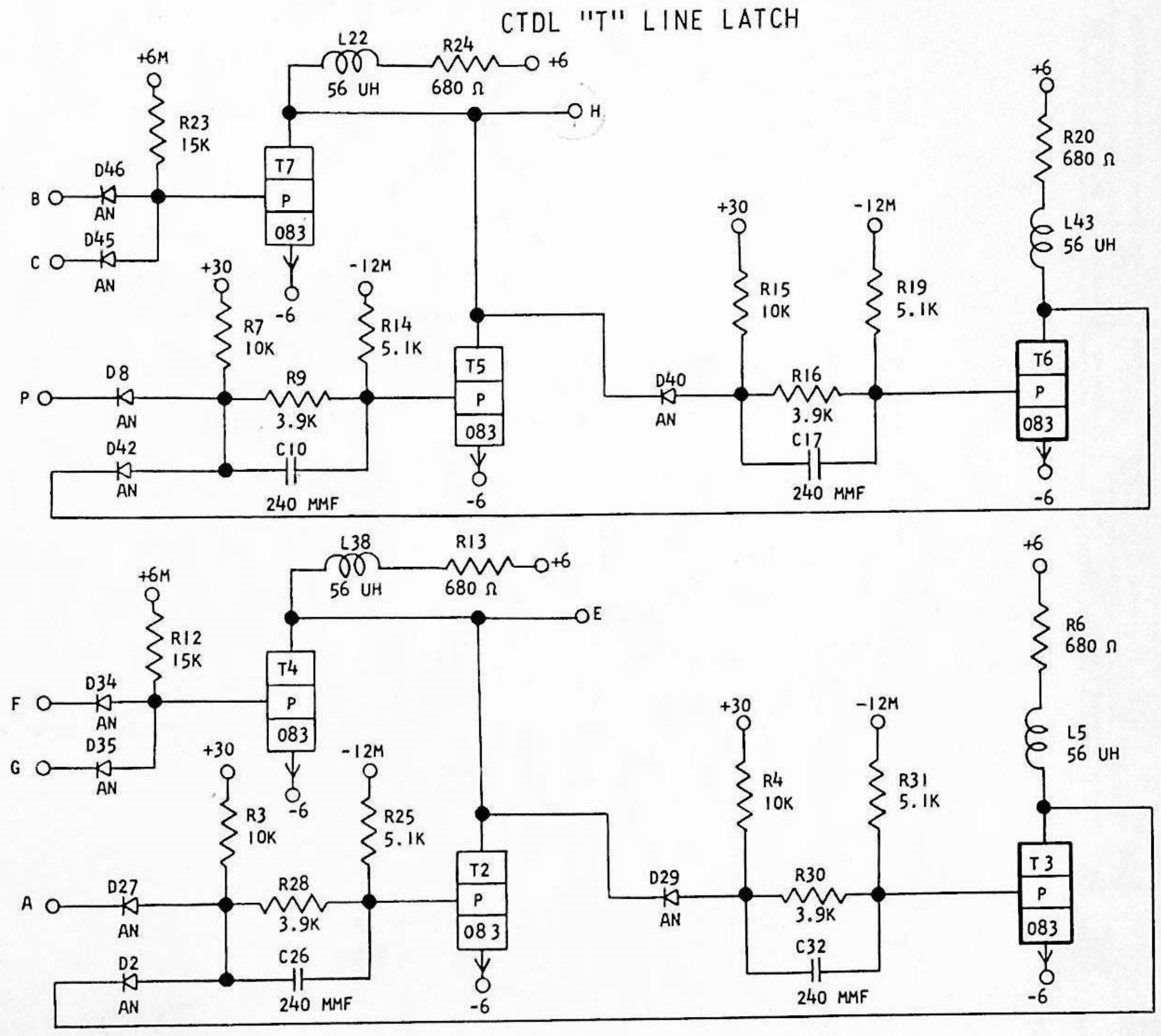
729819

CARD CODE	729819
C E M -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370357





SEQUENCE OF OPERATION

1. T6 IS ON, T5, T7 OFF
2. WHEN B & C ARE UP; T7 TURNS ON, THE OUTPUT IS DOWN, T6 TURNS OFF, T5 TURNS ON
3. WHEN P IS DOWN, T5 IS OFF, THE OUTPUT IS UP, T6 TURNS ON

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B,C	U	SET		UP	-5.26	.24
				DOWN	-7.44	-12.48
H	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
P	T	RESET		UP	3.68	6.24
				DOWN	-4.46	-6.24
F,G	U	SET		UP	-5.26	.24
				DOWN	-7.44	-12.48
E	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
A	T	RESET		UP	3.68	6.24
				DOWN	-4.46	-6.24

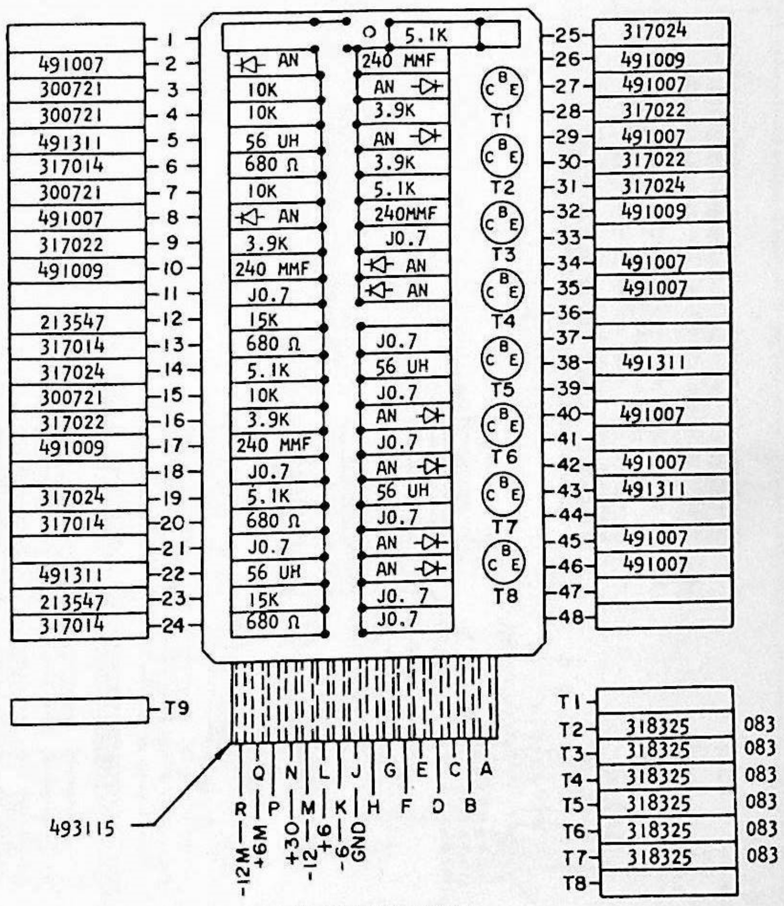
DELAY - USEC

1. SET TO OUTPUT

	MIN.	MAX
TURN ON	0.05	0.70
TURN OFF	0.05	1.50

2. RESET TO OUTPUT:

TURN ON	----	.08
TURN OFF	----	.23



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL "T" LINE LATCH				/ -62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729819

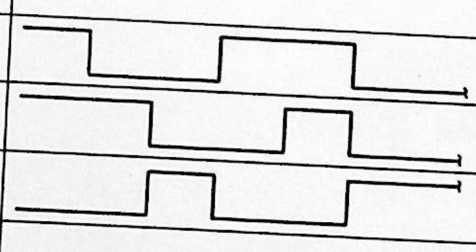
FORM 88-001

C

CG

SEQUENCE OF OPERATION

1. BOTH INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. EXTERNAL COLLECTOR LOADING REQUIRED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B,F,D	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C,G,E	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
H,N,A	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

CARD CODE	STANDARDS CODE	370975
CG **	2-7049	

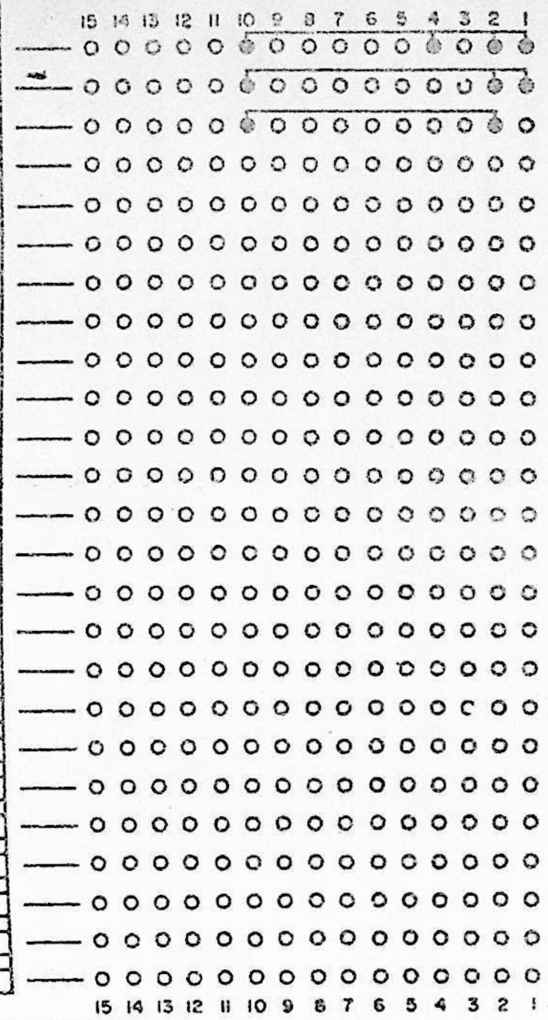
CTDL TWO WAY AND PNP

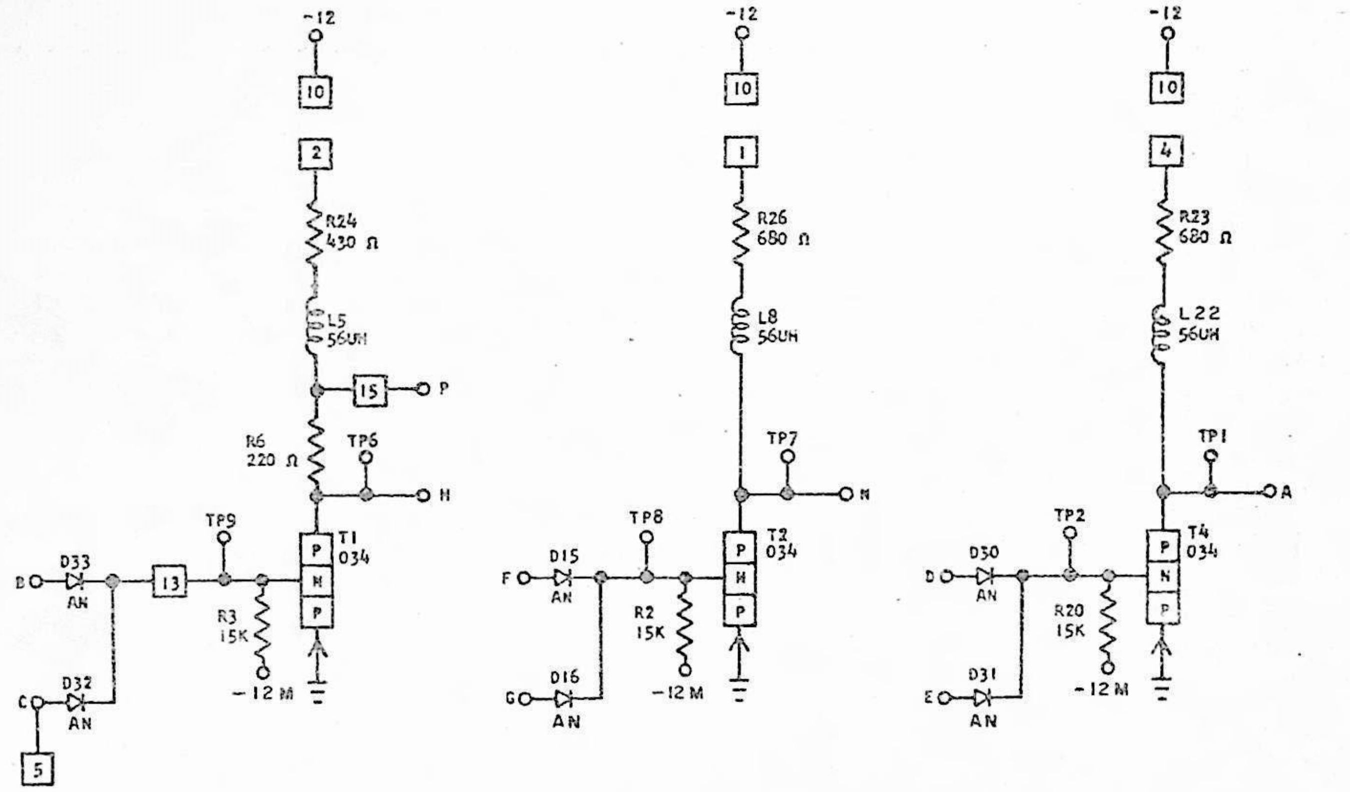
FIELD REPLACEMENT

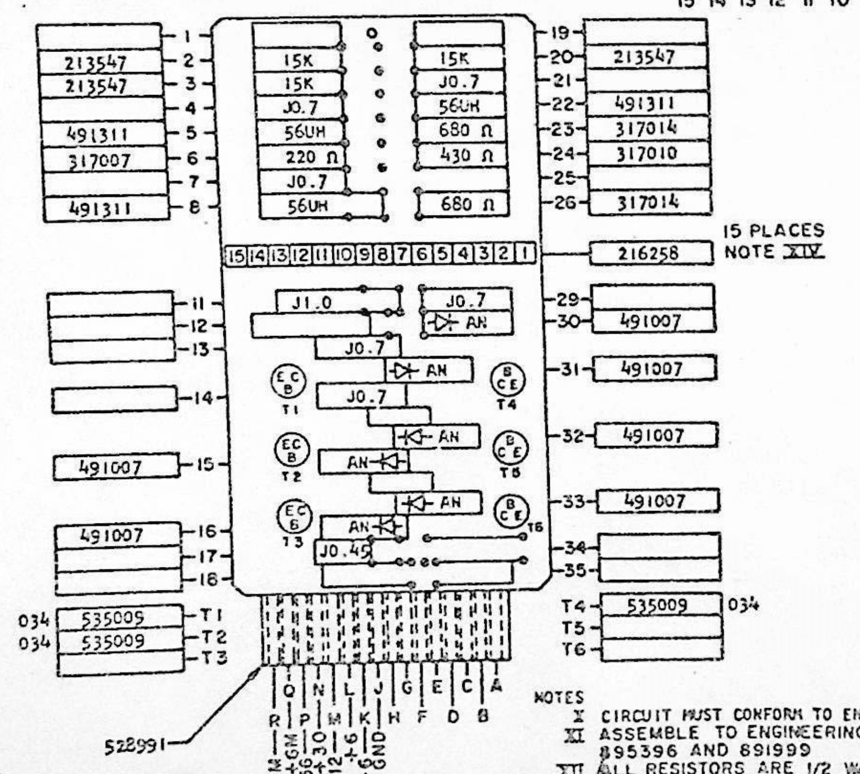
DISCONTINUED

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC
CTDL 2 WAY AND PNP	WW	371251	891071
CTDL 2 WAY AND PNP-TWO LOADS	VW	371261	891071
CTDL 2 WAY AND PNP-ONE LOAD	VV	371262	891071
CTDL 2 WAY AND PNP-NO LOAD	—	371263	891071

CAP CONFIGURATION







NOTES
- I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891071
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
- XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED
- XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491296
- XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H. D. Hanford	7-6-60

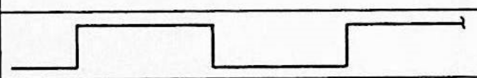
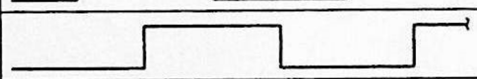
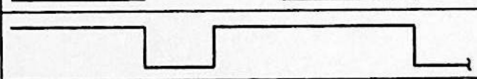
370975

INTERNATIONAL BUSINESS MACHINES CORP.			DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL TWO WAY AND PNP		8-4-60	109542	DWB				X0668
DESIGN		TYPE SMS	11-4-60	D109900	IWB				
DETAIL		SCALE NONE	12-1-60	110517	IWB				
CHECK	TBJ 8-1-60	DRAW HDE 7-7-60							
APPRO	RES 8-3-60	CHECK 95 7/13/60							

370975

SEQUENCE OF OPERATION

1. BOTH INPUTS UP, TRANSISTOR ON, OUTPUT DOWN
2. ANY INPUT DOWN, TRANSISTOR OFF, OUTPUT UP
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
B,F,D	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
C,G,E	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
H,N,A	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.70
TURN OFF	0.05	1.50*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

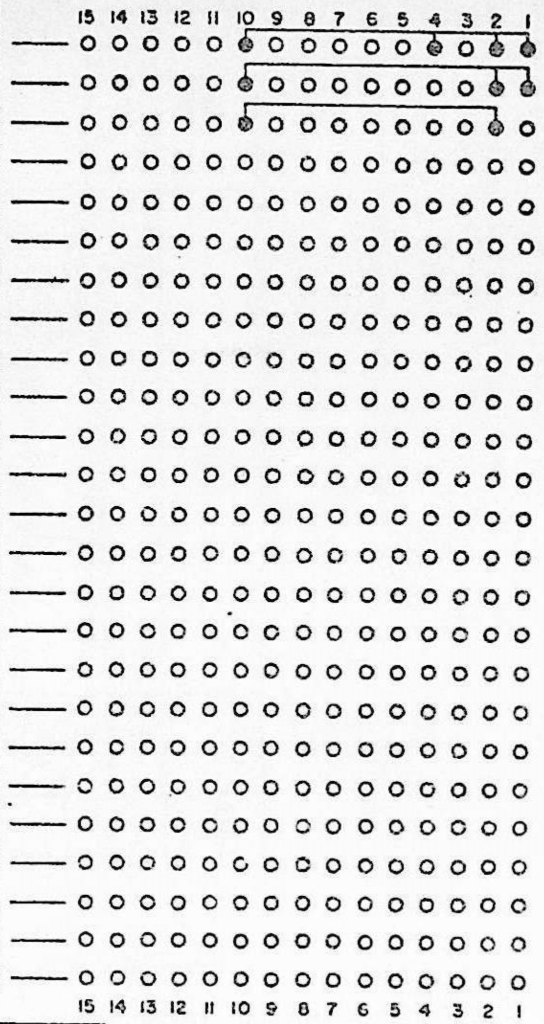
CARD CODE	STANDARDS CODE	370976
CH **	2-7045	

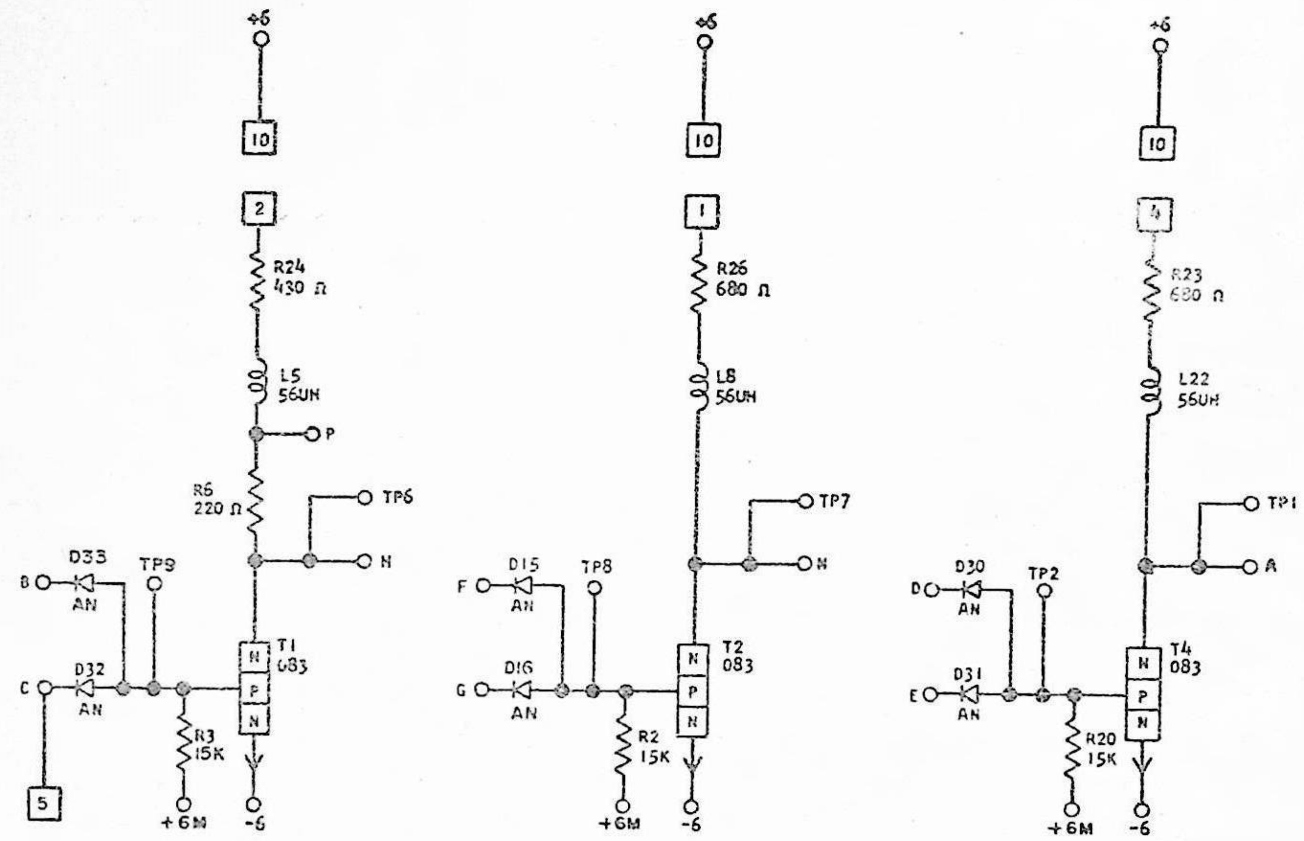
CTDL TWO WAY AND NPN
FIELD REPLACEMENT

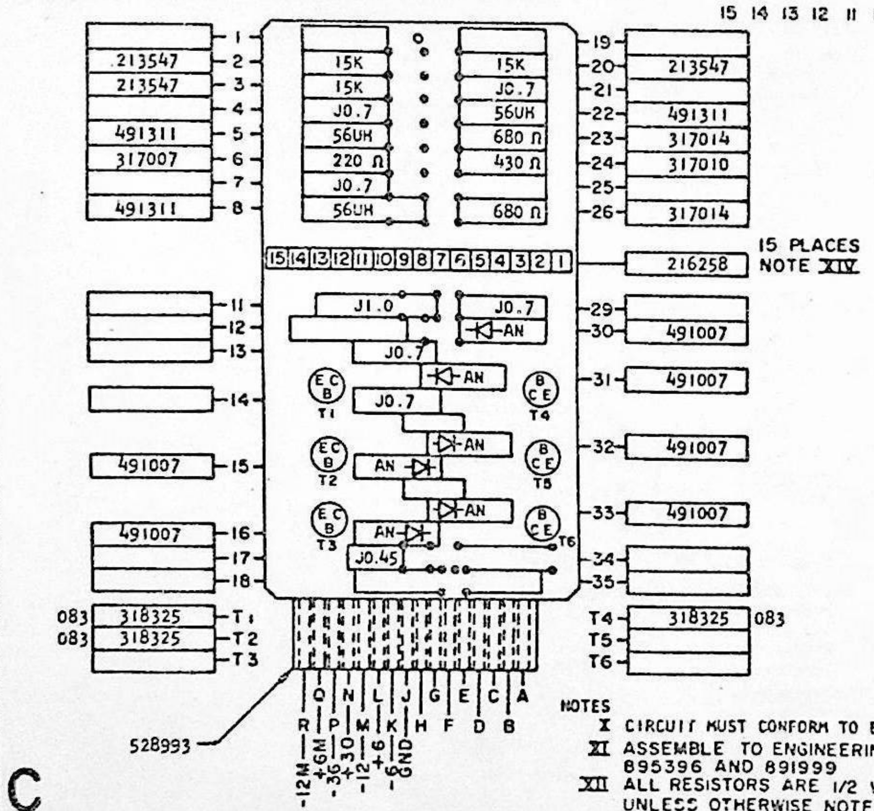
DISCONTINUED

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC
CTDL-TWO WAY AND NPN	WW	371252	891071
CTDL-TWO WAY AND NPN-TWO LOADS	VW	371264	891071
CTDL-TWO WAY AND NPN-ONE LOAD	VV	371265	891071
CTDL-TWO WAY AND NPN-NO LOADS	—	371266	891071

CAP CONFIGURATION







NOTES

I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891071

XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999

XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED

XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491296

XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H D Harford	7-6-60

370976

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-CTDL				
	TWO WAY AND NPN				
DESIGN			TYPE	SMS	
DETAIL			SCALE	NONE	
CHECK	TBJ	8-1-60	DRAW	MDE	7-7-60
APPRO	BES	8-3-60	CHECK		7-12-60

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
8-4-60	109642	JWB				X0667
9-30-60	D110081	IWB				
10-26-60	D110160					
12-1-60	110517	IWB				

370976

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP

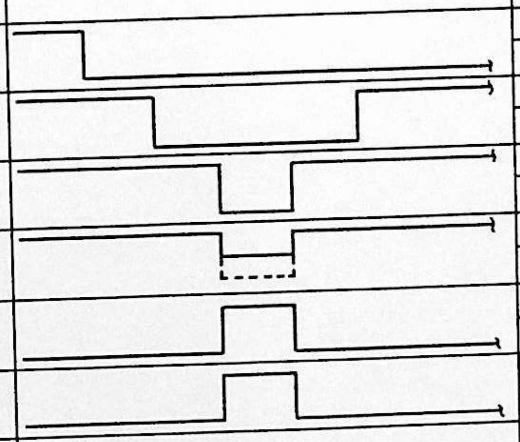
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN

3. INPUTS ON EXTENDER CARD DOWN IN COINCIDENCE WITH DOWN INPUTS ON CARD FOR UP OUTPUT

4. TI COLLECTOR MUST BE LOADED

5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
D, A	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
E, B	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
F, C	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
G		EXTENDER INPUT		UP	+6.0	
				DOWN	0.0	
H, N	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5
P	P	OUTPUT		UP	-4.93	-3.54
				DOWN	-8.82	-12.5



DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCK.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

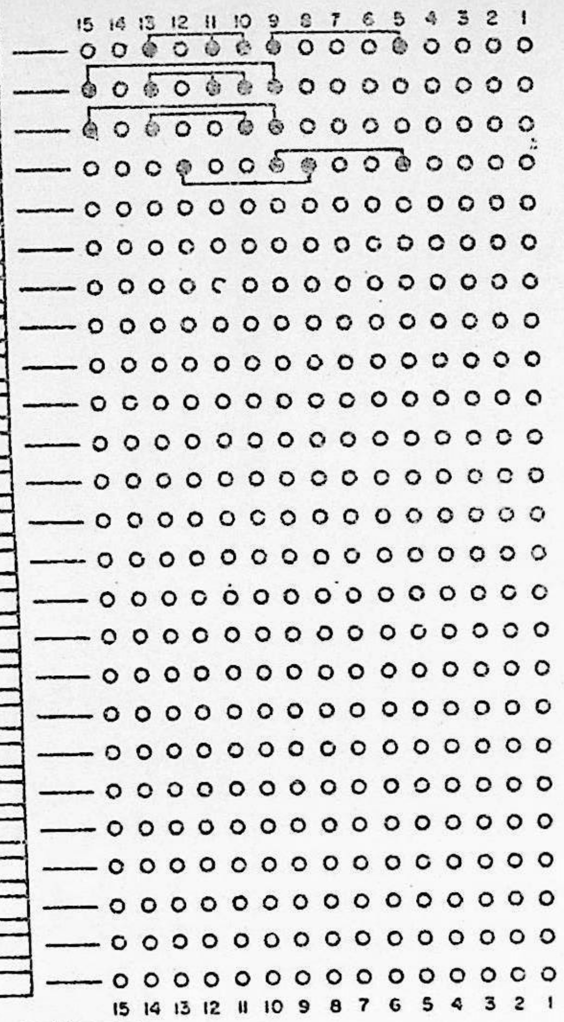
CARD CODE	STANDARDS CODE	370977
CJ **	2-7045	

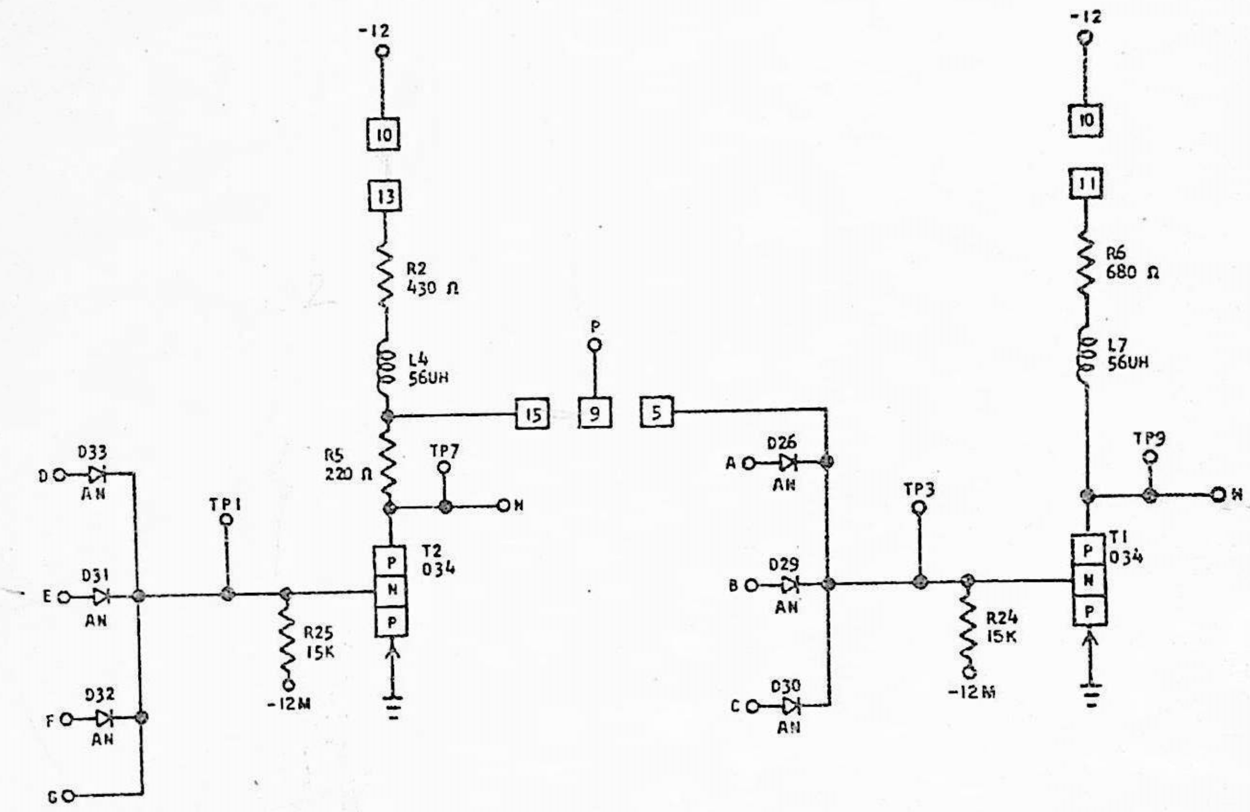
CTDL 3 WAY AND PNP FIELD REPLACEMENT

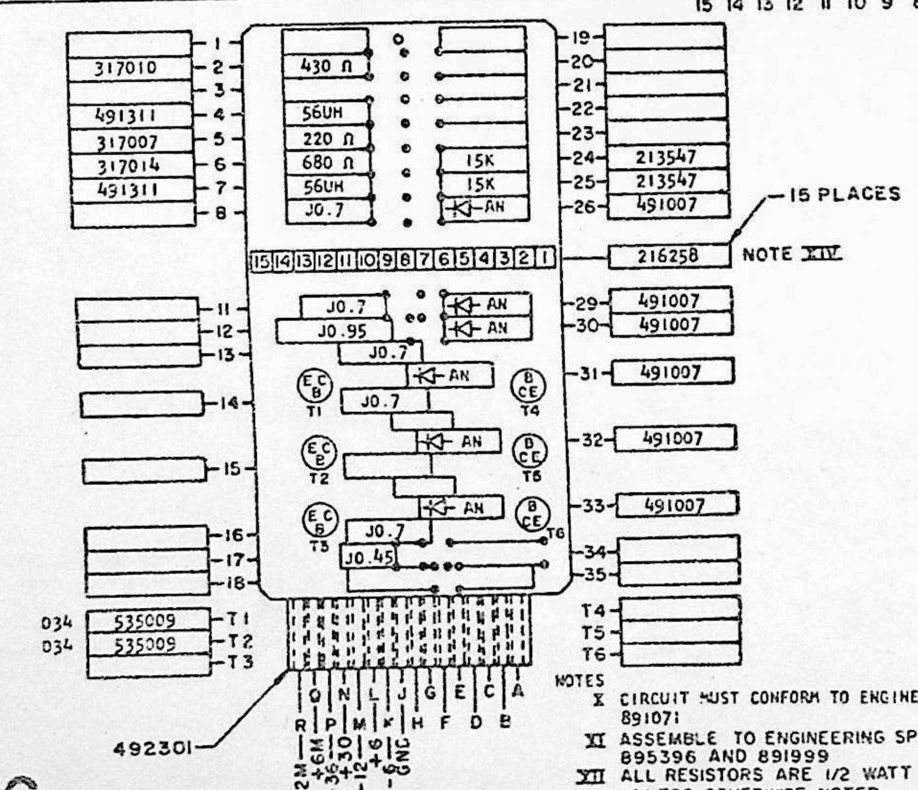
DISCONTINUED

CAP CONFIGURATION

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC
CTDL 3 WAY AND EXTENDED INPUTS	YC	371071	891071
CTDL 3 WAY AND PNP	WV	371253	891071
CTDL 3 WAY AND PNP-1 LOAD	VU	371267	891071
CTDL 3 WAY AND PNP-NO LOAD	WF	371268	891071







NOTES

X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891071

XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999

XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED

XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491296

XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H E Harty	7-6-60

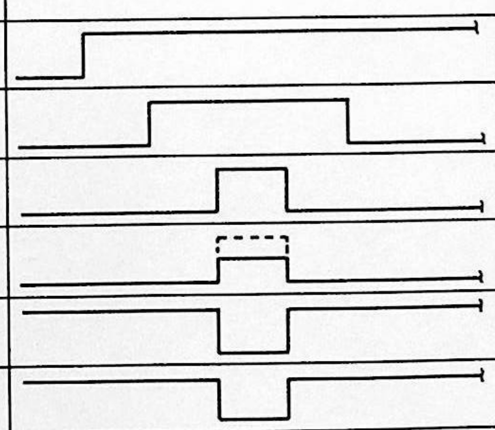
370977

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL				8-4-60	105642					X0669
3 WAY AND PNP					9-30-60	D110081	IWB				
DESIGN		TYPE	SMS		12-14-60	110166	IWB				
DETAIL		SCALE	NONE								
CHECK	TGJ 8-1-60	DRAWN	HOE 7-8-60								
APPRD	BSS 8-3-60	CHECK	7-13-60								

370977

SEQUENCE OF OPERATION

1. ALL INPUTS UP TRANSISTOR ON OUTPUT DOWN
2. ANY INPUT DOWN TRANSISTOR OFF OUTPUT UP
3. INPUTS ON EXTENDER CARD UP IN COINCIDENCE WITH UP INPUTS CARD FOR DOWN OUTPUT
4. TI COLLECTOR MUST BE LOADED
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
D,A	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
E,B	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
F,C	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
G		EXTENDER INPUT		UP	-6.	
				DOWN	-12.	
N,H	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
P	N	OUTPUT		UP	2.82	6.24
				DOWN	-1.07	-2.40

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.70
TURN OFF	0.05	1.50*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

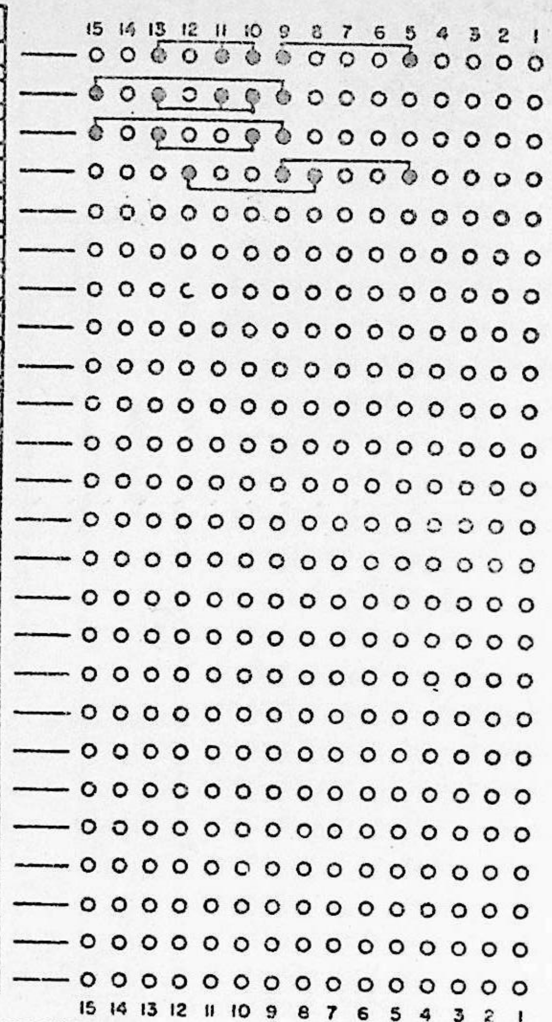
CARD CODE	STANDARDS CODE	370978
CK **	2-7045	

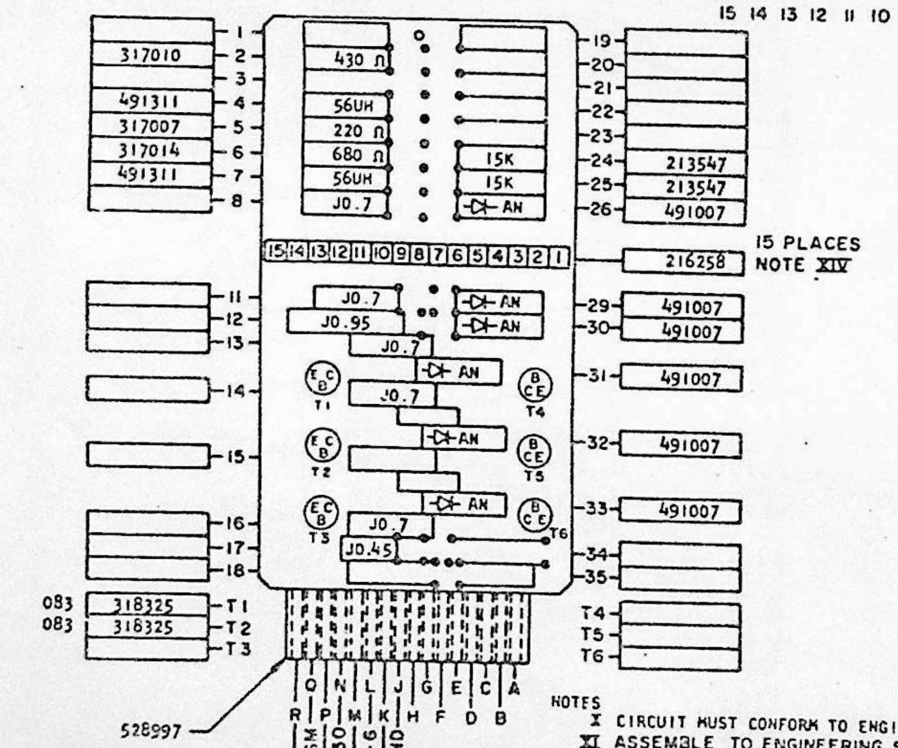
CTDL 3 WAY AND NPN
FIELD REPLACEMENT

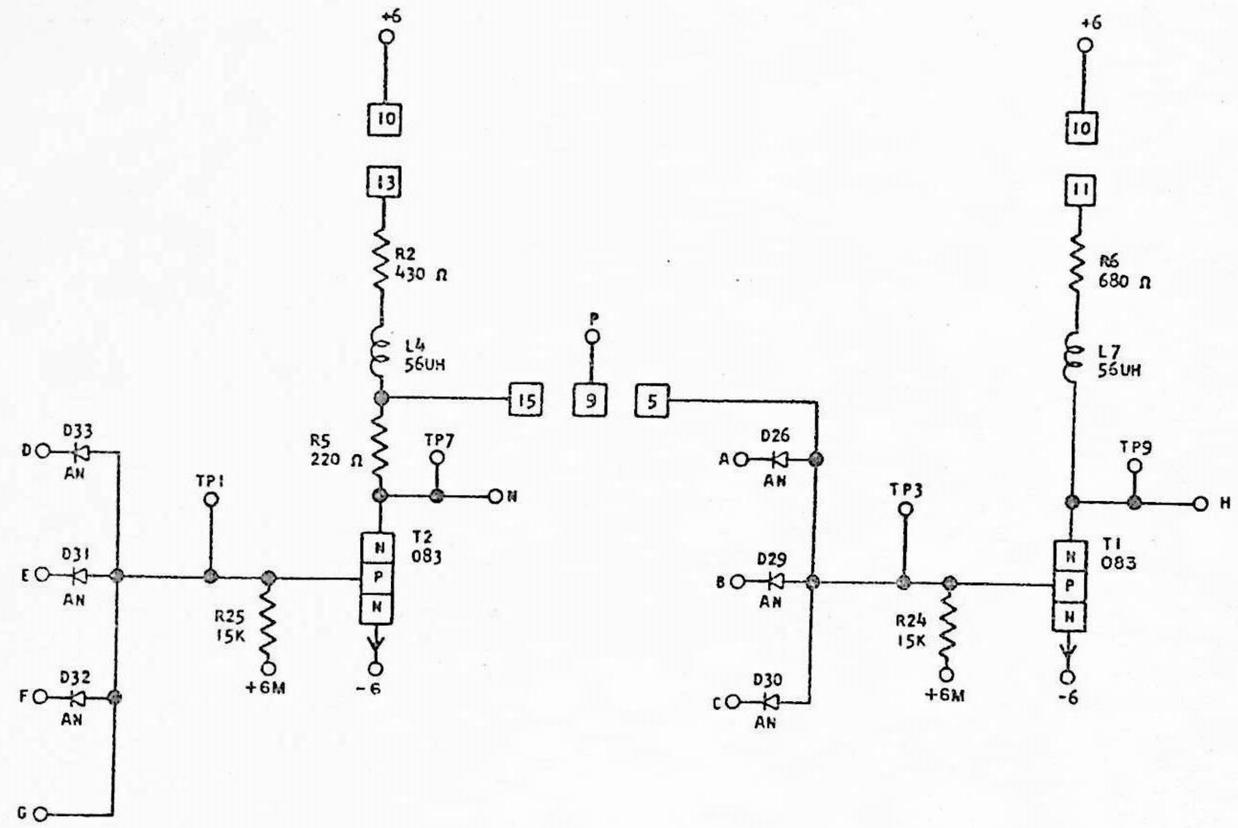
DISCONTINUED

CAP CONFIGURATION

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC
CTDL 3 WAY AND NPN EXTENDED INPUT	YC	371072	891071
CTDL 3 WAY AND NPN	WV	371254	891071
CTDL 3 WAY AND NPN-1 LOAD	VU	371269	891071
CTDL 3 WAY AND NPN-NO LOAD	WF	371270	891071







NOTES
I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891071
XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED
XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491296
XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H D Hanford	7-6-60

370978

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL 3 WAY AND NPN			F 4 60	103642	QWB				X0662
DESIGN		TYPE	SMS	9-30-60	D110081	IWB				
DETAIL		SCALE	NONE	11-23-60	110190	IWB				
CHECK	TRJ 8-1-60	DRAW	MDE 7-11-60							
APPROVED	GGS 8-3-60	CHECK	2-13-61							

370978

5

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
B	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
D	T	EXTENDER OUTPUT		UP	+6	
				DOWN	0.0	
E	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
F	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
G	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
H	U	EXTENDER OUTPUT		UP	-6	
				DOWN	-12	

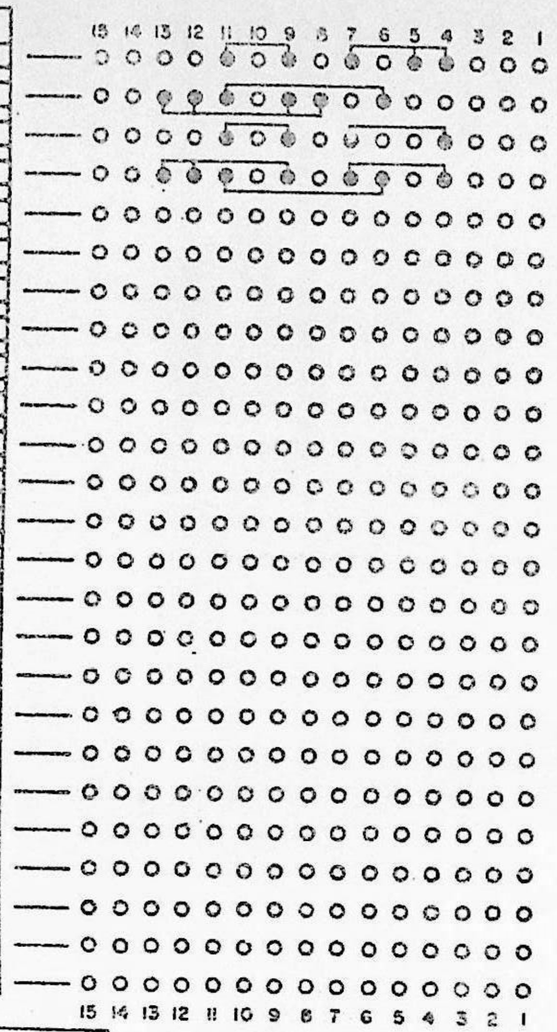
CARD CODE	STANDARDS CODE	370979
CL **	2-7045	

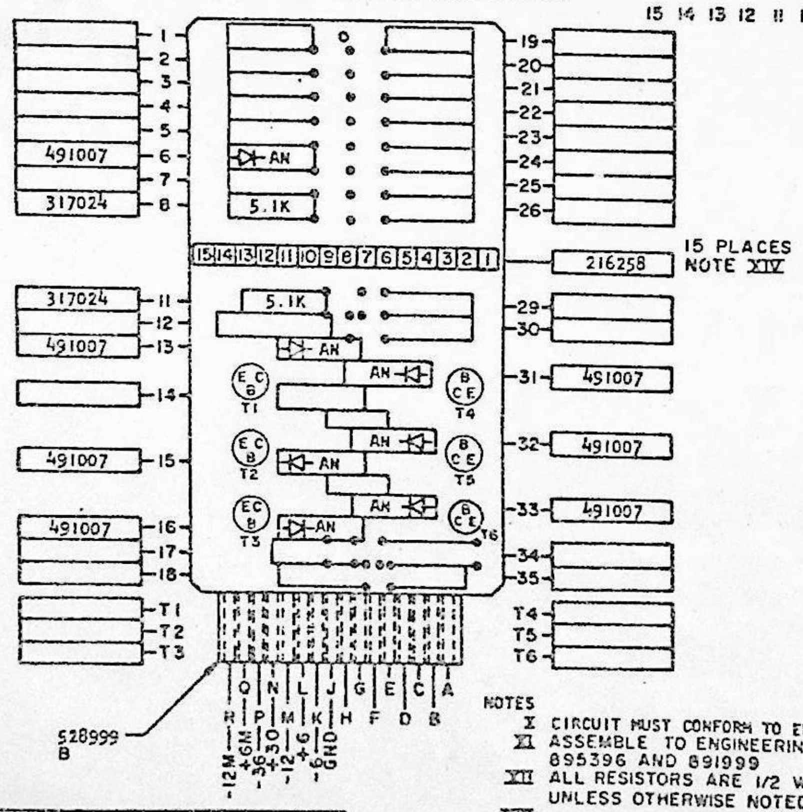
DISCONTINUED

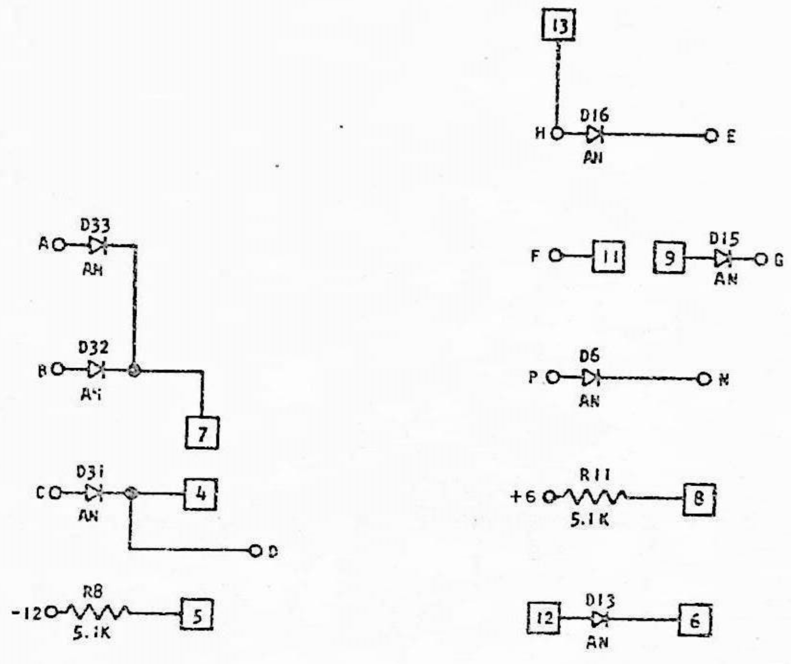
CTDL EXTENDER CARD
FIELD REPLACEMENT

CAP CONFIGURATION

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC
CTDL +P OR EXTENDED CARD	VT	371073	
CTDL -N OR EXTENDED CARD	VS	371074	
CTDL EXTENDED CARD	VR	371075	
CTDL EXTENDED CARD	VQ	371255	891071







C

NOTES
I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891071
XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED
XIII
XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H. D Hanford	7-6-60

370979

INTERNATIONAL BUSINESS MACHINES CORP				
NAME	CARD ASM TSTR-CTDL			
	EXTENDER CARD			
DESIGN		TYPE	SMS	
DETAIL		SCALE	NONE	
CHECK	TEJ 8-1-60	DRAWN	HDE	7-8-60
APPROVED	DES 8-3-60	CHECKED		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL
8-4-60	109642	JWB			
11-4-60	D109900	IWB			
12-1-60	110517	IWB			
2-13-61	D111072	IWB			

DEVELOPMENT NO.
X0661

370979

STANDARDS CODE

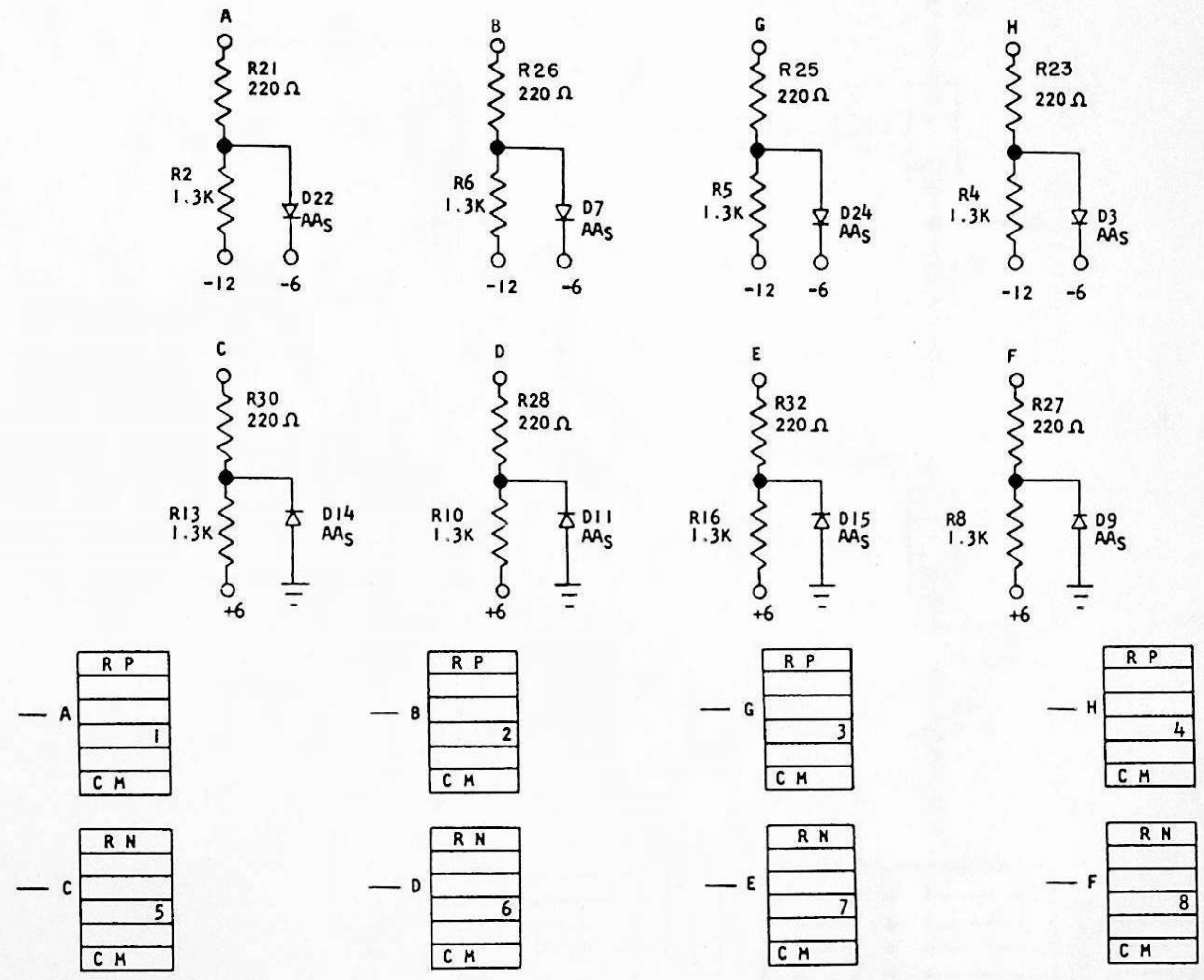
729840

CARD CODE	729840
CM --	

REFERENCE DRAWING

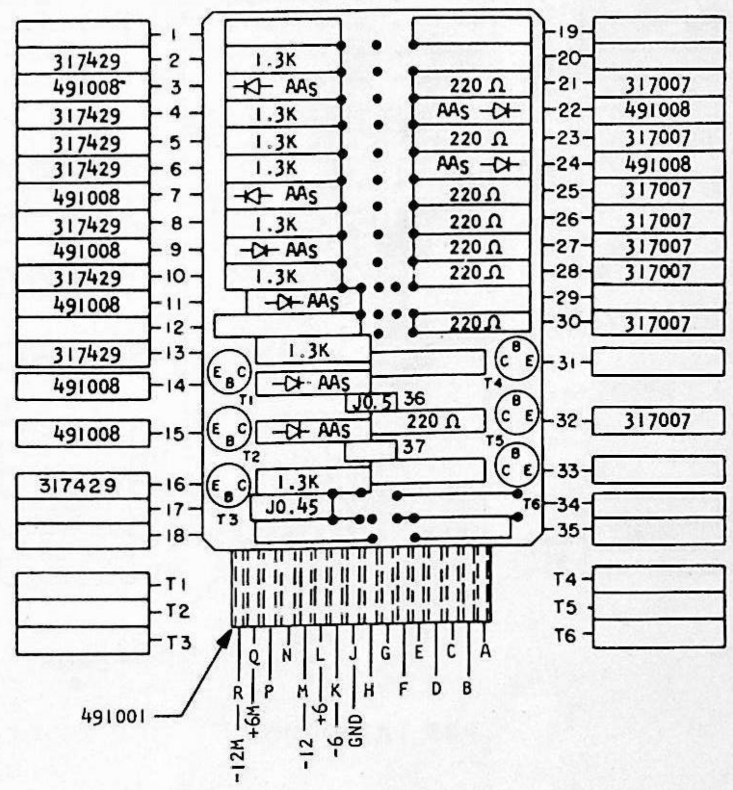
SEE PRODUCTION DRAWING 371256

CTDL - COUPLING NETWORK



SEQUENCE OF OPERATION

1. COLLECTOR LOADING FOR CURRENT MODE LOGIC BLOCKS
2. A, B, G, H, PROVIDE P LEVEL OUTPUTS; C, D, E, F, PROVIDE N LEVEL OUTPUTS
3. FOR DELAY DATA REFER TO THE GENERAL INFORMATION ON CTDL DELAY UNDER CURRENT MODE TO CTDL COUPLING.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.												
NAME	CARD ASM TSTR - CTDL					[illegible]-62	115599					
	COUPLING NETWORK											
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
[illegible]-62	115599					

729840

C

STANDARDS CODE

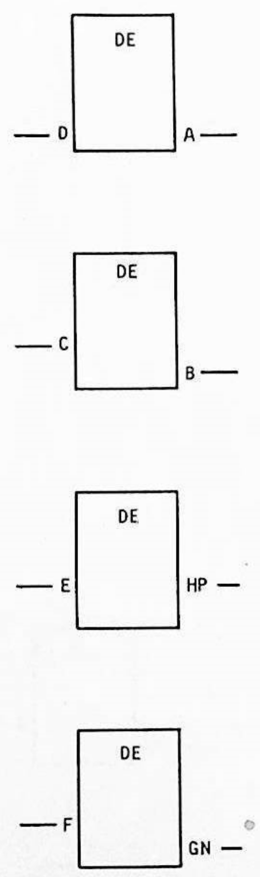
729841

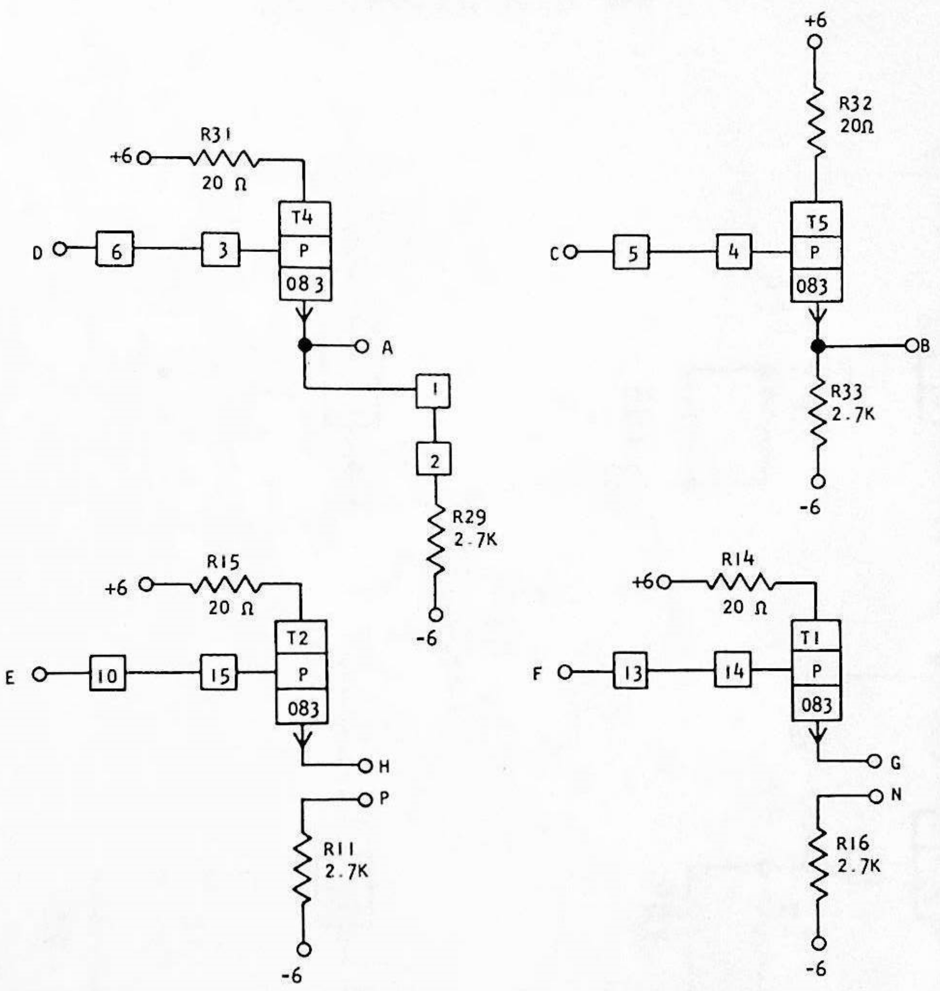
CARD CODE	729841
CN WT/	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371260

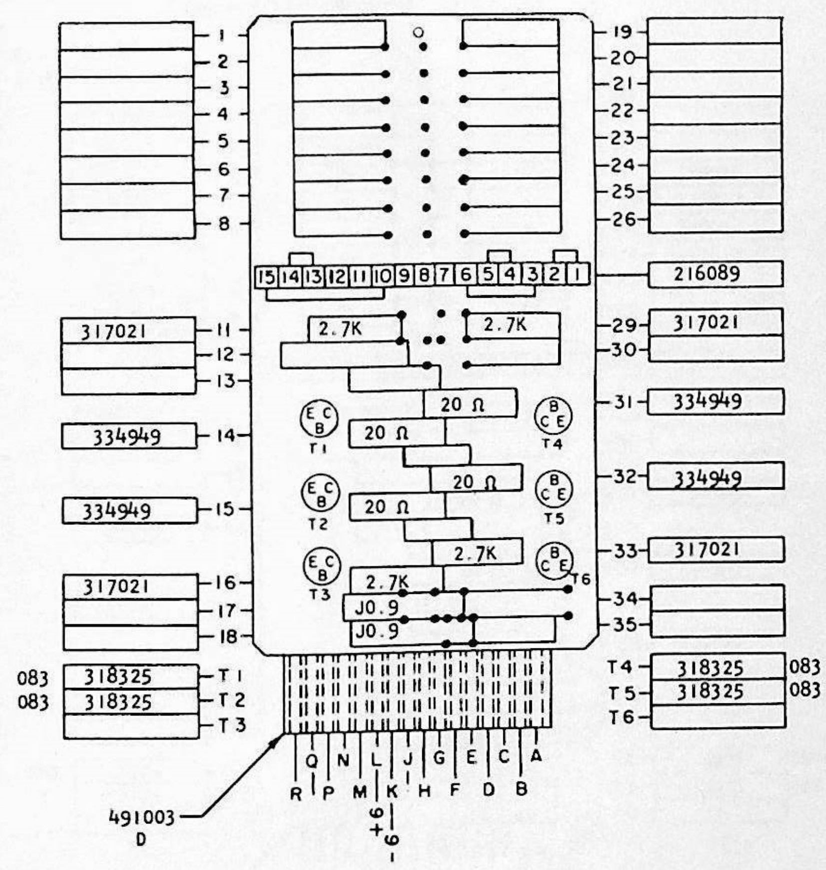
CTDL - EMITTER FOLLOWER NPN





SEQUENCE OF OPERATION

1. OUTPUT WILL FOLLOW INPUT, TRANSISTOR ALWAYS IN CONDUCTION
2. LOGICAL FUNCTIONS PREFORMED WHEN OUTPUTS SHARE COMMON LOAD
3. T1, T2, EMITTER MUST BE LOADED



PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
C, D E, F	T	INPUT		UP	1.9	6.24
				DOWN	-5.46	-6.24
A, B H, P	T	OUTPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24

DELAY

THESE IS NO APPRECIABLE DELAY BETWEEN THE INPUT AND THE OUTPUT OF THE EF WHEN THE LOGIC BLOCK THAT DRIVES THE EF IS TURNED OFF.

WHEN THE LOGIC BLOCK THAT DRIVES THE EF IS TURNED ON, THE EF DELAY IS A FUNCTION OF ITS CAPACITIVE LOAD (EXAMPLE: WIRING CAPACITANCE). IN SOME CIRCUIT APPLICATIONS, THIS DELAY CAN BE IN THE ORDER OF 3 OR 4 USEC. IN NORMAL APPLICATION (NO APPRECIABLE WIRING CAPACITANCE ON THE OUTPUT OF THE EF) THE DELAY IS NOT APPRECIABLE.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL				4 -62	115599					
	EMITTER FOLLOWER NPN										
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729841

C

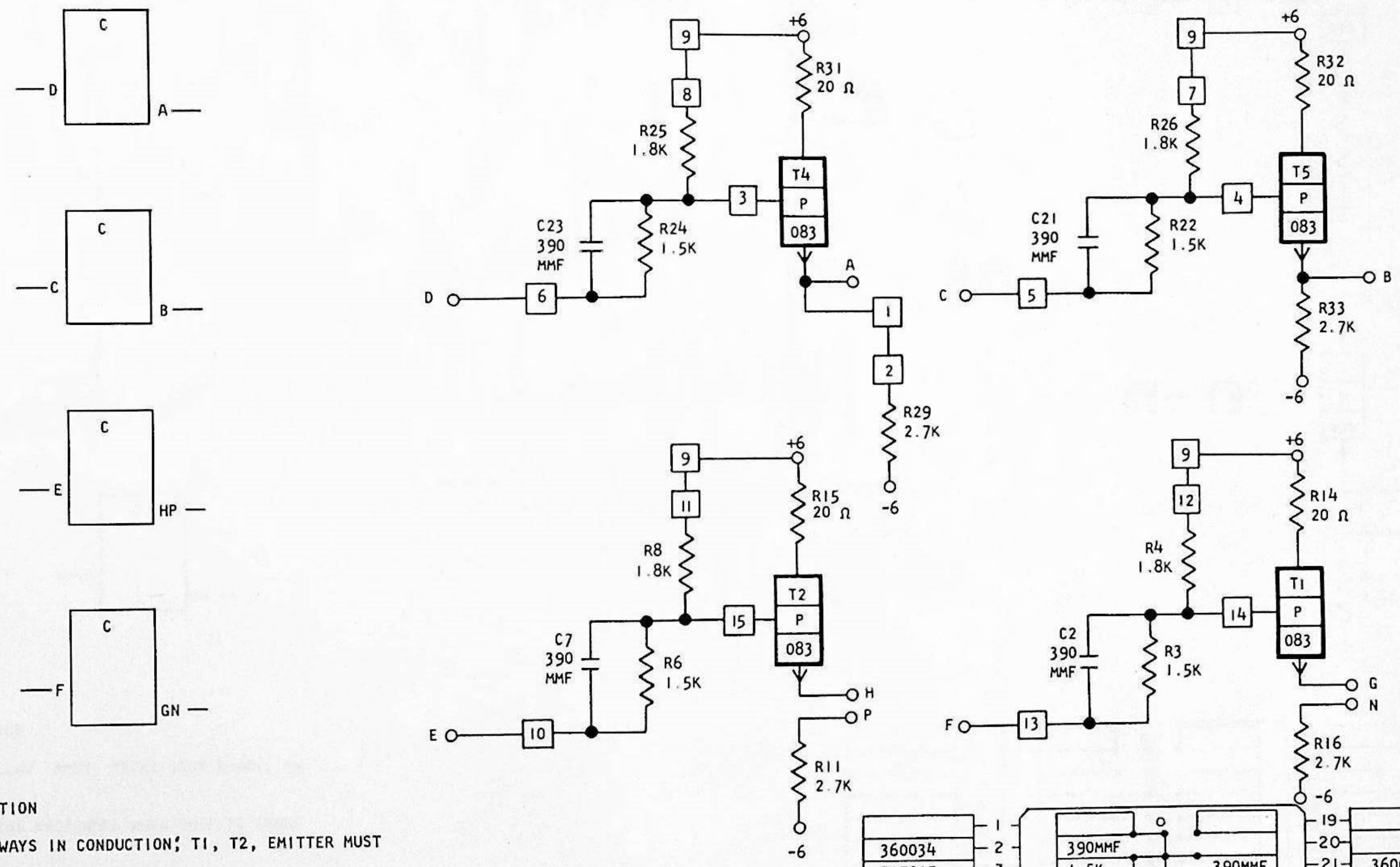
STANDARDS CODE	
729842	

CARD CODE	729842
CN WU	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371258

CTDL-TRANSLATE BLOCK NPN



SEQUENCE OF OPERATION

1. TRANSISTOR ALWAYS IN CONDUCTION; T1, T2, EMITTER MUST BE LOADED
2. OUTPUT WILL FOLLOW INPUT
3. LOGICAL FUNCTIONS PREFORMED WHEN OUTPUTS SHARE COMMON LOAD

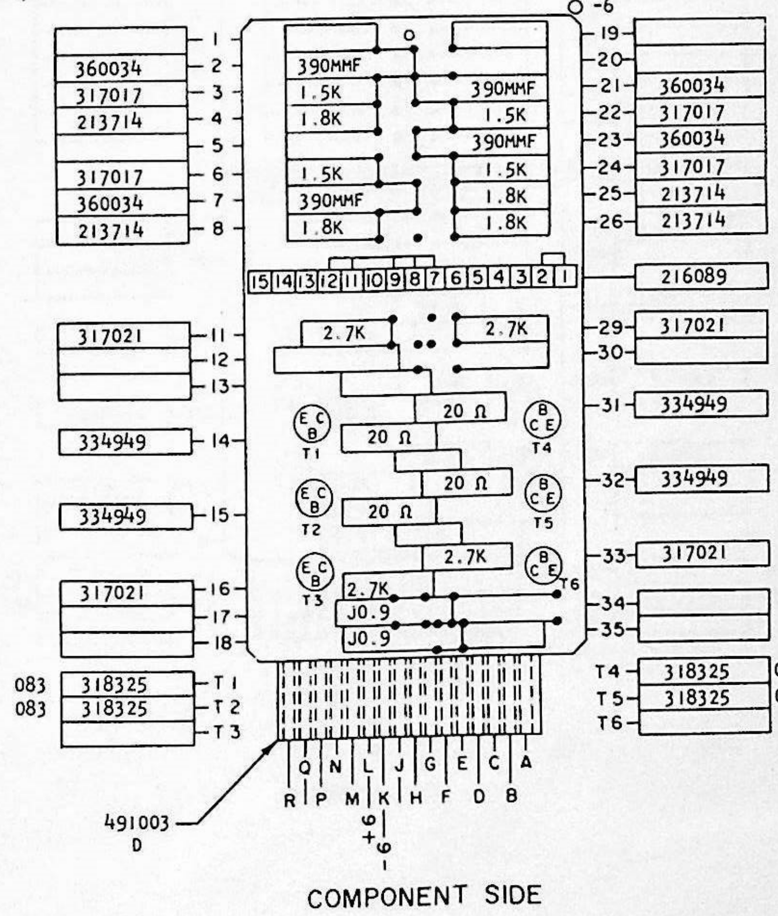
PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
D,C, E,F	U	INPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5
A,B, H,G	T	OUTPUT		UP	1.44	3.12
				DOWN	-0.74	-5.23

DELAY

THE DELAY CHARACTERISTICS OF THE TRANSLATE BLOCK ARE SIMILAR TO THOSE OF THE EF.

NO APPRECIABLE DELAY SHOULD BE NOTICED WHEN THE DRIVING BLOCK IS TURNED ON OR OFF.

APPRECIABLE DELAY CAN BE OBSERVED (1 TO 2.5 USEC.) WHEN THE DRIVING BLOCK IS TURNED ON AND THE OUTPUT OF THE TRANSLATE BLOCK IS DRIVING SIGNIFICANT WIRING CAPACITANCE (SEVERAL FEET OF WIRE FROM ONE GATE TO ANOTHER.)



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL				-62	115599					
	TRANSLATE BLOCK NPN										
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIC 3-17-62							
APPRO			CHECK								

729842

C

STANDARDS CODE

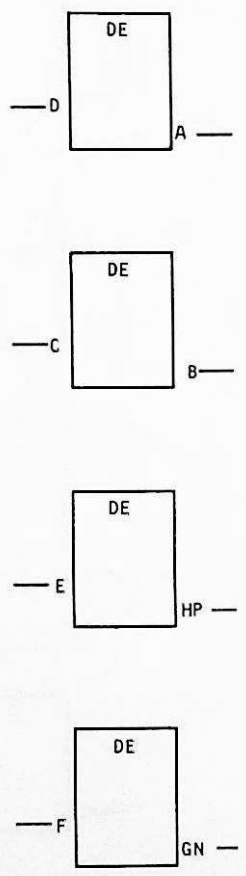
729843

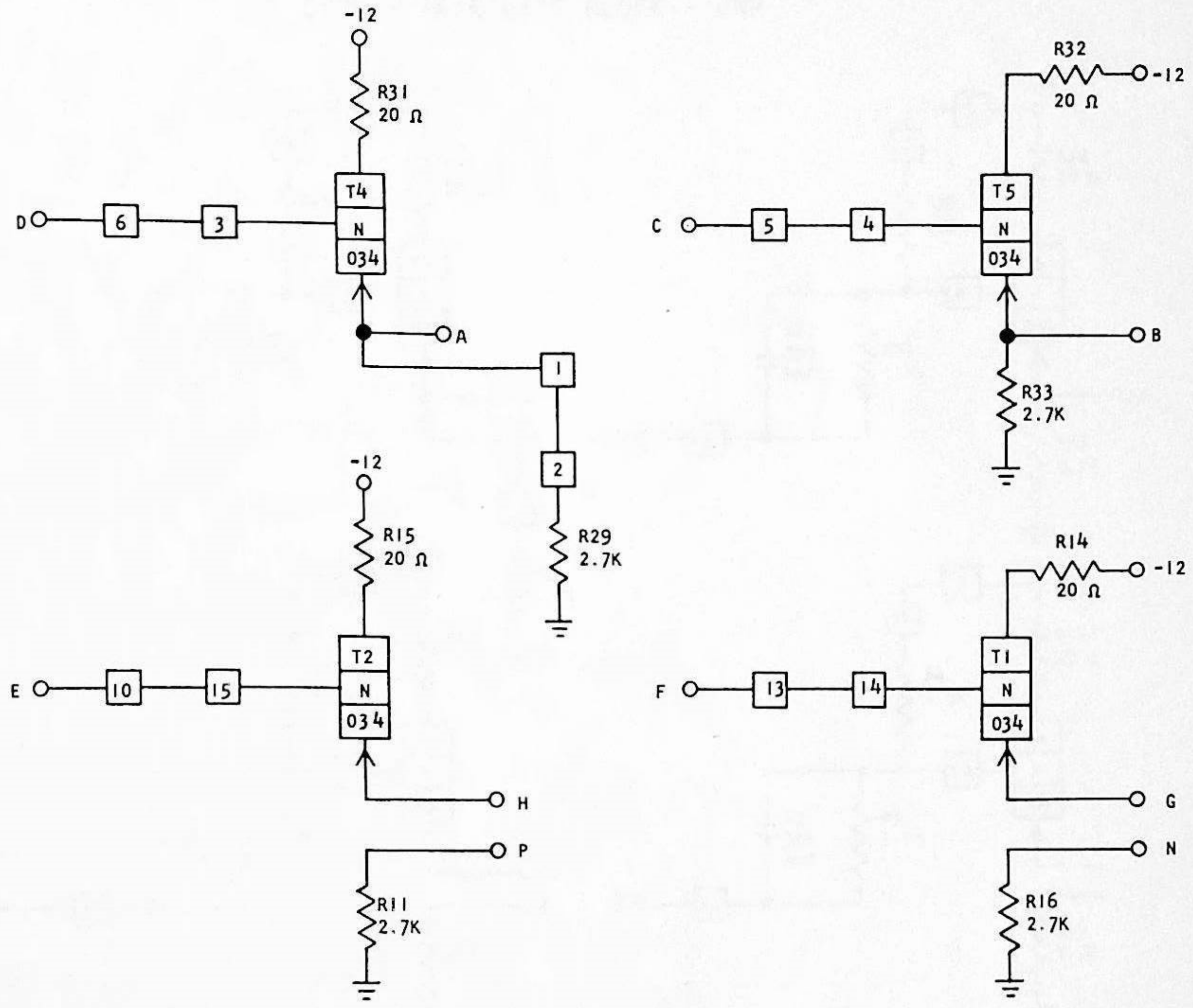
CARD CODE	729843
CP WT	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371259

CTDL - EMITTER FOLLOWER PNP





SEQUENCE OF OPERATION

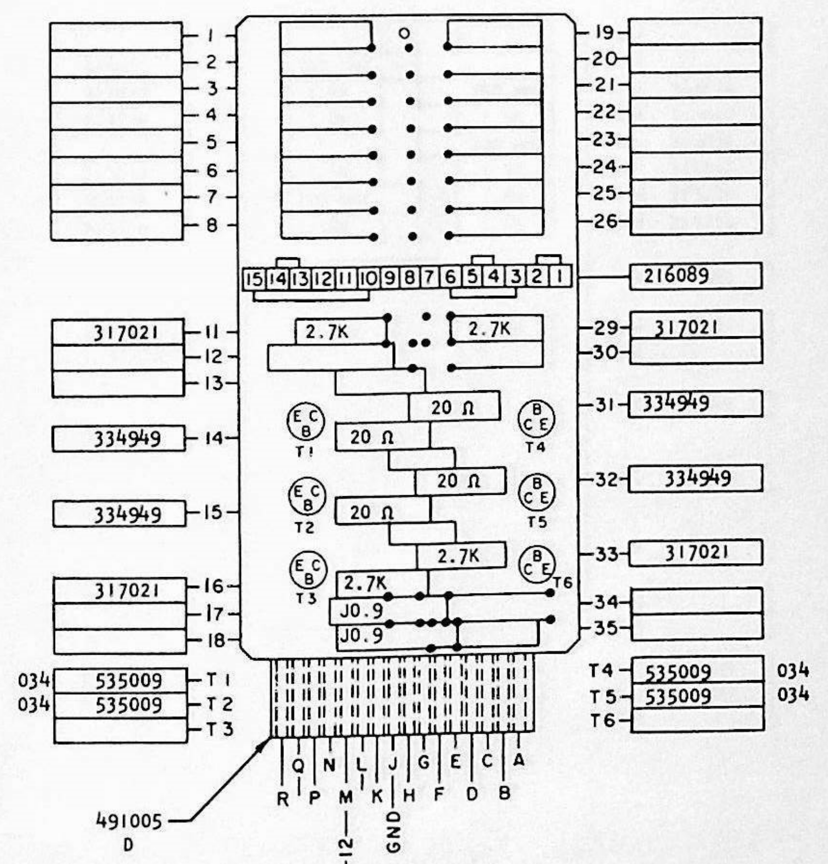
1. OUTPUT WILL FOLLOW INPUT, TRANSISTOR ALWAYS IN CONDUCTION
2. LOGICAL FUNCTIONS PREFORMED WHEN OUTPUTS SHARE COMMON LOAD
3. T1, T2 EMITTER MUST BE LOADED

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D, C, E, F	U	INPUT		UP	-5.5	+.24
				DOWN	-7.6	-12.5
A, B, H, G	U	OUTPUT		UP	-5.3	0.2
				DOWN	-7.4	-12.5

DELAY

THERE IS NO APPRECIABLE DELAY BETWEEN THE INPUT AND THE OUTPUT OF THE EF WHEN THE LOGIC BLOCK THAT DRIVES THE EF IS TURNED OFF.

WHEN THE LOGIC BLOCK THAT DRIVES THE EF IS TURNED ON, THE EF DELAY IS A FUNCTION OF ITS CAPACITIVE LOAD (EXAMPLE: WIRING CAPACITANCE). IN SOME CIRCUIT APPLICATIONS, THIS DELAY CAN BE IN THE ORDER OF 3 OR 4 USEC. IN NORMAL APPLICATION (NO APPRECIABLE WIRING CAPACITANCE ON THE OUTPUT OF THE EF) THE DELAY IS NOT APPRECIABLE.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL			6-7 62	115599					
	EMITTER FOLLOWER PNP									
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

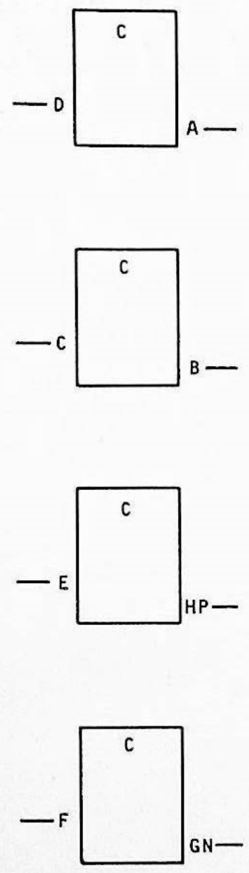
729843

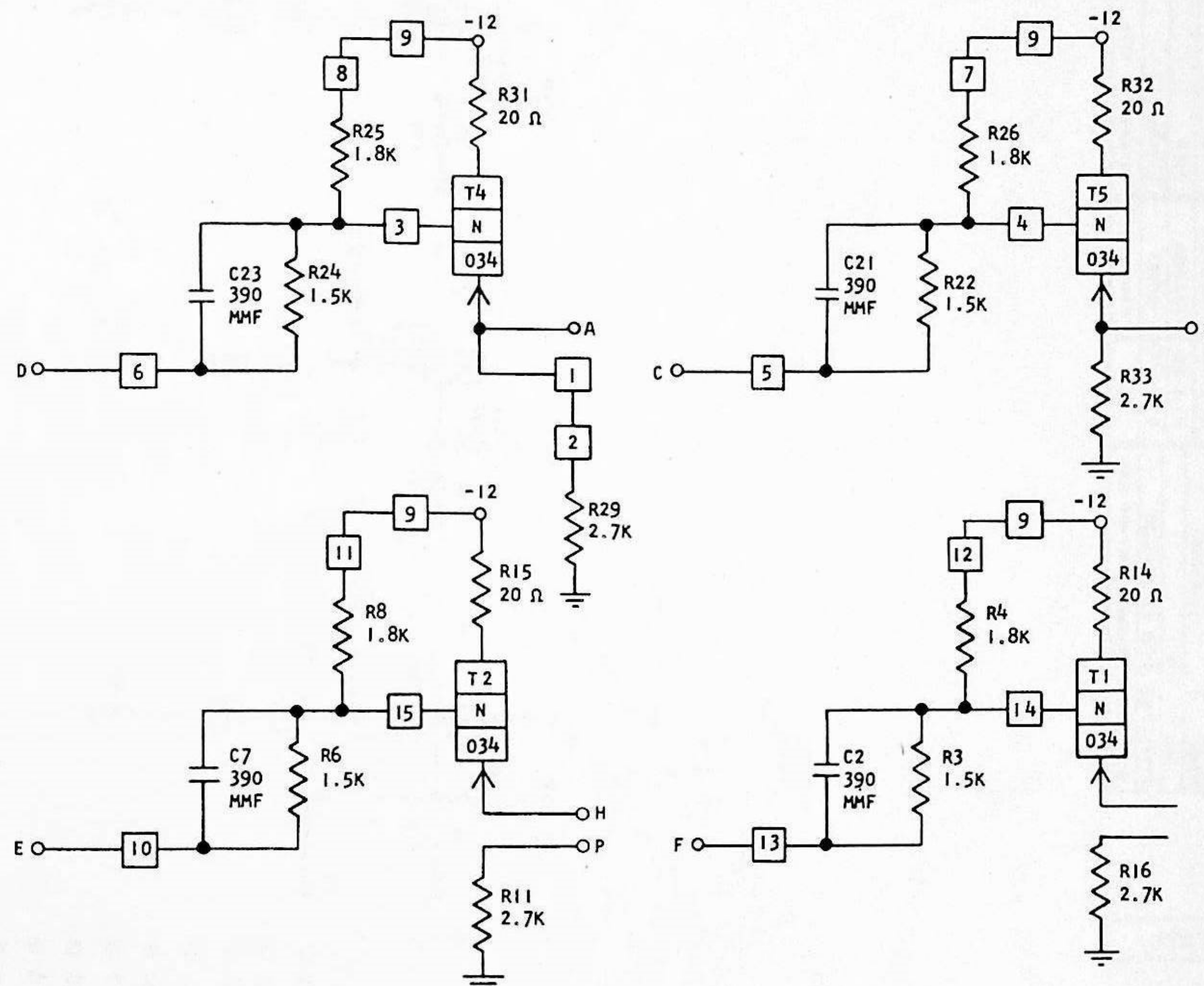
C

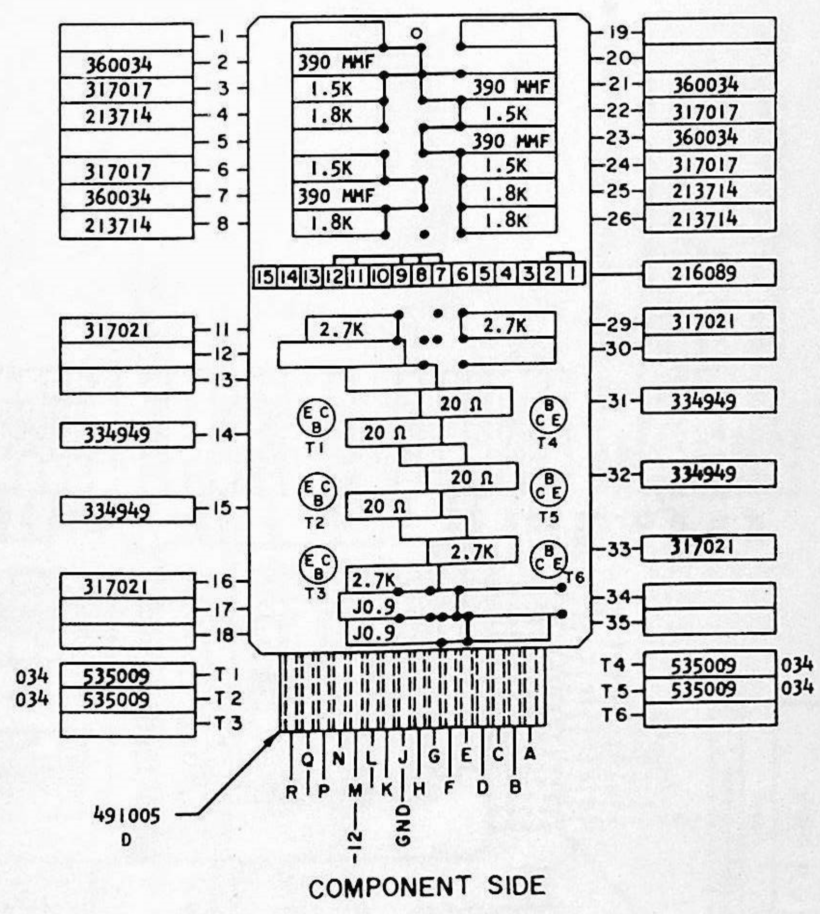
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371257

CTDL - TRANSLATE BLOCK - PNP







SEQUENCE OF OPERATION

1. OUTPUT WILL FOLLOW INPUT, TRANSISTOR ALWAYS IN CONDUCTION
2. LOGICAL FUNCTIONS PREFORMED WHEN OUTPUTS SHARE COMMON LOAD
3. T1, T2 EMITTER MUST BE LOADED

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
D,C E,F	T	INPUT		UP	1.44	6.24
				DOWN	-5.5	-6.24
A,B H,G	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2

DELAY

THE DELAY CHARACTERISTICS OF THE TRANSLATE BLOCK ARE SIMILAR TO THOSE OF THE EF.

NO APPRECIABLE DELAY SHOULD BE NOTICED WHEN THE DRIVING BLOCK IS TURNED ON OR OFF.

APPRECIABLE DELAY CAN BE OBSERVED (1 TO 2.5 USEC.) WHEN THE DRIVING BLOCK IS TURNED ON AND THE OUTPUT OF THE TRANSLATE BLOCK IS DRIVING SIGNIFICANT WIRING CAPACITANCE (SEVERAL FEET OF WIRE FROM ONE GATE TO ANOTHER).

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR -CTDL TRANSLATE BLOCK - PNP				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
4 -62	115599					

SEQUENCE OF OPERATION

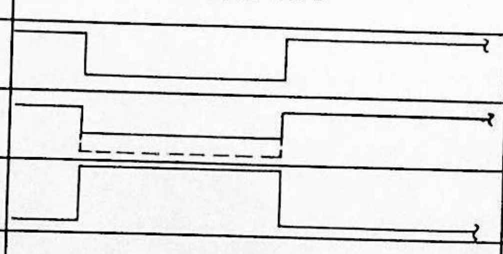
1. DOWN INPUT TRANSISTOR ON OUTPUT UP

2. UP INPUT TRANSISTOR OFF OUTPUT DOWN

3. INPUTS ON EXTENDER CARD DOWN IN COINCIDENCE WITH DOWN INPUT ON CARD FOR UP OUTPUT

4. COLLECTORS MUST BE LOADED

5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
E,F, H,D	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
N,B		EXTENDER INPUT		UP	+6.0	
				DOWN	0.0	
G,C, P,A	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

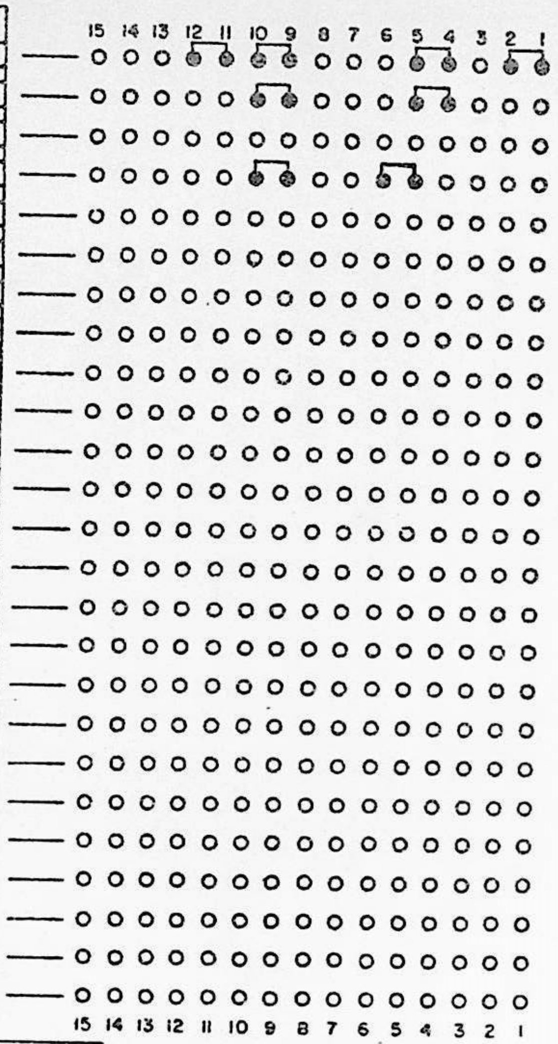
CARD CODE	STANDARDS CODE	370981
CO **	2-7045	

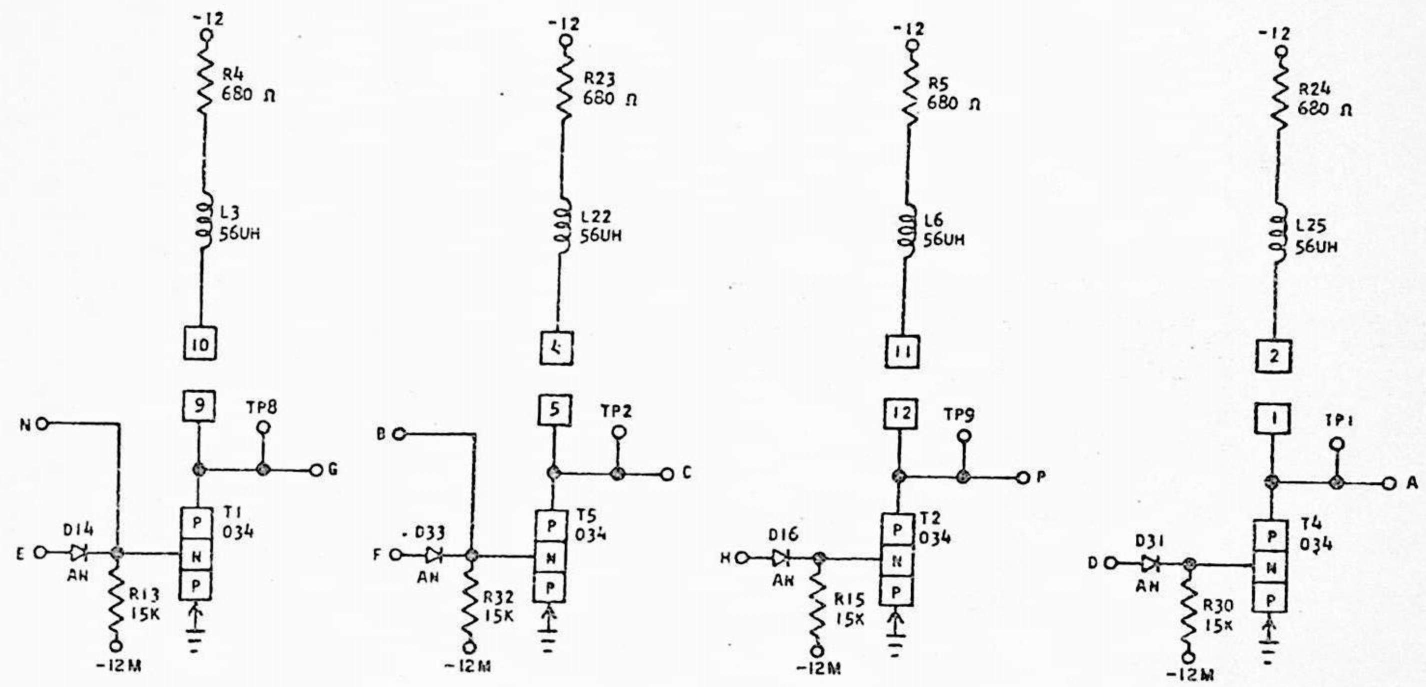
CTDL ONE WAY PNP FIELD REPLACEMENT

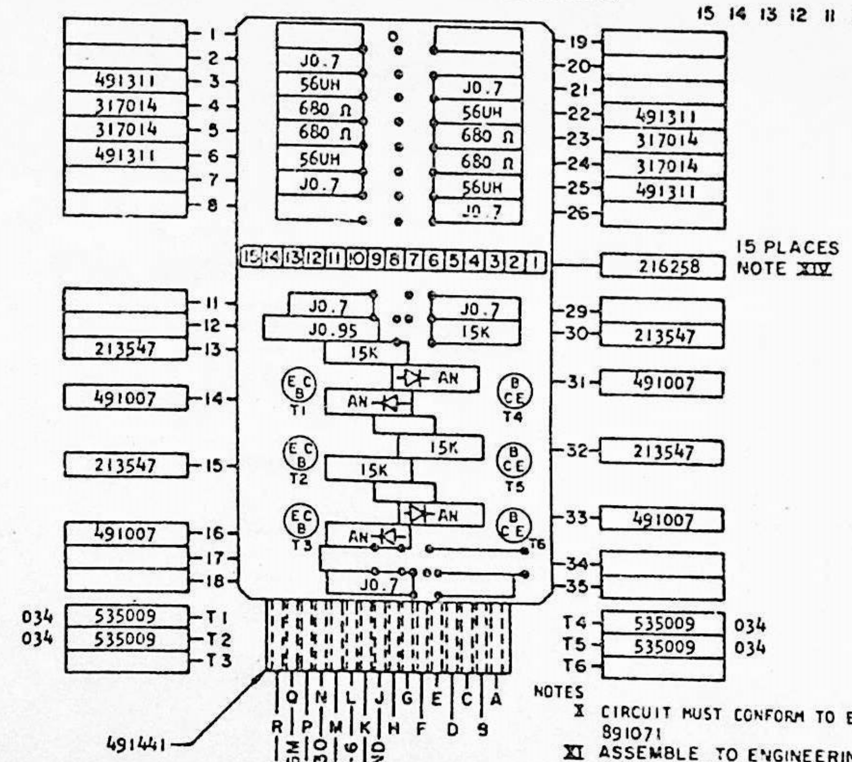
DISCONTINUED

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC
CTDL ONE WAY PNP-4 LOADS	ZV	371271	891071
CTDL ONE WAY PNP-2 LOADS	ZT	371272	891071
CTDL ONE WAY PNP-NO LOAD	—	371273	891071
CTDL ONE WAY PNP-1 LOAD	YG	371278	891071

CAP CONFIGURATION







NOTES

I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891071

XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999

XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED

XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491296

XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H. B. Haford	7-6-60

370981

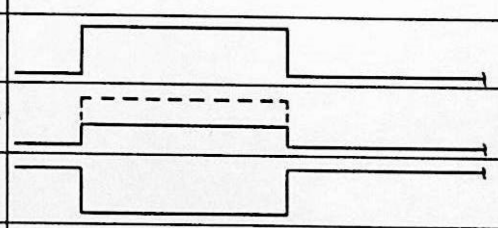
INTERNATIONAL BUSINESS MACHINES CORP.				
NAME	CARD ASM TSTR-CTDL ONE WAY PNP			
DESIGN		TYPE	SMS	
DETAIL		SCALE	NONE	
CHECK	TGJ 3-1-60	DRAW	MDE	7-7-60
APPROVED	FES 3-3-60	CHECK		7-11-60

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
8-4-60	109642	[illegible]				X0660
11-4-60	D109900	IWB				
12-1-60	110517	IWB				

370981

SEQUENCE OF OPERATION

1. UP INPUT TRANSISTOR ON OUTPUT DOWN
2. DOWN INPUT TRANSISTOR OFF OUTPUT UP
3. INPUTS ON EXTENDER CARD UP IN COINCIDENCE WITH UP INPUT ON CARD FOR DOWN OUTPUT
4. COLLECTORS MUST BE LOADED
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
E,F, H,D	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
N,B		EXTENDER INPUT		UP	-6.	
				DOWN	-12.	
G,C, P,A	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.70
TURN OFF	0.05	1.50*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

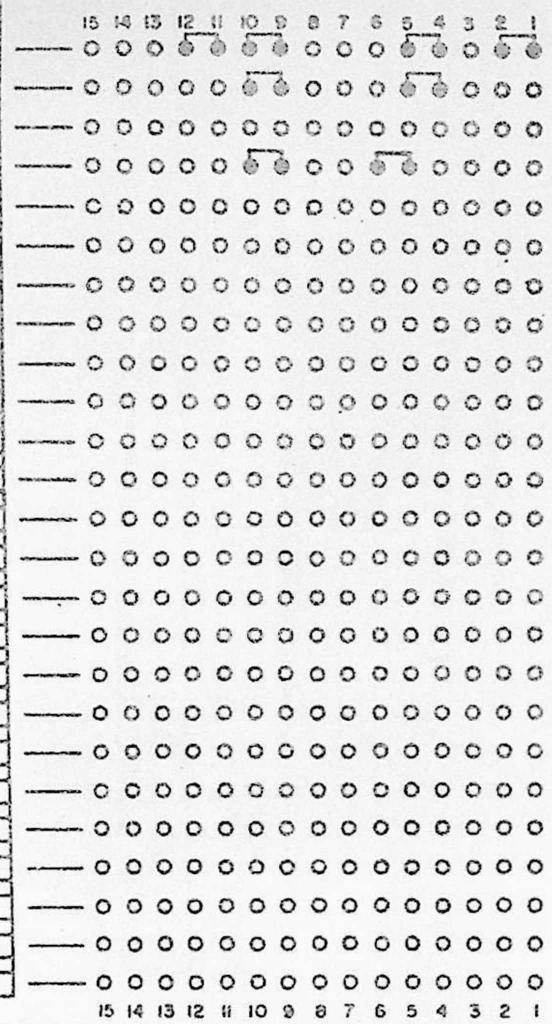
CARD CODE	STANDARDS CODE	370980
CR **	2-7045	

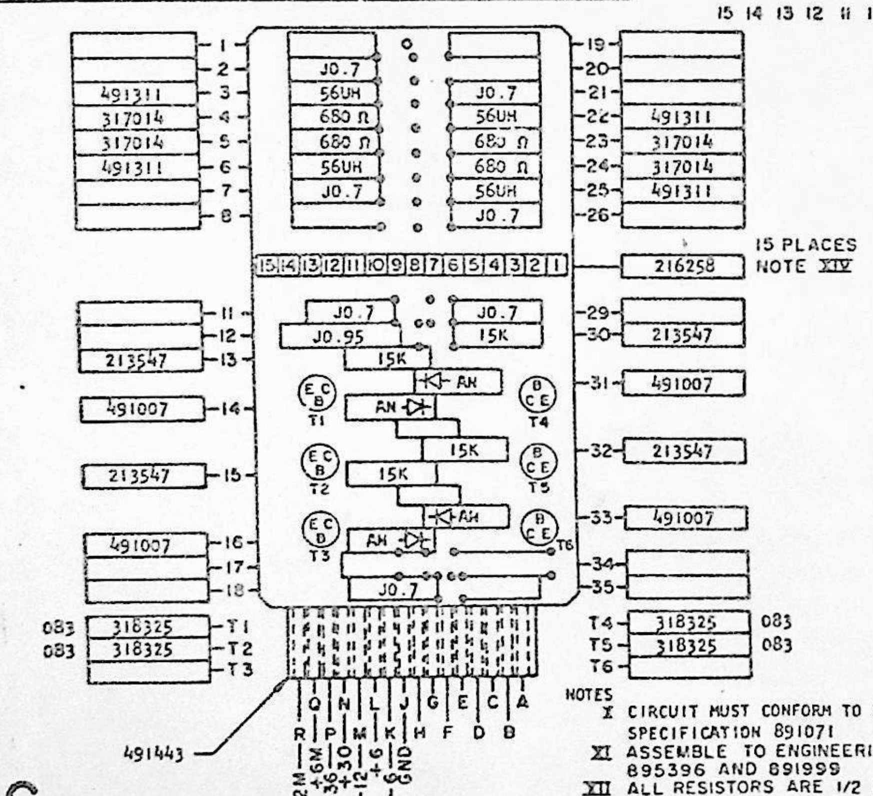
DISCONTINUED

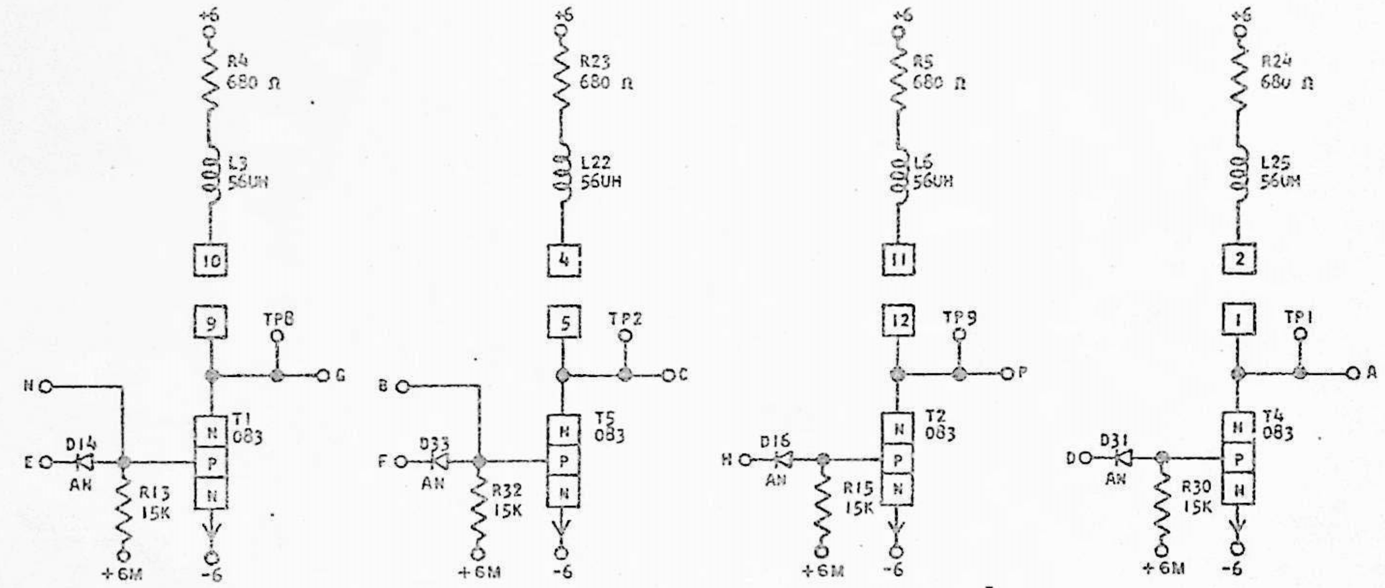
CTDL ONE WAY NPN
FIELD REPLACEMENT

CAP CONFIGURATION

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC
CTDL ONE WAY-4 LOADS	ZY	371274	891071
CTDL ONE WAY NPN-2 LOADS	ZT	371275	891071
CTDL ONE WAY NPN-NO LOAD	—	371276	891071
CTDL ONE WAY NPN-1 LOAD	YG	371277	891071







NOTES
- X CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891071
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
- XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED
- XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491296
- XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H. D. Hanford	7-6-60

370980

INTERNATIONAL BUSINESS MACHINES CORP.
NAME CARD ASM TSTR-CTDL ONE WAY NPN
TYPE SMS — SCALE NONE — DRAWN 7-7-60

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
8-4-60	109642	DWB				X0666
11-4-60	D109900	IWB				
12-1-60	110517	IWB				

370980

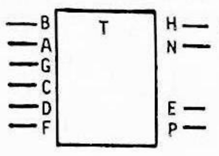
STANDARDS CODE	

729853

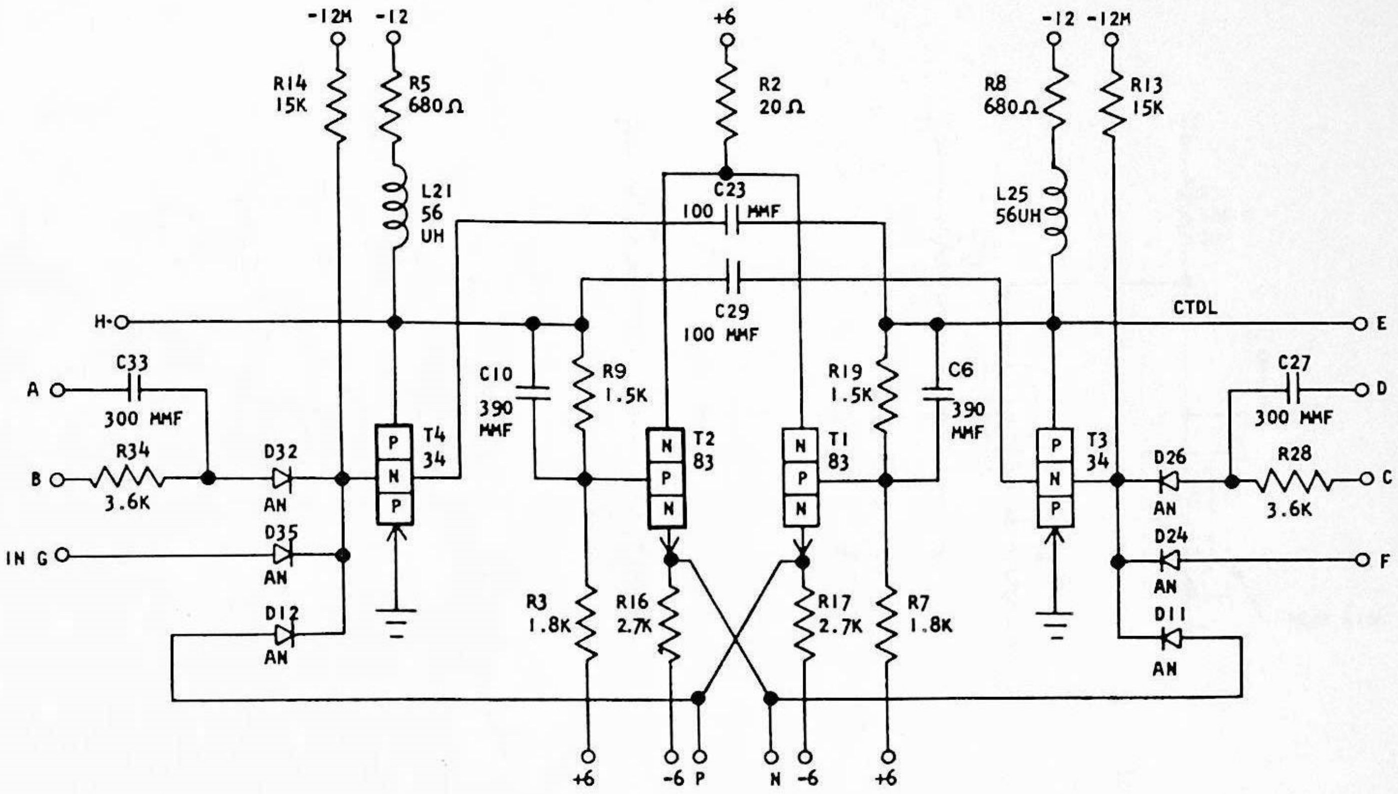
CARD CODE	729853
CW --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371534

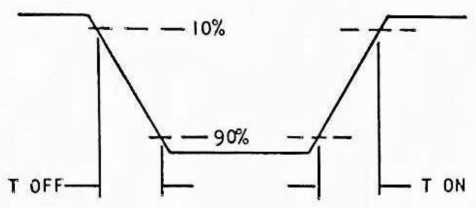


CTDL TRIGGER



DELAY - USEC

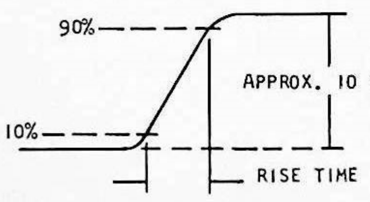
TYPICAL INVERTER AND EF OUTPUT WAVEFORM



INVERTER DELAY	MINIMUM	MAXIMUM
T OFF	0.15	0.8
T ON	0.10	0.3
EF DELAY	MINIMUM	MAXIMUM
T OFF	0.05	0.1
T ON	0.10	0.4

THE FOLLOWING DELAY INFORMATION APPLIES WHEN THE AC TRIGGERING INPUT PULSE HAS A RISE TIME OF 0.45 USEC. (SEE FOLLOWING FIGURE)

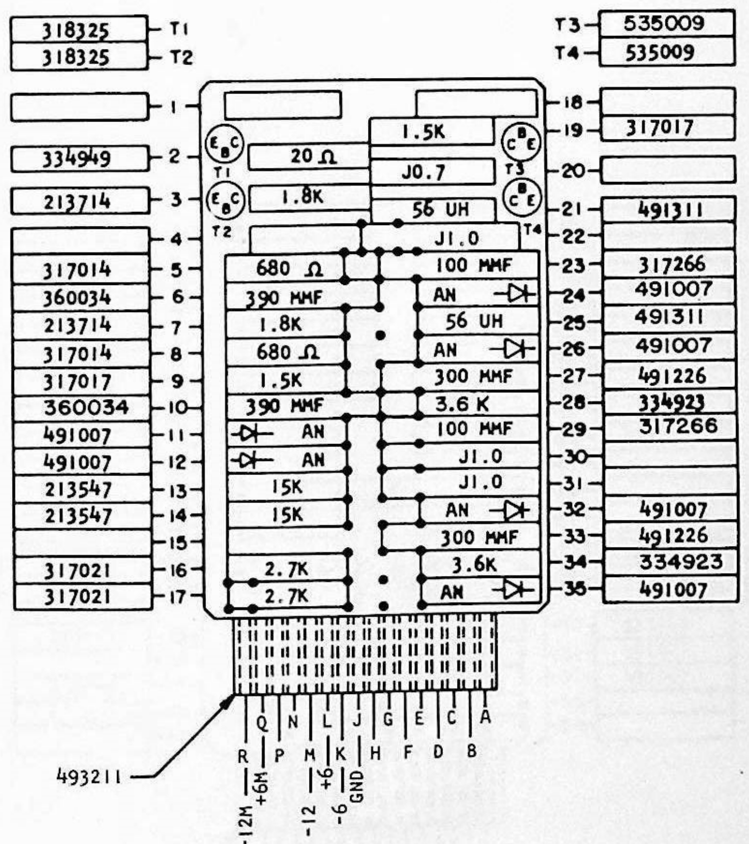
TRIGGERING PULSE



	MINIMUM	MAXIMUM
FROM AC SET TO INVERTER OUTPUTS	0.10	0.40
FROM AC SET TO EF OUTPUTS	0.10	0.30

SEQUENCE OF OPERATION

1. T4, T2 ON, T3, T1 OFF
2. GATE UP TO PIN B, AC SET TO PIN A T3, T1 ON T4, T2 OFF
3. GATE UP TO PIN C, AC SET TO PIN D T3, T1 OFF T4, T2 ON
4. GATE MUST BE UP 3.75 U SEC BEFORE AC SET
5. DC SET PIN G, T3, T1 ON T4, T2 OFF
6. COLLECTIVE PULLOVER MAY BE USED TO TURN T3 OR T4 ON
7. DC SET ON PIN F UP WHEN T1, T3 ARE ON WILL RESET TO CONDITION 1
8. DC SET OR RESET PULSE WIDTH: 0.5 USEC MINIMUM.



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B	U	GATE		UP	-0.54	0.24
				DOWN	-7.44	-12.4
A,D	U	AC SET		UP	-0.54	0.24
				DOWN	-7.44	-12.4
G	T	DC SET		UP	1.44	6.24
				DOWN	-0.74	-6.24
E	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2
N	T	OUTPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C	U	GATE		UP	-0.54	0.24
				DOWN	-7.44	-12.4
F	T	DC SET		UP	1.44	6.24
				DOWN	-0.74	-6.24
P	T	OUTPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
H	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-CTDL TRIGGER				6 62	115599					
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729853

C

STANDARDS CODE

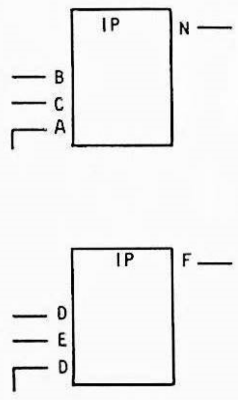
729854

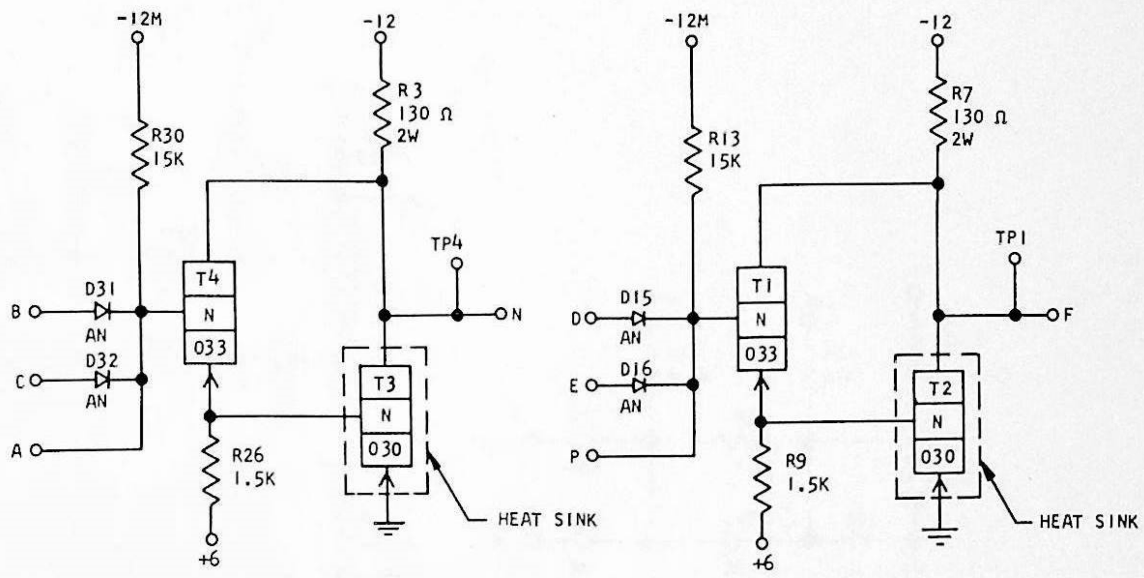
CARD CODE	729854
CY --	

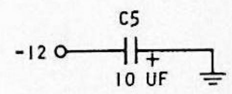
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371542

CTDL POWER INVERTER



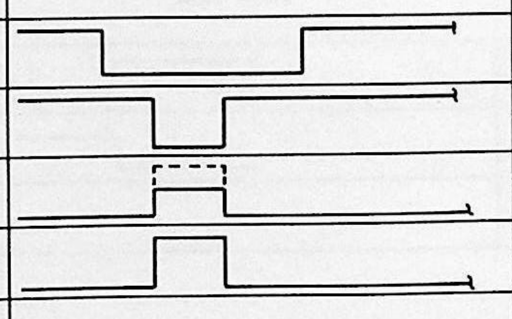




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN T4, T1 ON; T3, T2 OFF OUTPUT UP
2. ANY INPUTS UP T4, T1, OFF; T3, T2 ON OUTPUT DOWN
3. DOWN INPUT OF AT LEAST 1 U SEC REQUIRED TO TURN T4 OR T1 ON
4. EXTENDER INPUTS MUST BE DOWN IN COINCIDENCE WITH INPUTS ON CARD FOR UP OUTPUT

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
B,D	T	INPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
C,E	T	INPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
A,E		EXTENDER INPUT		UP	-6	
				DOWN	-12	
N,F	U	OUTPUT		UP	-5.2	0.8
				DOWN	-7.4	-9.2



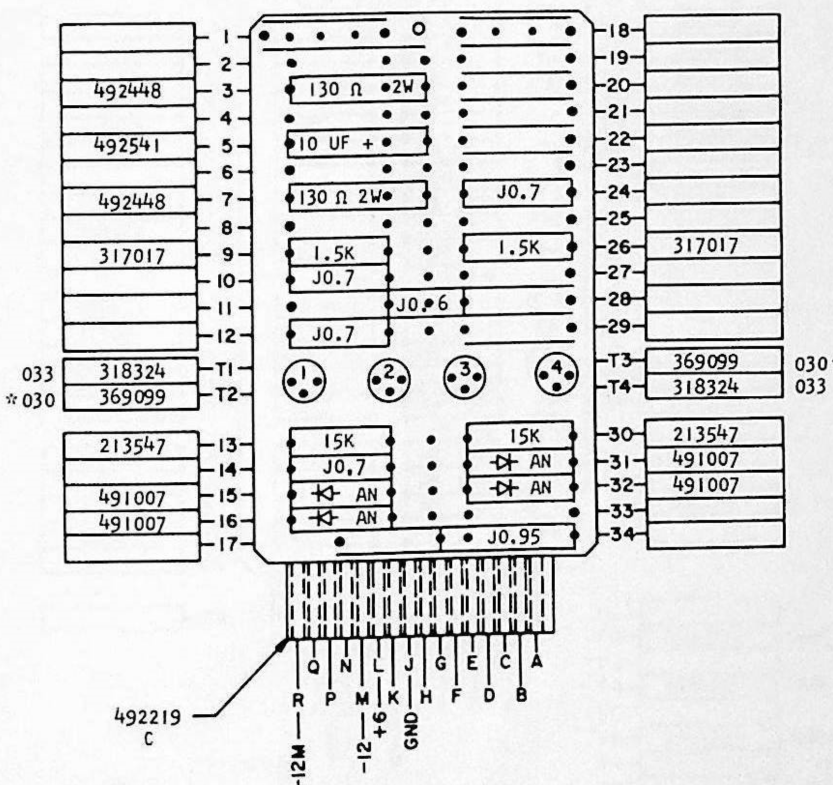
DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.20	0.60*
TURN OFF	0.25	0.40**

*THIS DELAY CAN INCREASE TO 0.75 USEC FOR CAPACITIVE LOAD.

**THIS DELAY CAN INCREASE TO 0.55 USEC FOR CAPACITIVE LOAD.

NOTE: LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL POWER INVERTER				6 -1-62	115599					729854
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

STANDARDS CODE	

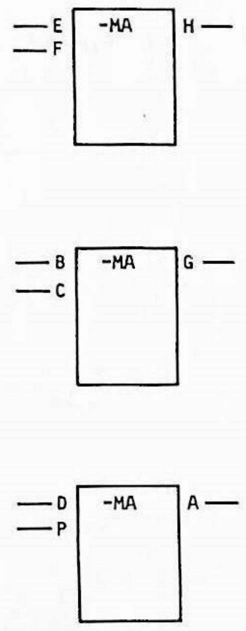
729855

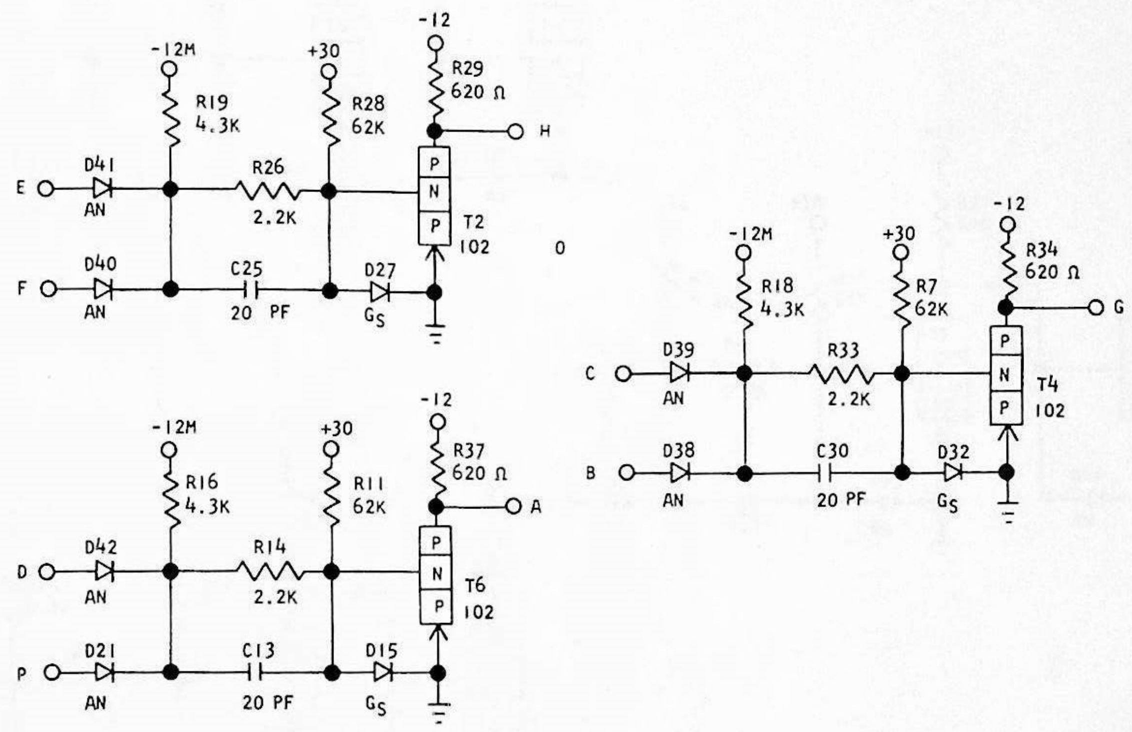
CARD CODE	729855
D A B -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371924

DTDL - AND GATE



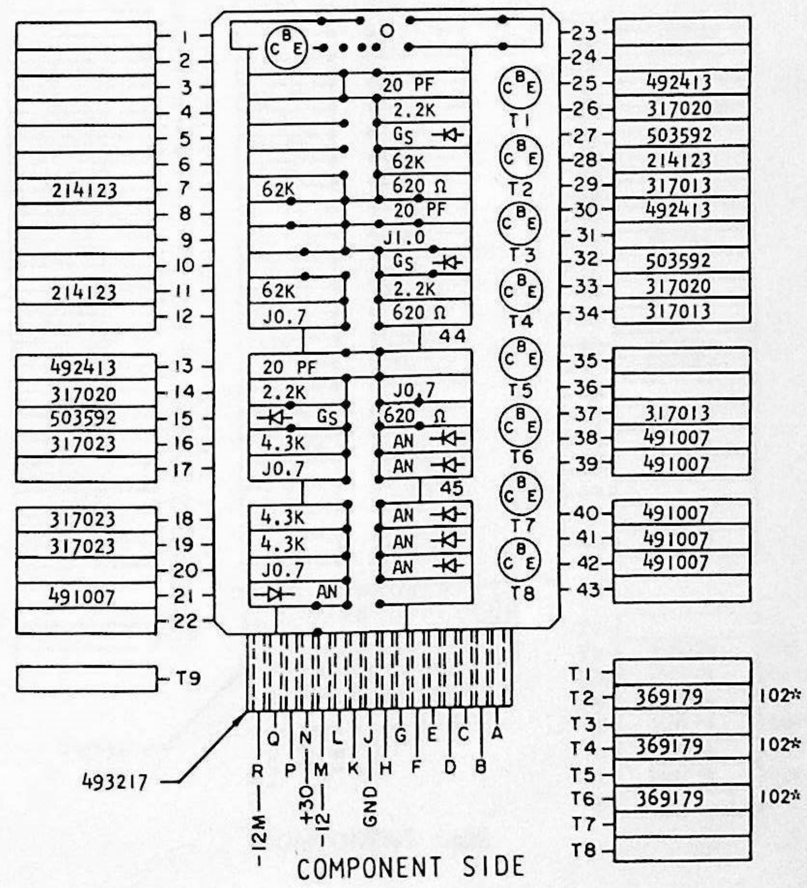


SEQUENCE OF OPERATION

1. INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. EITHER OR BOTH INPUTS UP TRANSISTOR OFF AND OUTPUT IS DOWN
3. DRIVING CTDL LOADS:
   MAXIMUM TURN ON DELAY - .28 USEC
   MAXIMUM TURN OFF DELAY - .09 USEC

   DRIVING WORST CASE CLOCK LOAD
   MAXIMUM TURN ON DELAY - .15 USEC
   MAXIMUM TURN OFF DELAY - .144 USEC

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,F, D,P, C,B	T	INPUTS		UP	+1.44	+6.24
				DOWN	-4.46	-6.24
H A G	U	OUTPUTS		UP	-.89	+.24
				DOWN	-7.44	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - DTDL- AND GATE			4-2-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729855

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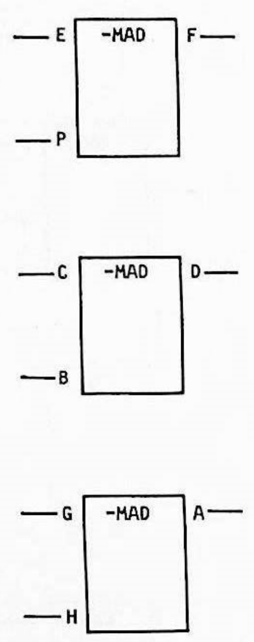
729856

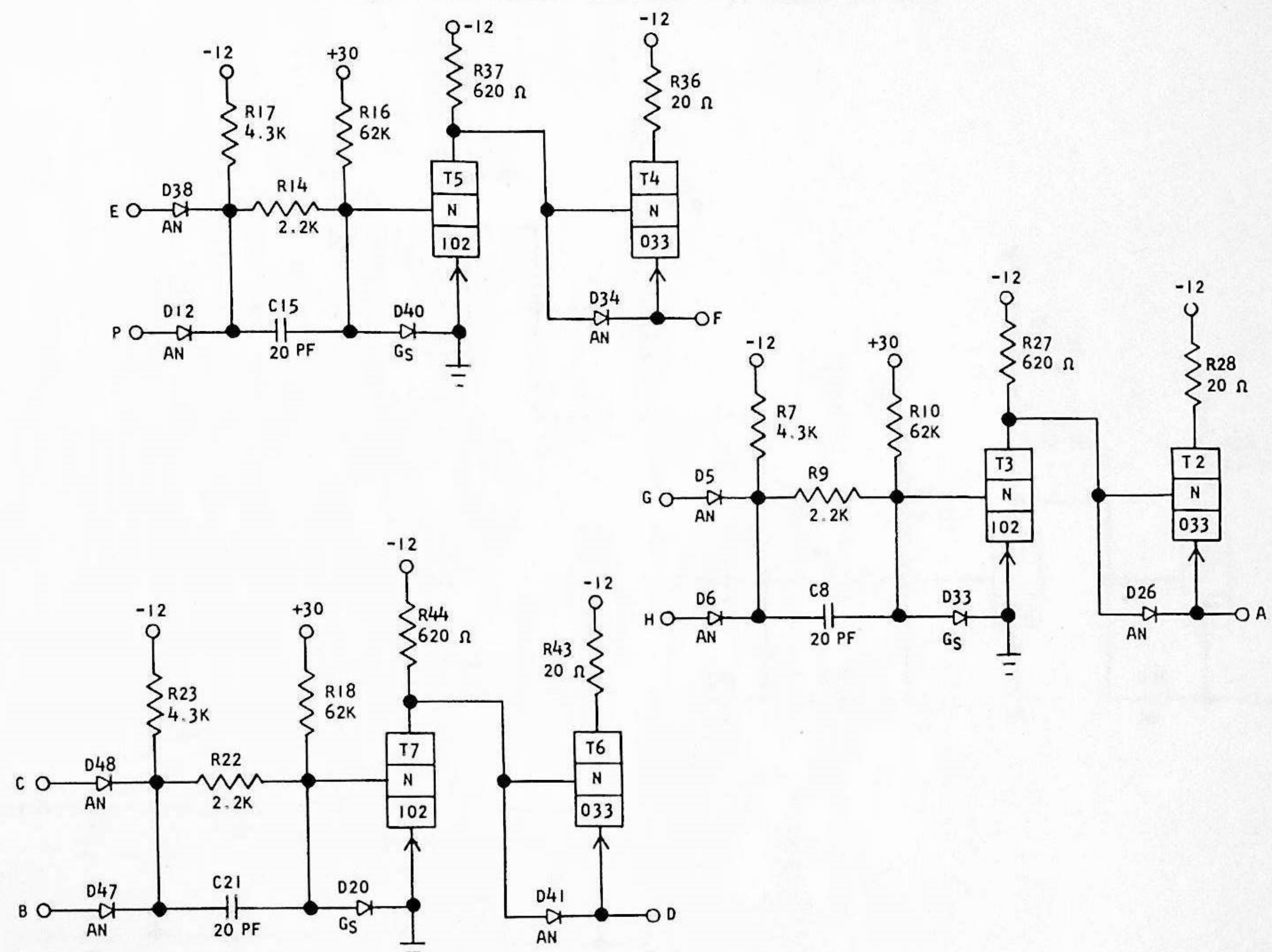
STANDARDS CODE

CARD CODE	729856
D G P -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370343

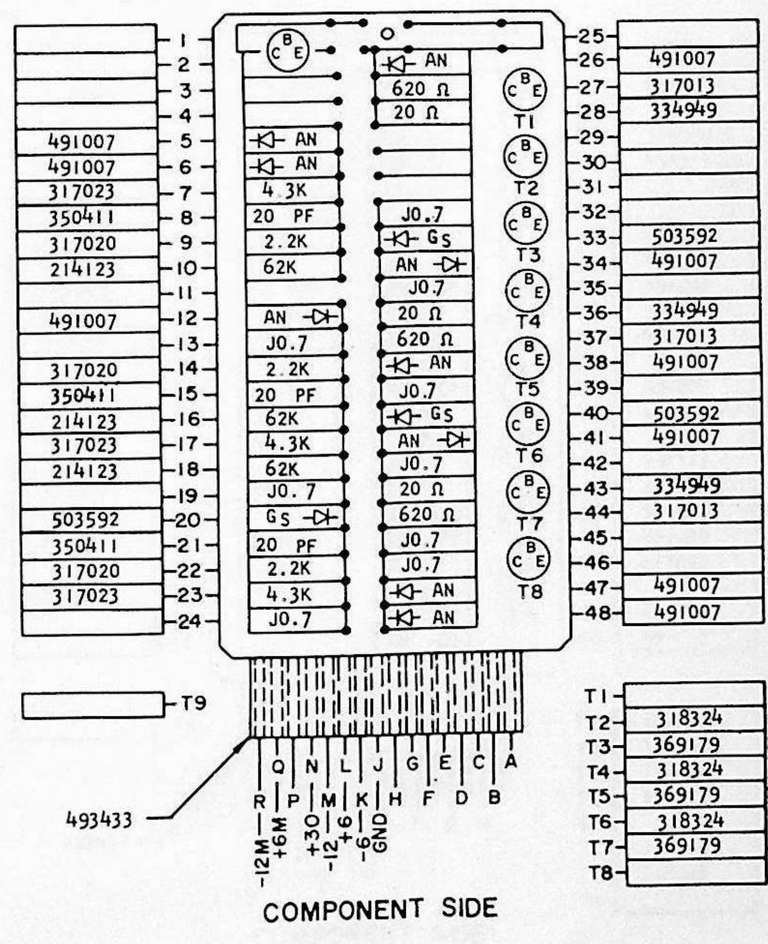




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN T5 TURNS ON, T4 OFF, OUTPUT IS UP
2. ANY INPUT UP, T5 OFF, T4 ON, OUTPUT IS DOWN
3. DELAY DRIVING CTDL LOADS
   TURN ON .28 USEC MAX
   TURN OFF .1 USEC MAX
4. DELAY DRIVING CLOCK LOAD
   TURN ON .15 USEC
   TURN OFF .15 USEC

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
E,P, C,B, G,H	T	INPUT		UP	1.44	6.24
				DOWN	-4.46	-6.24
F D A	U	OUTPUT		UP	-.89	.24
				DOWN	-7.44	-12.48



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.			
NAME	CARD ASM TSTR-CLOCK - AND WITH EMITTER FOLLOWER DRIVER		
DESIGN		MODEL	SMS
DETAIL	RQ 3-1-62	SCALE	NONE
CHECK	WH 3-1-62	DRAW	LIG 3-17-62
APPRO		CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6 -62	115599					

729856

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STANDARDS CODE

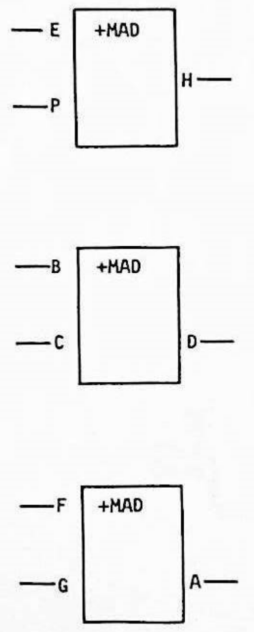
729857

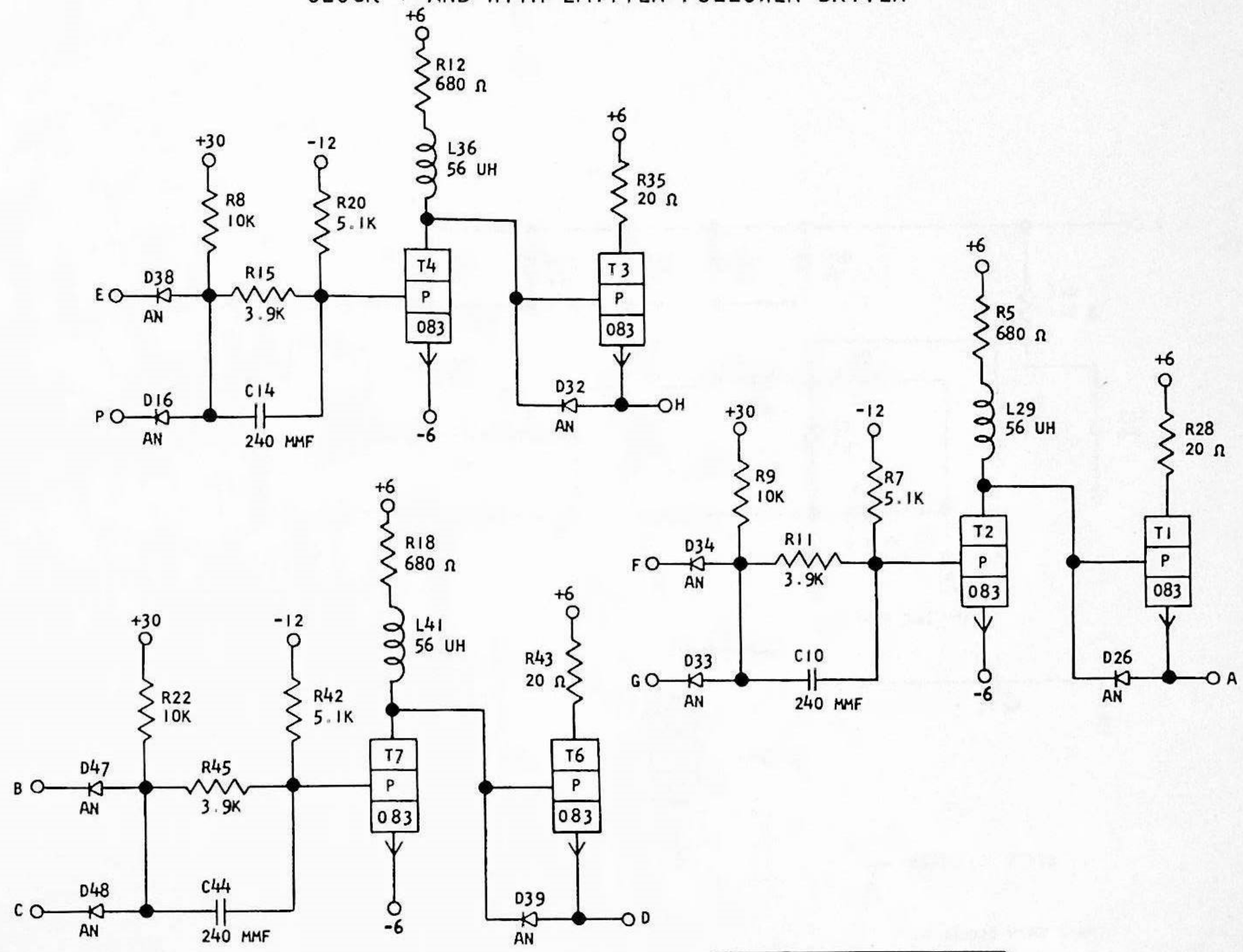
CARD CODE	729857
D G Q -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370342

CLOCK + AND WITH EMITTER FOLLOWER DRIVER

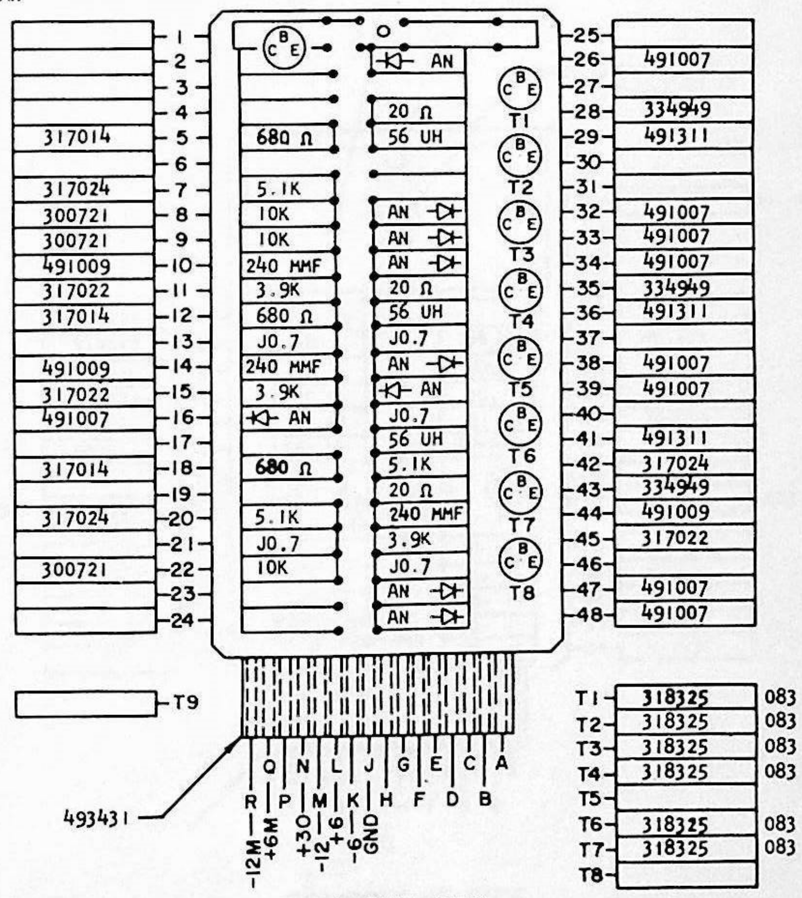




SEQUENCE OF OPERATION

1. ALL INPUTS UP, T4 IS ON, T3 IS OFF, OUTPUT IS DOWN
2. ONE INPUT DOWN, T4 IS OFF, T3 IS ON, OUTPUT IS UP
3. DELAY WHEN DRIVING CTDL LOADS
   TURN ON .1 USEC MAX
   TURN OFF .25 USEC MAX
4. DELAY WHEN DRIVING CLOCK LOAD
   TURN ON .26 USEC MAX
   TURN OFF .12 USEC MAX

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
E,F,B	T	INPUT		UP	3.68	6.24
				DOWN	-4.46	-6.24
P,G,C	T	INPUT		UP	3.68	6.24
				DOWN	-4.46	-6.24
H,A,D	T	OUTPUT		UP	3.89	6.24
				DOWN	-4.46	-6.24



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CLOCK +AND					6-27-62	115599					
WITH EMITTER FOLLOWER DRIVER												
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729857

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STANDARDS CODE

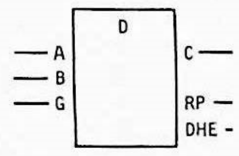
729858

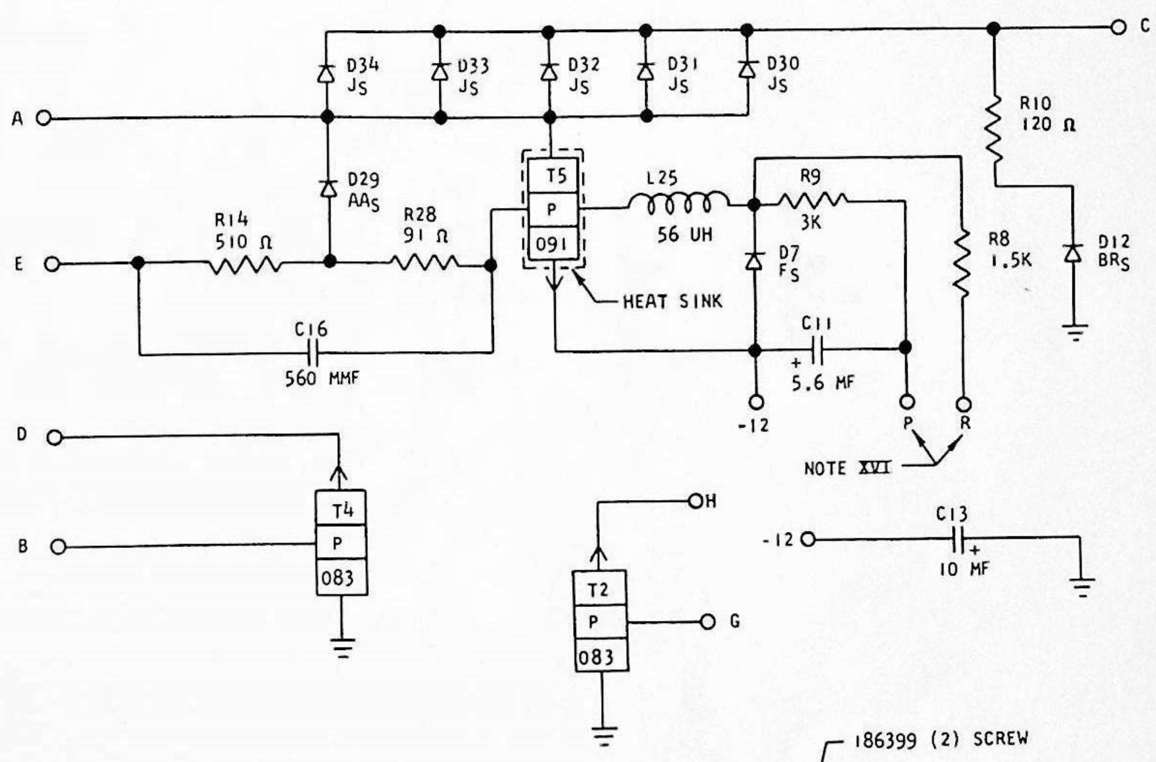
CARD CODE	729858
D K A -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370443

ALLOY-DRIVER, CURRENT

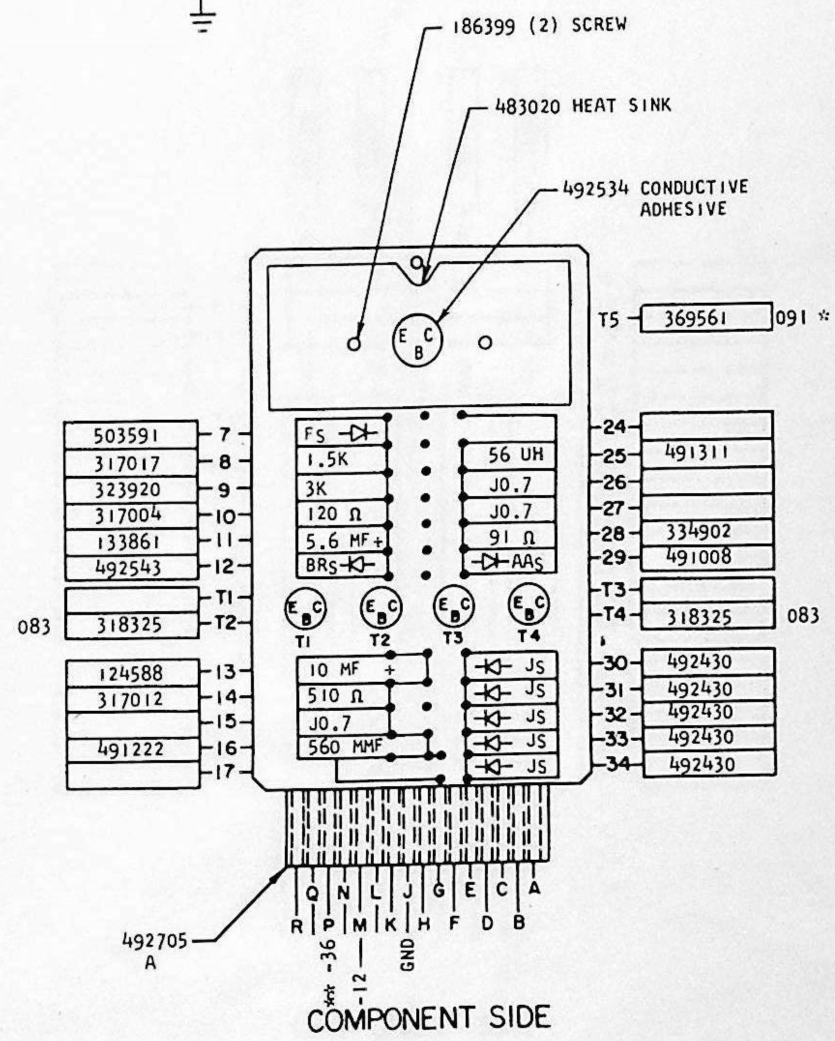


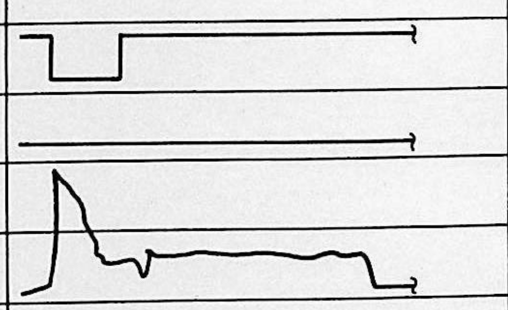


SEQUENCE OF OPERATION

1. H, D, E TIED TOGETHER
2. DOWN OUTPUT AT B, G, T4, T2 OFF, BASE OF T5 GOES TO A MINUS LEVEL AND OFF
3. WITH T5 OFF ITS COLLECTOR IS AT PLUS LEVEL; THIS FORWARD BIAS THE DIODES D30 TO 34 ALLOWING CURRENT TO FLOW

NOTE: FOR -36V USE AS IS, FOR -20V, JUMPER BACK PANEL PINS "P" AND "R"



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B	U	ACTIVATE STORAGE		UP	-5.26	0.24
				DOWN	-7.44	-12.5
G	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
A		+34 →				
A		GROUND →				

DELAY
1. TURN-ON DELAY SHALL BE MEASURED FROM THE 90% POINT OF THE FALL OF THE INPUT PULSE TO THE 90% POINT ON THE RISE OF THE OUTPUT PULSE AS MEASURED ACROSS R_L AND SHALL BE NOT GREATER THAN 200 NANO SECONDS.
2. TURN-OFF DELAY SHALL BE MEASURED FROM THE 10% POINT ON THE RISE OF THE INPUT PULSE TO THE 10% POINT ON THE FALL OF THE OUTPUT PULSE AS MEASURED ACROSS R_L AND SHALL BE NOT GREATER THAN 100 NANO SECONDS.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				
NAME	CARD ASM TSTR- ALLOY- CURRENT DRIVER			
DESIGN			MODEL	SMS
DETAIL	RQ	3-1-62	SCALE	NONE
CHECK	WH	3-1-62	DRAW	LIG 3-17-62
APPRO			CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6 27-62	115599					

729858

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STANDARDS CODE

729859

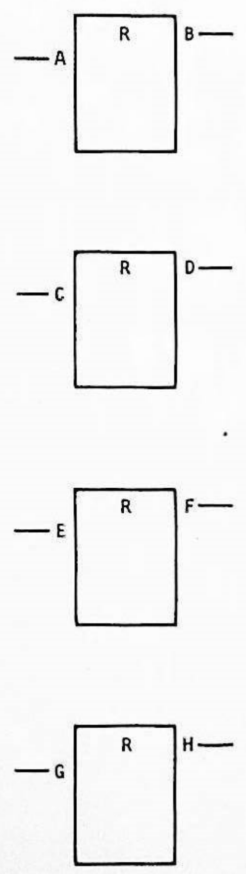
CARD CODE	729859
FP --	

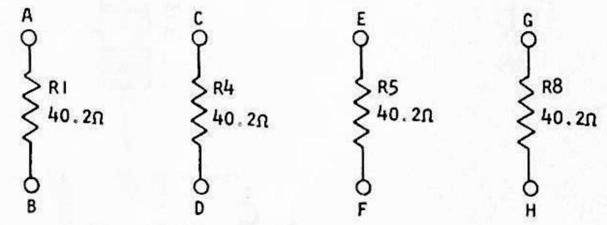
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371453

ALLOY - LOAD RESISTOR - 40.2Ω 2W

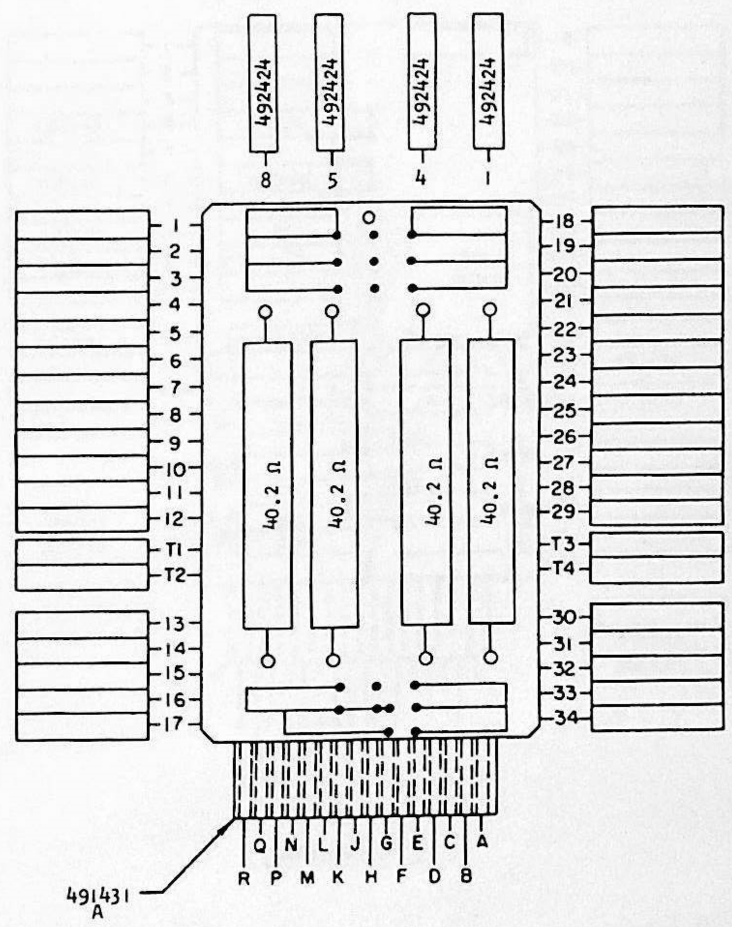
MOUNT CARD ON ONE INCH CENTERS NOTE XIV





APPLICATION

1. USED AS TERMINATING RESISTOR PRINT BUFFER ARRAY



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY LOAD RESISTOR 40.2Ω 2W			6 17-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729859

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STANDARDS CODE

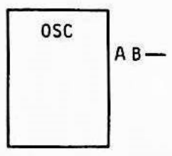
729860

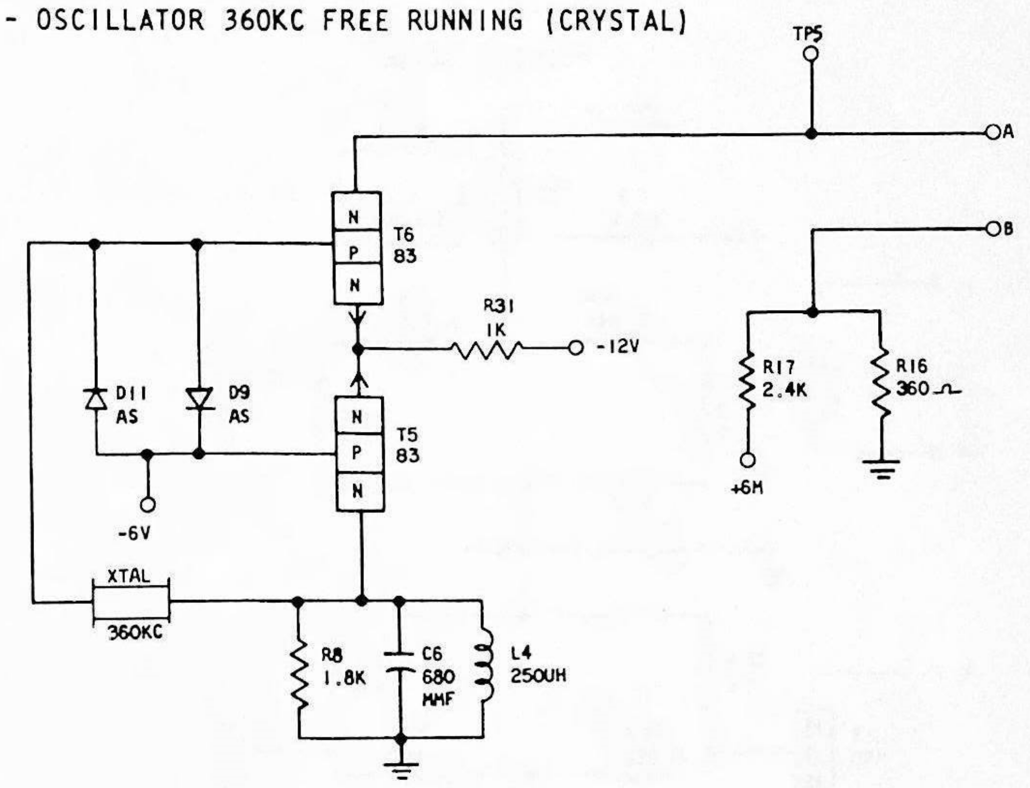
CARD CODE	729860
FT --	

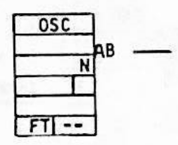
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371405

ALLOY - OSCILLATOR 360KC FREE RUNNING (CRYSTAL)

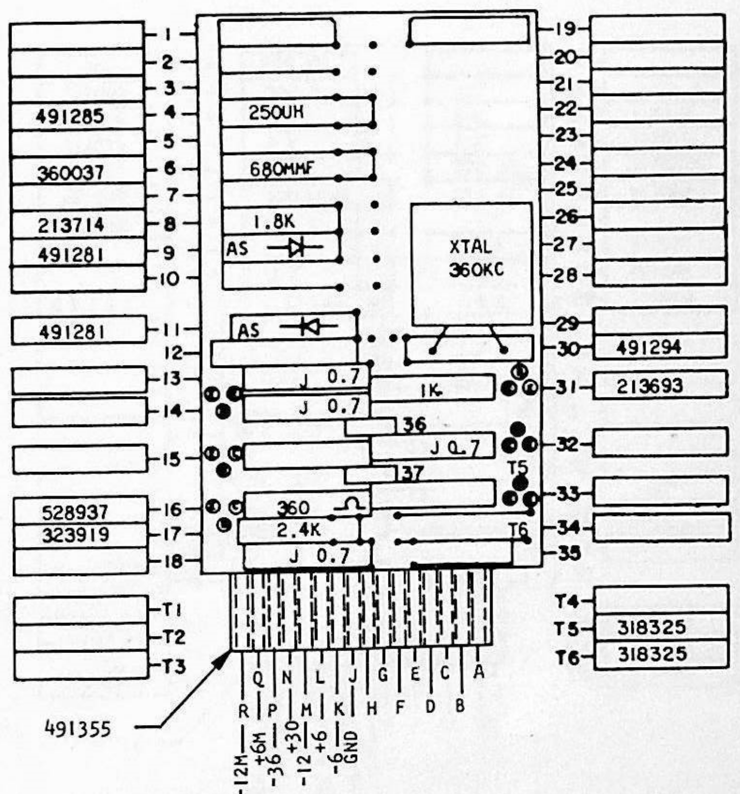




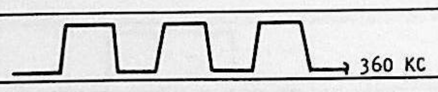


SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A MUST BE TIED TO PIN B



COMPONENT SIDE

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
A		OUTPUT	 360 KC	UP	.697	.86
				DOWN	-.92	-2.04

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY				4-27-62	115599					
OSC. F/R NPN 360KC (CRYSTAL)											
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729860

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STANDARDS CODE	

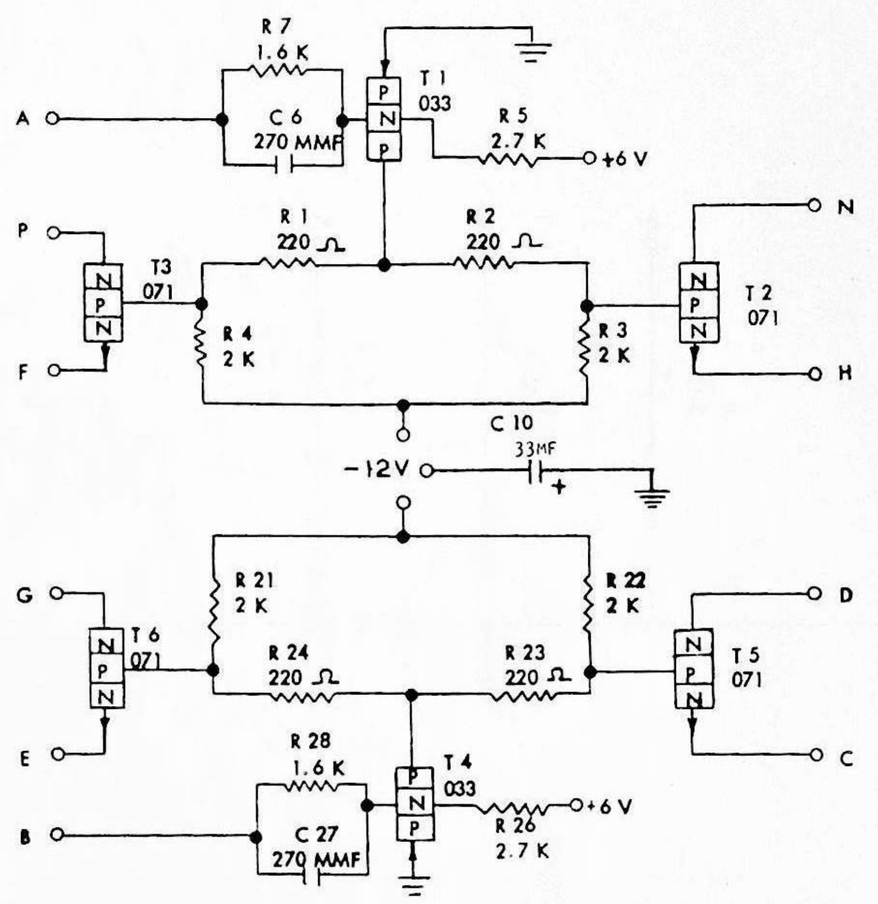
729861

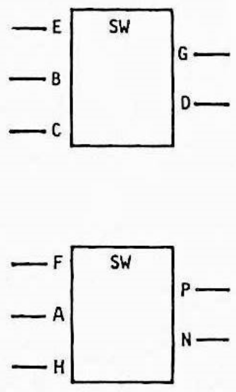
CARD CODE	729861
FW --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371490

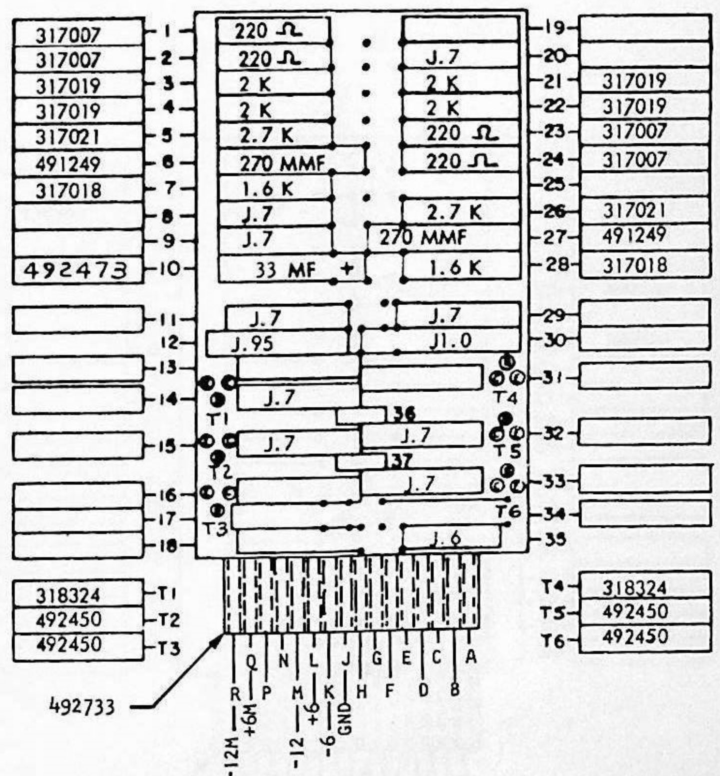
ALLOY - SWITCHES





SEQUENCE OF OPERATION

1. COLLECTORS OF T3, T2, T6, T5 ARE TIED TO +6 THRU A TERMINATING RESISTOR CARD AND THEIR EMITTERS ARE TIED TO CURRENT DRIVER SOURCE CARD THRU WINDINGS IN CORE ARRAY.
2. A DOWN INPUT AT A WILL TURN T1 ON AND T3 OR T2 DEPENDING ON WHICH TRANSISTOR IS SUPPLIED EMITTER CURRENT FROM CURRENT DRIVER CARD.



COMPONENT SIDE

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
A,B	S	INPUT		UP	-.2	+.3
				DOWN	-5.6	-12

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR - ALLOY - SWITCHES				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
-62	115599					

729861

C

STANDARDS CODE	

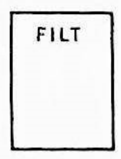
729862

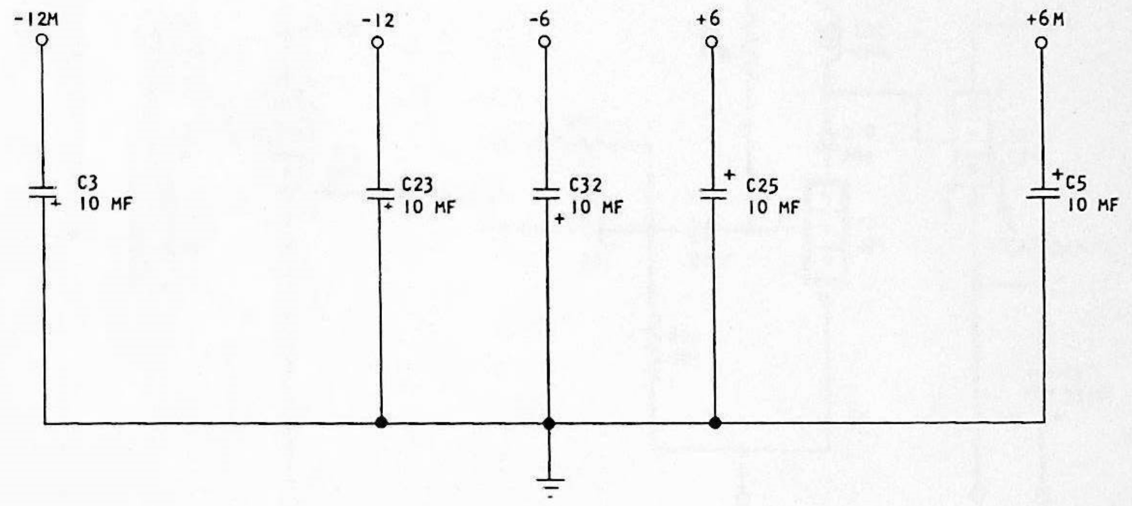
CARD CODE	729862
GJ --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371501

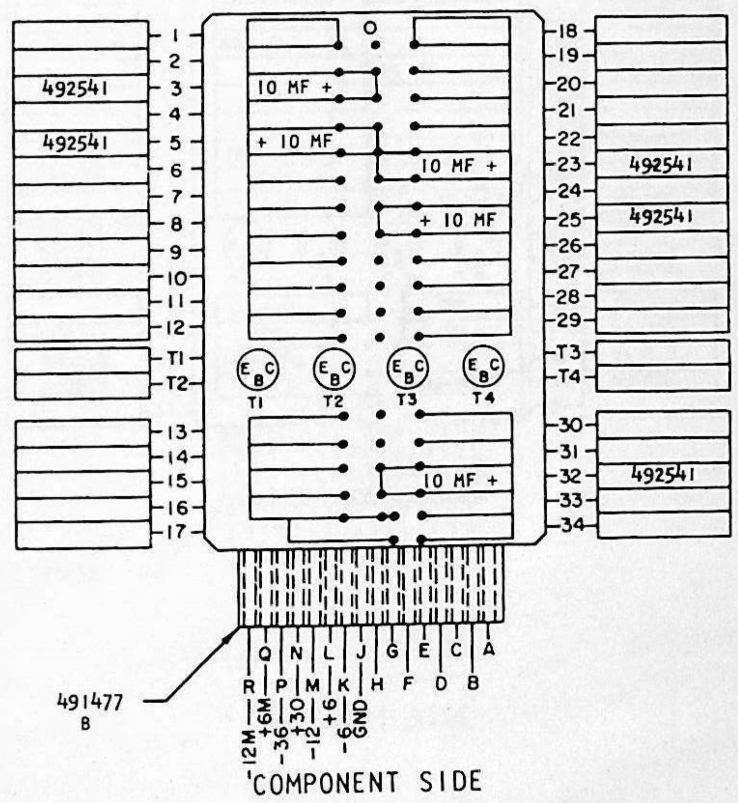
GENERAL PURPOSE FILTER CARD





APPLICATION

1. THIS CARD USED TO FILTER SUPPLY VOLTAGES TO GROUND POTENTIAL



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- GENERAL PURPOSE FILTER CARD				·62	115599					
DESIGN		MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729862

C

STANDARDS CODE

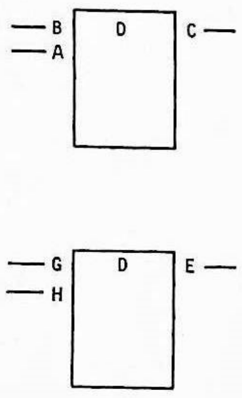
729863

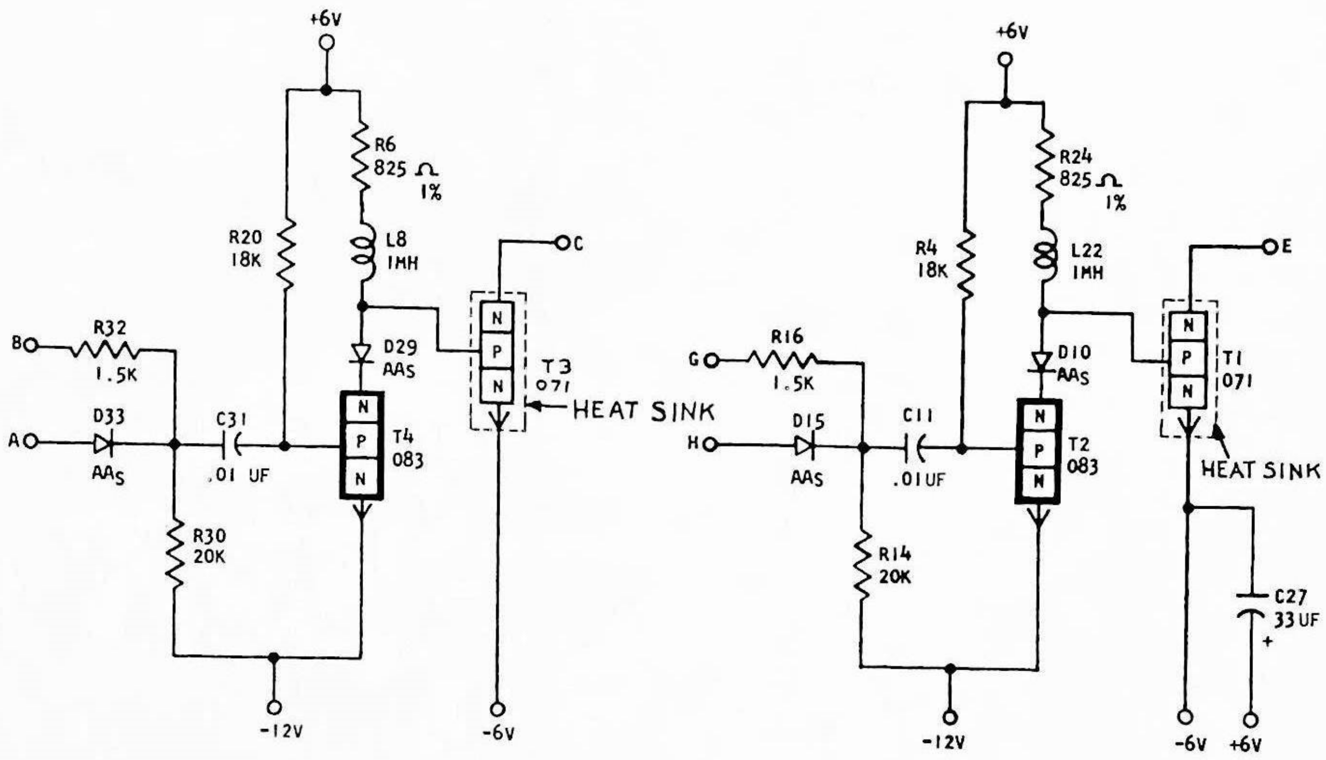
CARD CODE	729863
HN --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371463

ALLOY-DRIVERS, READ WRITE VM

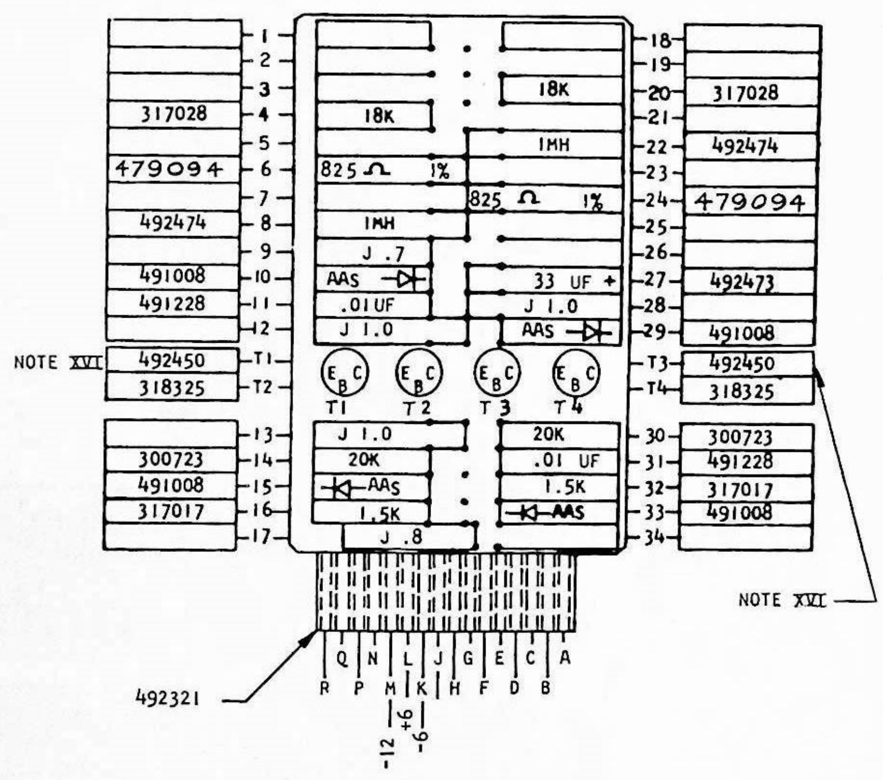




SEQUENCE OF OPERATION

1. T4, T2 ON; T3, T1 OFF
2. DOWN INPUT AT B 0.5 U SEC BEFORE DOWN INPUT AT A TURNS T4 OFF T3 ON
3. WAVE FORM AT C OR E NOT SHOWN AS THE FUNCTION OF T1 AND T3 IS CURRENT OUTPUT
4. DELAY

	MAXIMUM
TURN ON	.3 USEC
TURN OFF	.37 USEC



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B,G	U	INPUT GATE		UP	-0.54	0.24
				DOWN	-7.44	-12.5
A,H	U	INPUT SET		UP	0.0	-0.1
				DOWN	-11.5	-12.5
INPUT OF	TO	BASE T1, T3		UP	-5.8	
				DOWN	-11.8	

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

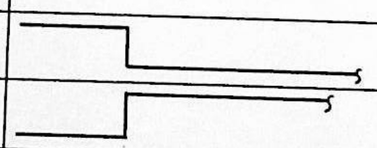
INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY DRIVERS - READ WRITE VM			[illegible]-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729863

C

SEQUENCE OF OPERATION

1. WHEN THE INPUT IS UP, THE TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. WHEN THE INPUT IS DOWN, THE TRANSISTOR IS ON, THE OUTPUT IS UP
3. ALL OUTPUTS MUST BE COLLECTOR LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
E,F, H,D	T	INPUT		UP	1.44	6.24
				DOWN	-.74	-6.24
G,C, P,A	U	OUTPUT		UP	-.54	.24
				DOWN	-7.44	-12.48

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.25
TURN OFF	0.10	0.40

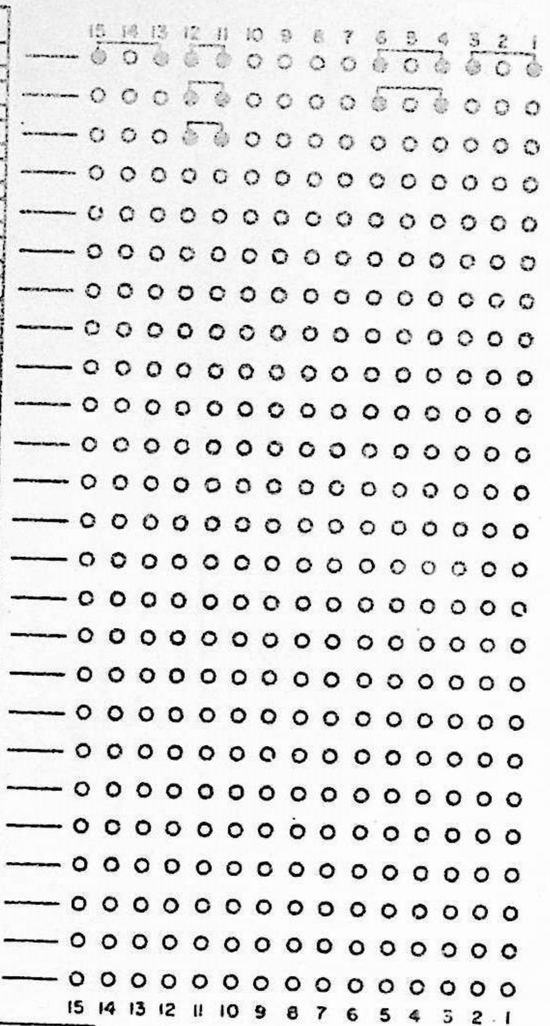
CARD CODE	STANDARDS CODE	370982
JF **	2-7046	

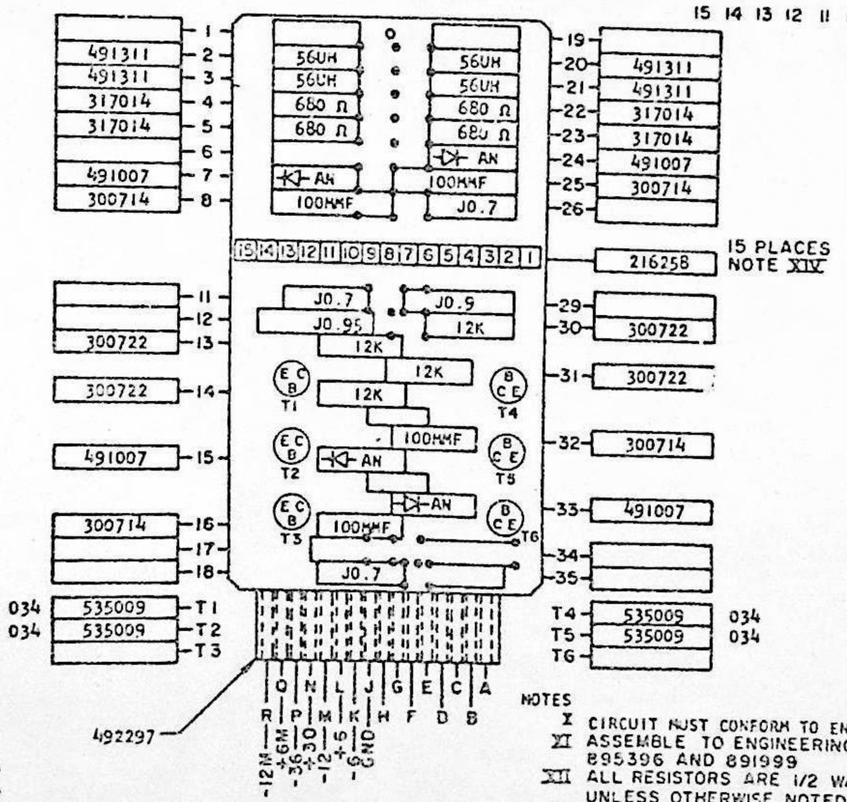
CTDL HIGH SPEED ONE WAY PNP
FIELD REPLACEMENT

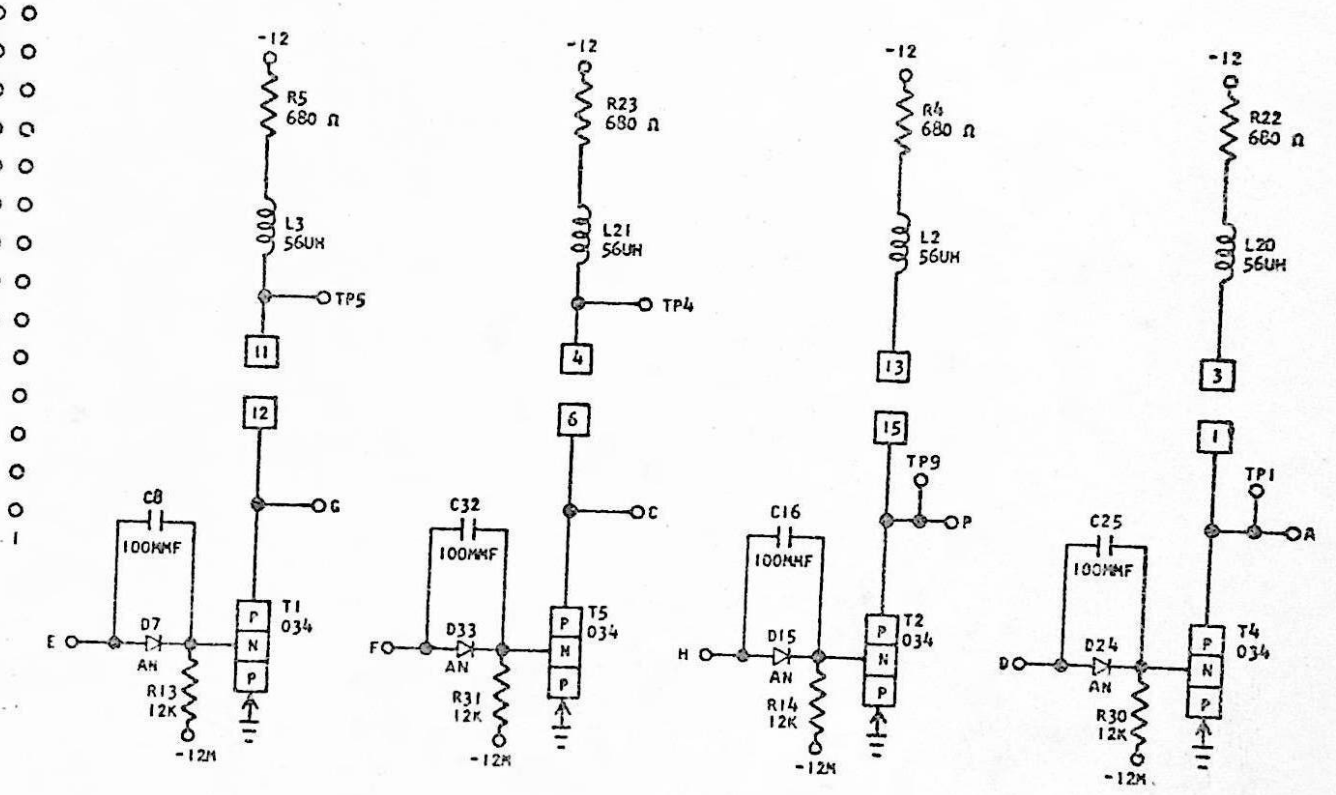
DISCONTINUED

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC
CTDL HIGH SPEED 1 WAY PNP-ALL LOADS	VP	371576	891576
CTDL HIGH SPEED 1 WAY PNP-TWO LOADS	VN	371577	891576
CTDL HIGH SPEED 1 WAY PNP-ONE LOAD	VA	371578	891576
CTDL HIGH SPEED 1 WAY PNP-NO LOAD	—	371579	891576

CAP CONFIGURATION







NOTES

I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891576

XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999

XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED

XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491296

XIV REFERENCE - 216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H D Hanford	7-6-60

370982

INTERNATIONAL BUSINESS MACHINES CORP			
NAME	CARD ASM TSTR - CTDL HIGH SPEED 1 WAY PNP		
DESIGN		TYPE	SMS
DETAIL		SCALE	NONE
CHECK	TH 7-1-60	DRAW	MDE 7-8-60
APPRO	GES 7-3-60	CHECK	7-11-60

DATE	CHANGE NO	APPROVAL	DATE	CHANGE NO.	APPROVAL
8-4-60	109642	GWB			
9-27-60	D110084	IWB			
12-1-60	110517	IWB			

DEVELOPMENT NO. X0665

370982

SEQUENCE OF OPERATION

1. ANY INPUT UP, TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, THE TRANSISTOR IS ON, THE OUTPUT IS UP
3. ALL OUTPUTS MUST BE COLLECTOR LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
B,F,D, C,G,E	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
H,N,A	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48

DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

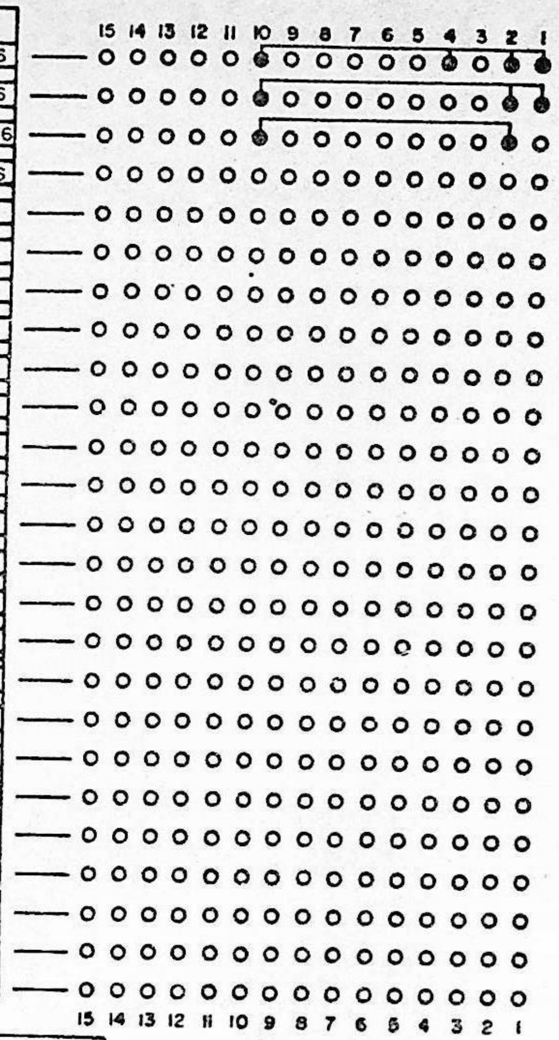
CARD CODE	STANDARDS CODE	370983
JG **	2-7045	

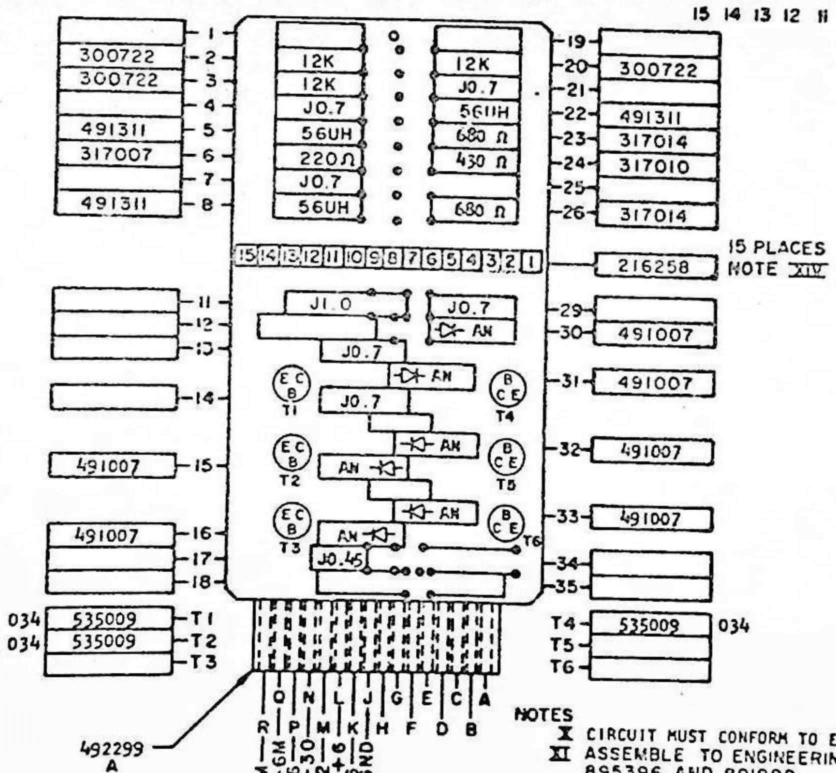
CTDL HIGH SPEED 2 WAY AND PNP
FIELD REPLACEMENT

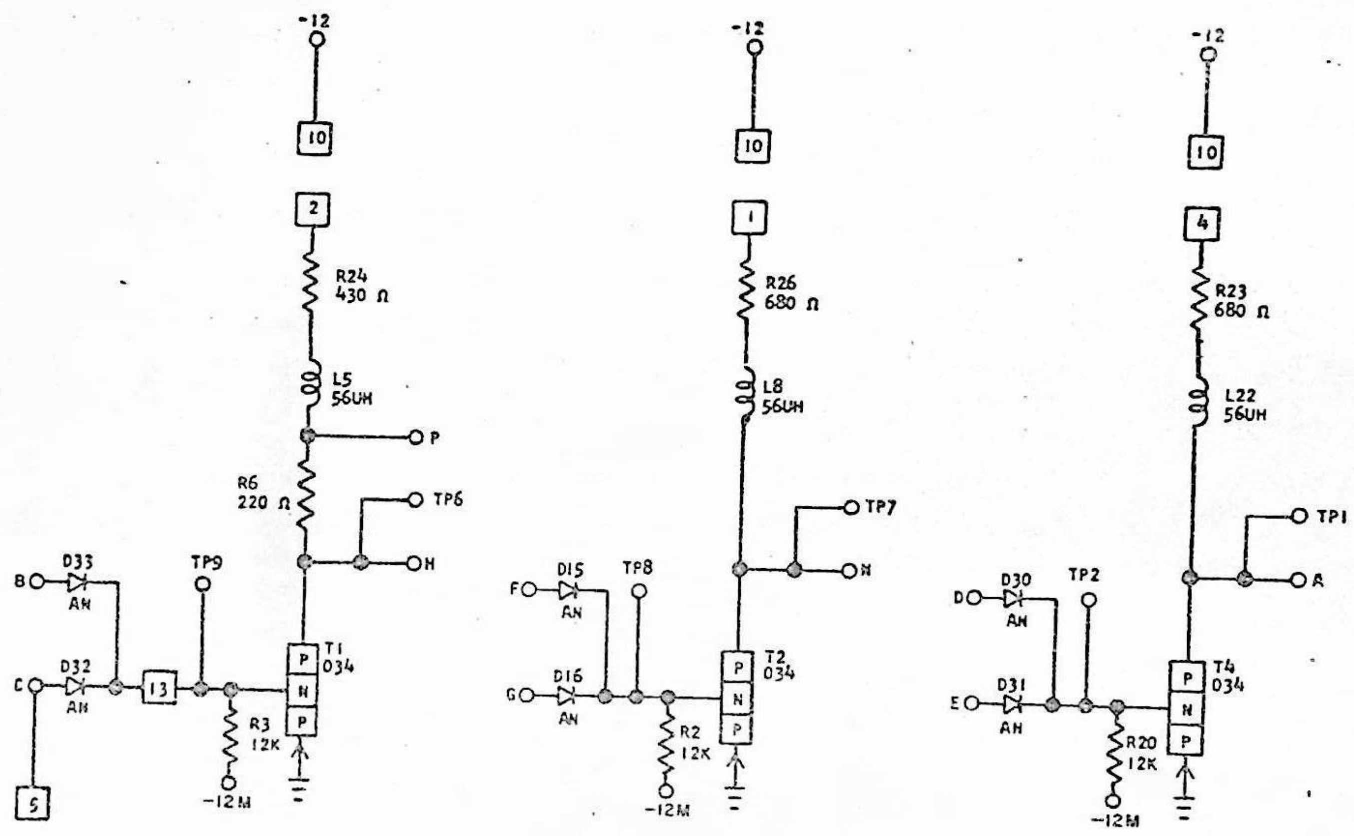
DISCONTINUED

CAP CONFIGURATION

CIRCUIT NAME	CAP CODE	ASM. NO	TEST SPEC
CTDL 2 WAY AND PNP-ALL LOADS	WW	371580	891576
CTDL 2 WAY AND PNP-2 LOADS	VW	371581	891576
CTDL 2 WAY AND PNP-1 LOAD	VV	371582	891576
CTDL 2 WAY AND PNP-NO LOAD	–	371583	891576







NOTES

XI CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891576
XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED
XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491298
XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H D Harford	7-6-60

370983

INTERNATIONAL BUSINESS MACHINES CORP						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- CTDL HIGH					8-4-60	105642					X0664
SPEED 2 WAY AND PNP						9-27-60	D110084	IWB				
DESIGN			TYPE	SMS		12-1-60	110517	IWB				
DETAIL			SCALE	NONE		2-20-61	D110931	IWB				
CHECK	TBJ	8-1-60	DRAW	NCE	7-6-60							
APPR	SES	8-3-60										

370983

SEQUENCE OF OPERATION

1. ANY INPUT UP, TRANSISTOR OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, TRANSISTOR ON, THE OUTPUT IS UP
3. INPUTS ON EXTENDER INPUTS MUST BE DOWN IN COINCIDENCE WITH INPUTS ON CARD FOR UP OUTPUT
4. BOTH OUTPUTS MUST BE COLLECTOR LOADED
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
D,E, F	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
N	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
				UP		
				DOWN		
A,B, C	T'	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
H	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
G		EXTENDER INPUT		UP	+6	
				DOWN	0.0	

DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

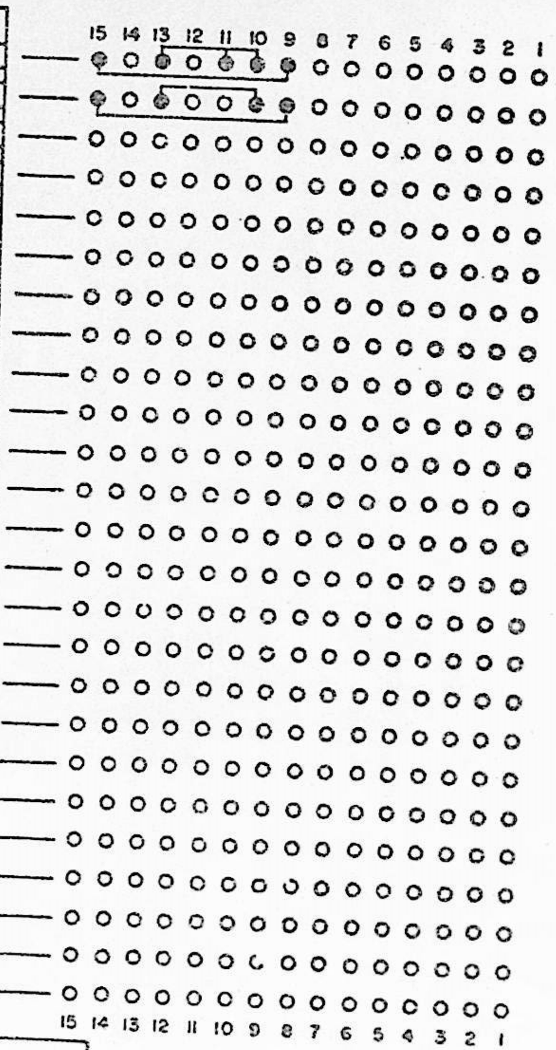
CARD CODE	STANDARDS CODE	370984
JH ☆☆	2-7045	

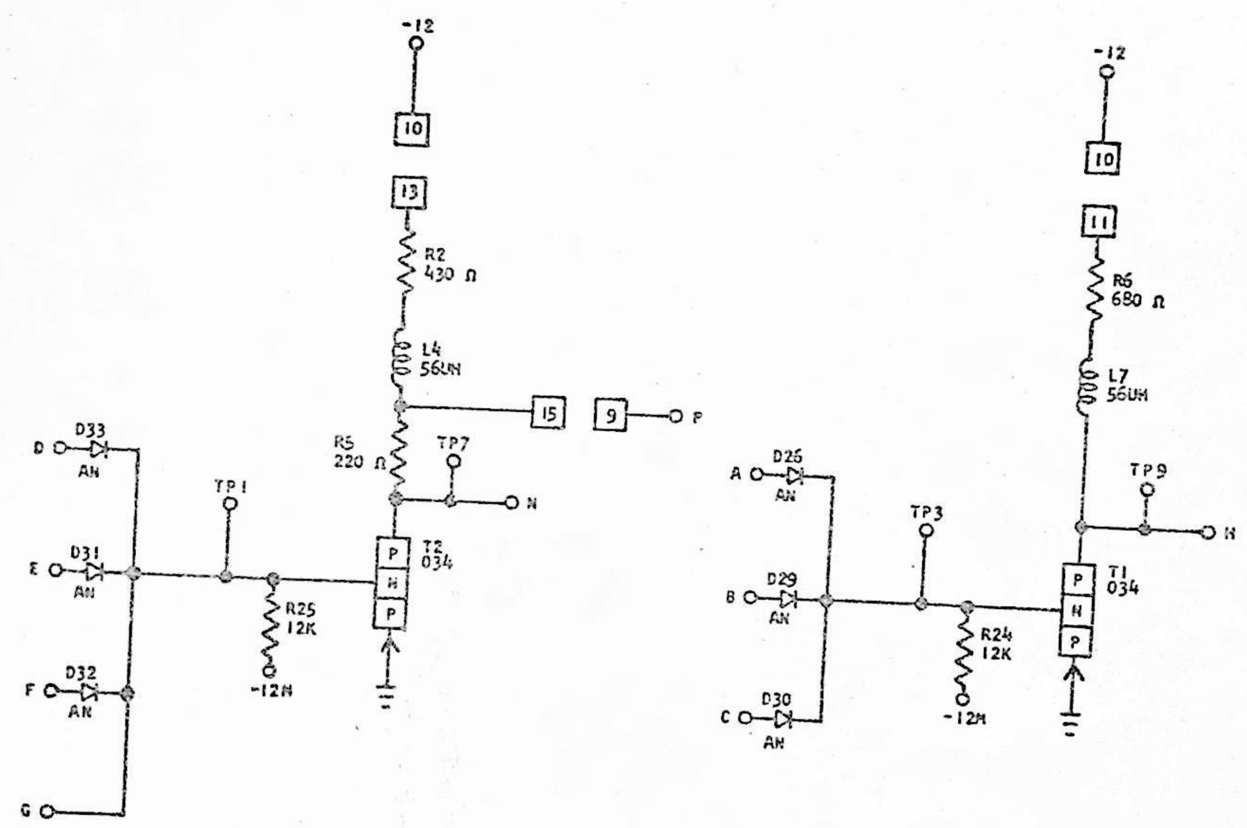
CTDL HIGH SPEED 3 WAY AND PNP
FIELD REPLACEMENT

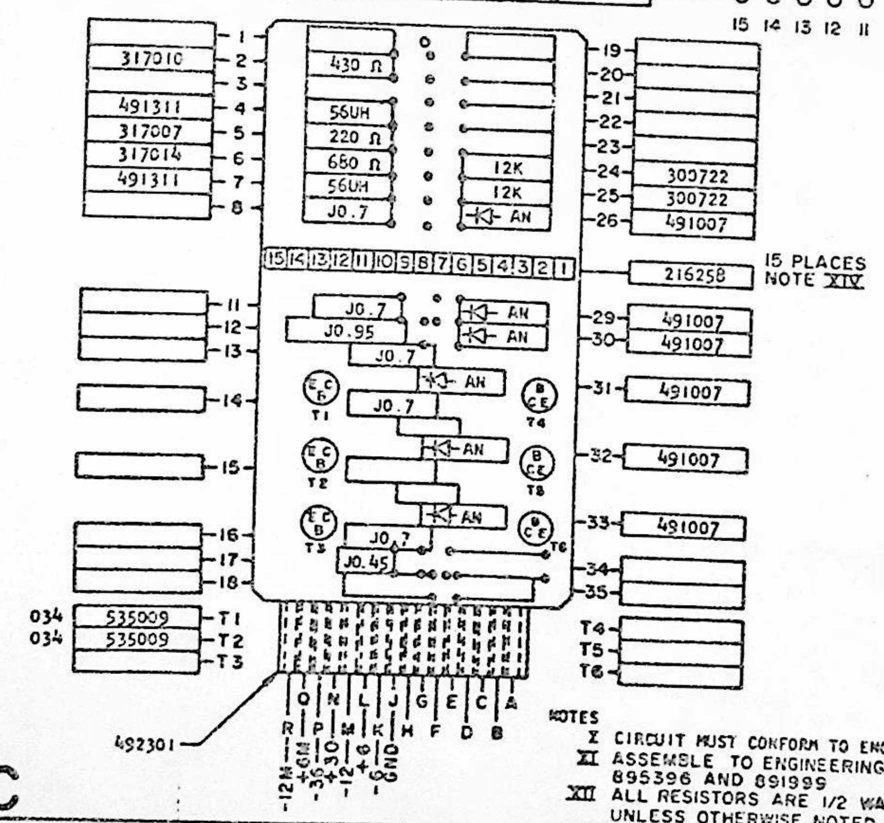
DISCONTINUED

CIRCUIT NAME	CAP CODE	ASM. NO	TEST SPEC
CTDL 3 WAY AND PNP-ALL LOADS	WV	371584	891576
CTDL 3 WAY AND PNP-1 LOAD	VU	371585	891576
CTDL 3 WAY AND PNP-NO LOAD	—	371586	891576

CAP CONFIGURATION







NOTES
- I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891576
- XI ASSEMBLE TO ENGINEERING SPECIFICATION 895396 AND 891999
- XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED
- XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491296
- XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H E Hosford	7-6-60

370984

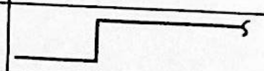
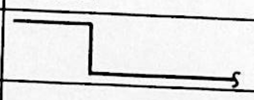
INTERNATIONAL BUSINESS MACHINES CORP.		
NAME	CARD ASM TSTR- CTDL HIGH SPEED 3 WAY AND PNP	
DESIGN	TYPE	SMS
DETAIL	SCALE	NONE
CHECK TB.J 8-2-60	DRAWN	HDE 7-7-60
APPRO BES 8-2-60	CHECK	7-11-60

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
8-4-60	109642	GWP				X0659
9-27-60	D110064	IWB				
12-1-60	110517	IWB				

370984

SEQUENCE OF OPERATION

1. IF THE INPUT IS UP, THE TRANSISTOR IS ON, THE OUTPUT IS DOWN
2. IF THE INPUT IS DOWN, THE TRANSISTOR IS OFF, THE OUTPUT IS UP
3. ALL TRANSISTORS MUST BE COLLECTOR LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
E,F,H,D	U	INPUTS		UP	-5.26	+.24
				DOWN	-7.44	-12.48
G,C,P,A	T	OUTPUTS		UP	+1.44	+6.24
				DOWN	-5.26	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.20
TURN OFF	0	0.30

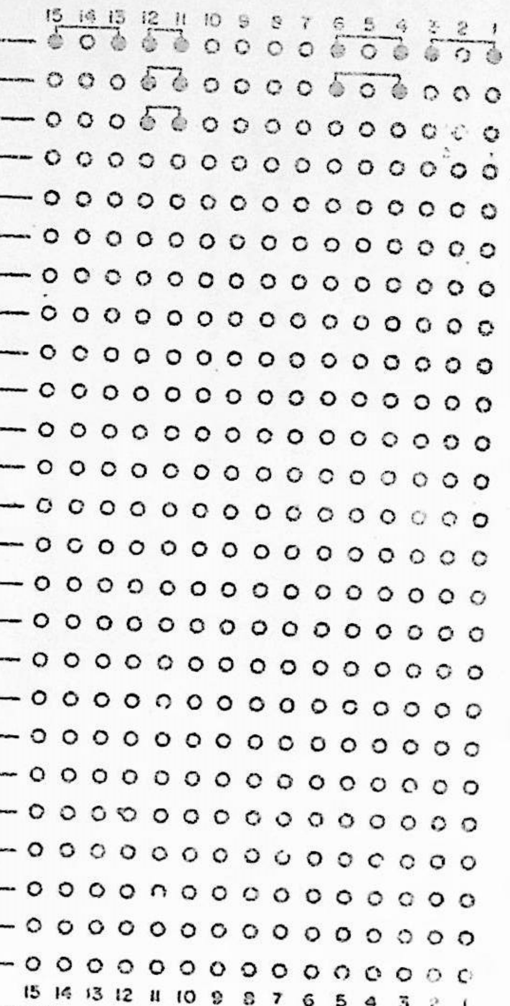
CARD CODE	STANDARDS CODE	370985
JJ **	2-7045	

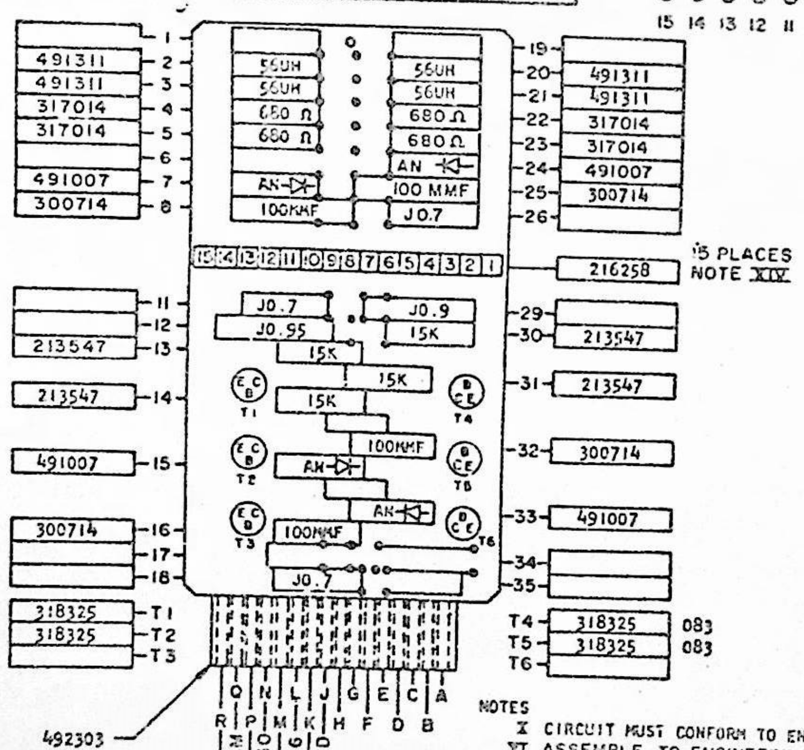
DISCONTINUED

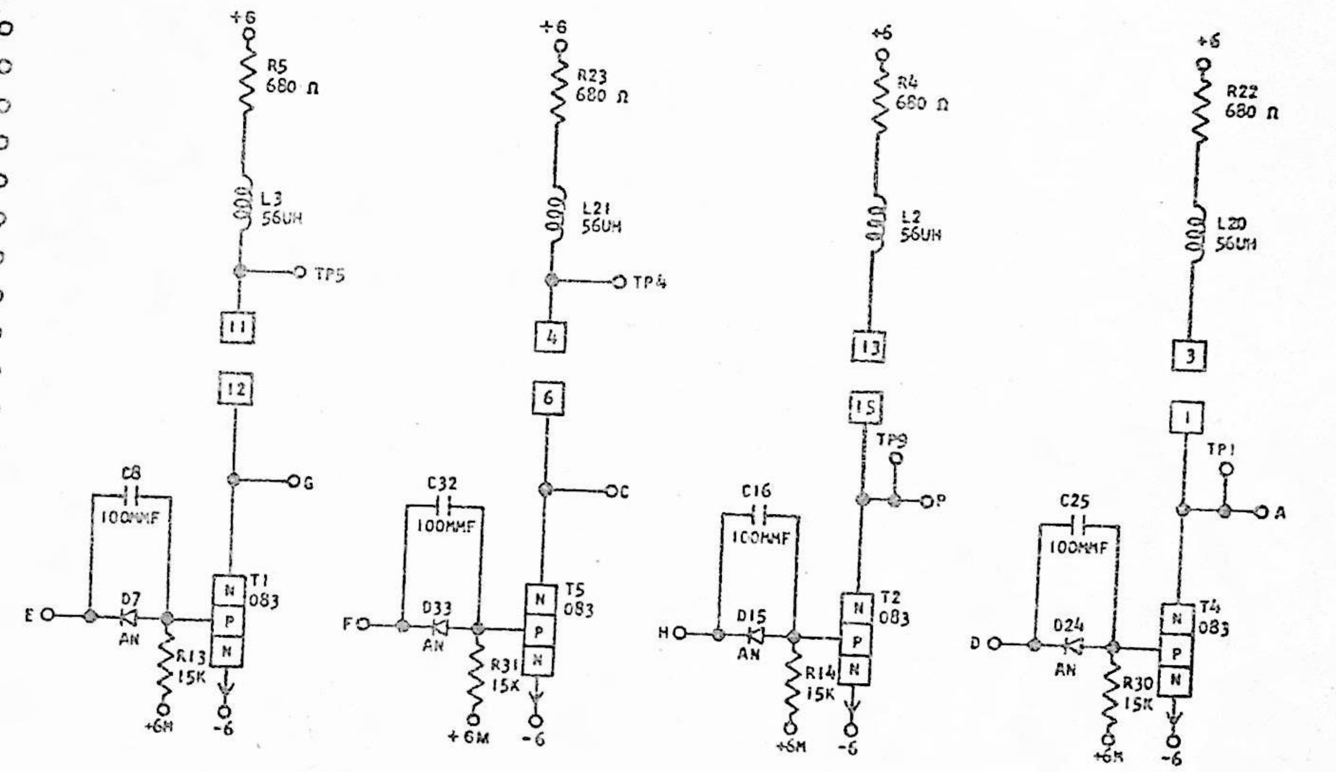
CTDL HIGH SPEED ONE WAY NPN
FIELD REPLACEMENT

CIRCUIT NAME	CAP CODE	ASM NO	TEST SPEC
CTDL HIGH SPEED 1 WAY NPN-ALL LOADS	VP	371587	891576
CTDL HIGH SPEED 1 WAY NPN-2 LOADS	VH	371588	891576
CTDL HIGH SPEED 1 WAY NPN-ONE LOAD	VA	371589	891576
CTDL HIGH SPEED 1 WAY NPN-NO LOAD	—	371590	891576

CAP CONFIGURATION







NOTES
I CIRCUIT MUST CONFORM TO ENGINEERING SPECIFICATION 891576
VI ASSEMBLE TO ENGINEERING SPECIFICATION 895395 AND 891999
XII ALL RESISTORS ARE 1/2 WATT AND ±5% UNLESS OTHERWISE NOTED
XIII "J" IN BLOCK DENOTES BARE WIRE JUMPER, 491295
XIV REFERENCE-216259 MALE CONTACT STRIP TO BE USED AS REQUIRED TO PROGRAM DESIRED CAP CODE

C

DPD CIRCUIT & PACKAGING STANDARD	
APPROVAL	DATE
H. D. Hanford	7-6-60

370985

INTERNATIONAL BUSINESS MACHINES CORP				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL HIGH SPEED ONE WAY NPN			8-4-60	F05642					X0663
DESIGN		TYPE	SMS	9-27-60	D110084	IWB				
DETAIL		SCALE	NONE	12-1-60	110517	IWB				
CHECK	7-6-60	DRAW	7-8-60							
APPROVAL										

370985

STANDARDS CODE

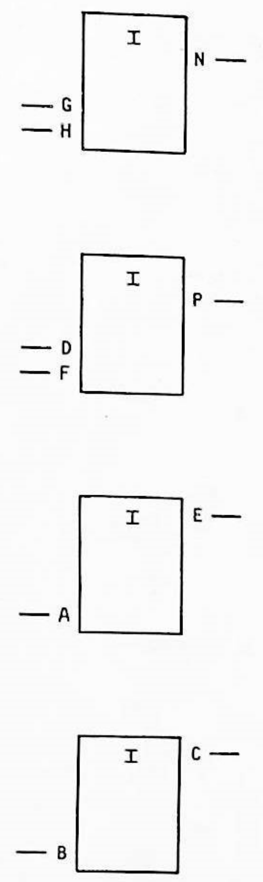
729879

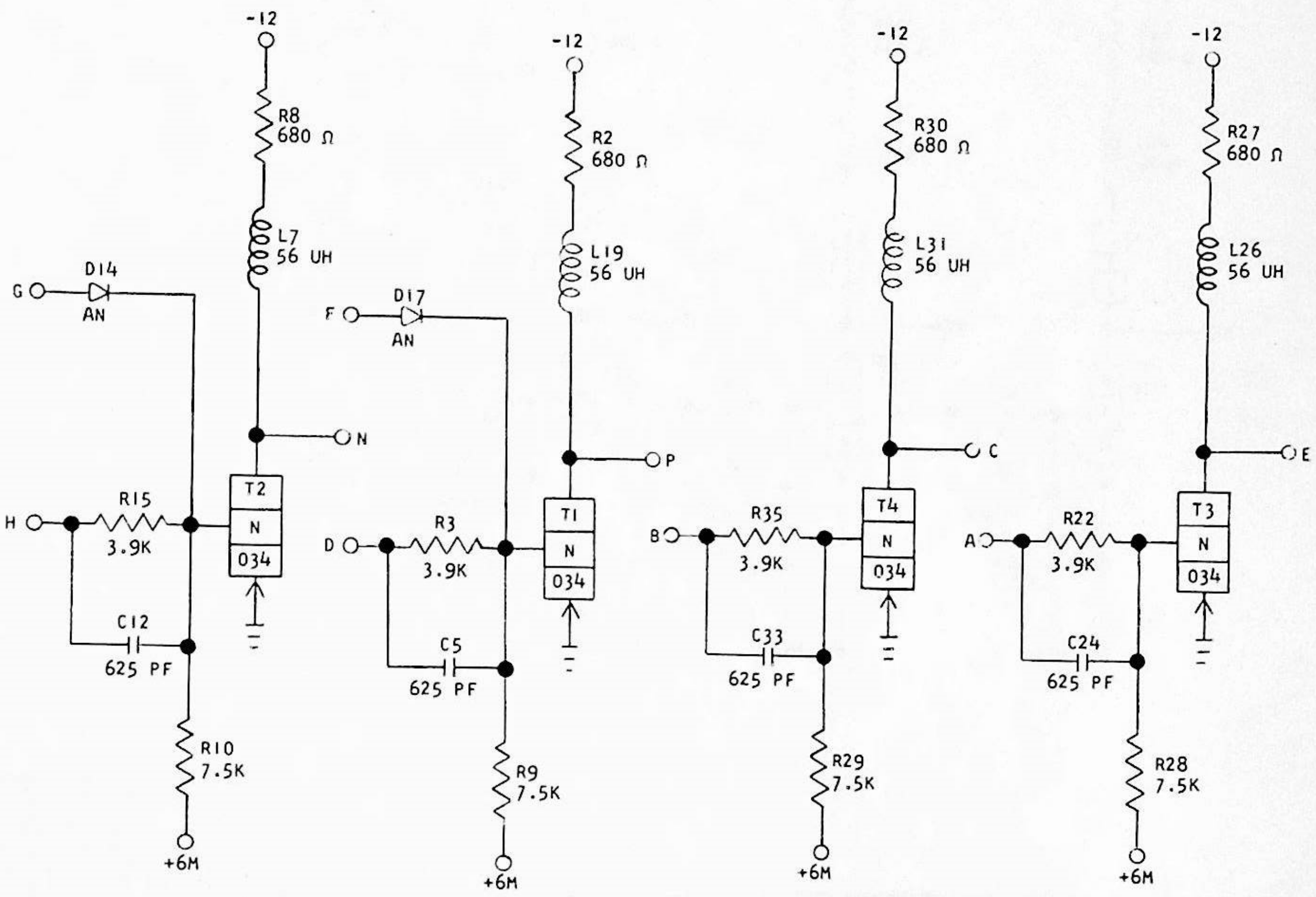
CARD CODE	729879
JL VB	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371077

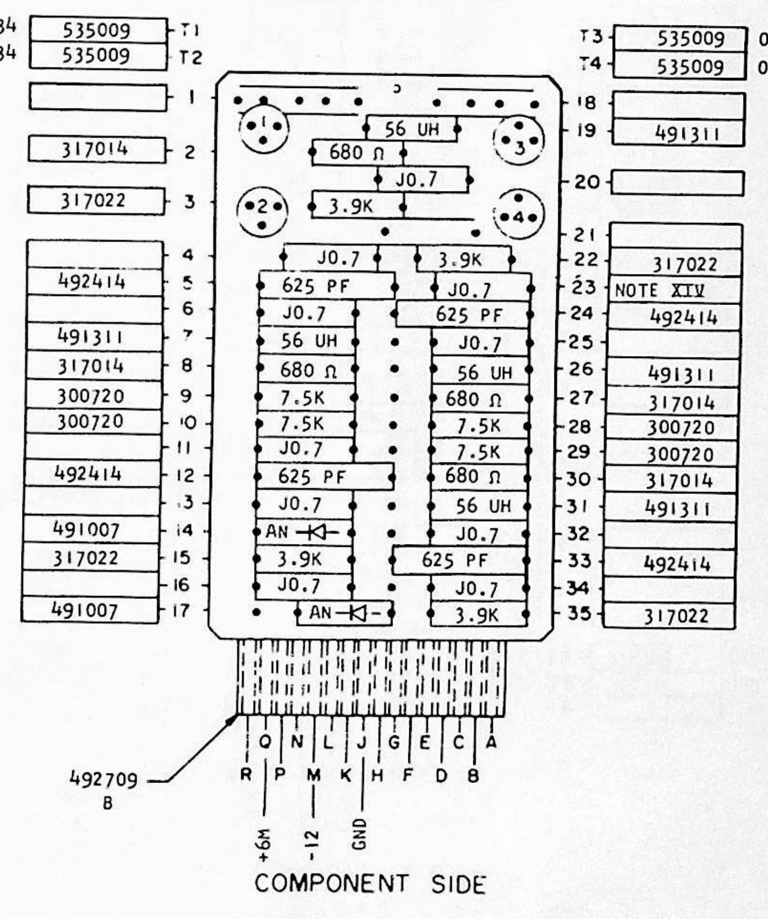
CTDL LOGIC INVERTER PNP ALL LOADS





SEQUENCE OF OPERATION

1. FOR AN UP OUTPUT THE INPUT MUST BE DOWN
2. THE GATING DIODE IS PROVIDED ONLY TO RESET A LOGIC INVERTER LATCH. IT SHOULD NOT BE USED AS A SIGNAL INPUT SINCE IT IS POSSIBLE FOR THE SIGNAL INPUT TO OVERRIDE THE GATE
3. IN APPLICATIONS USING BOTH INPUTS ON CIRCUITS 1 AND 2 THE GATE (PINS G OR F) AND SIGNAL INPUTS MUST BE DOWN FOR AN UP OUTPUT
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
H,D	U	INPUT SIGNAL		UP	-0.54	+0.24
				DOWN	-7.44	-12.48
G,F	T	INPUT GATE		UP	+1.44	+6.24
				DOWN	-0.74	-6.24
N,P	U	OUTPUT		UP	-0.54	+0.24
				DOWN	-7.44	-12.48
A,B, H,D	U	INPUT		UP	0.54	+0.24
				DOWN	-7.44	-12.48
E,C, P,N	U	OUTPUT		UP	-0.54	+0.24
				DOWN	-7.44	-12.48

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	-0.05	-0.15
TURN OFF	+0.05	+0.55

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR - CTDL				
	LOGIC INVERTER PNP ALL LOADS				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
[illegible]-62	115599					

729879

C

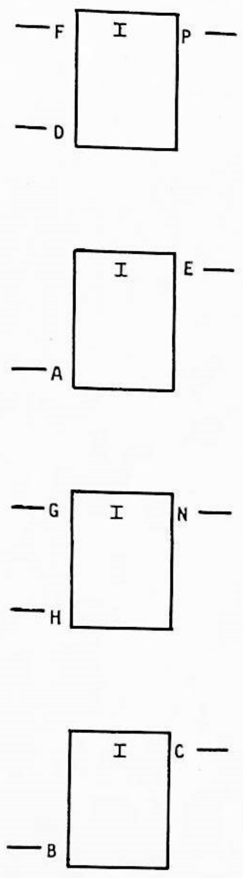
STANDARDS CODE
729880

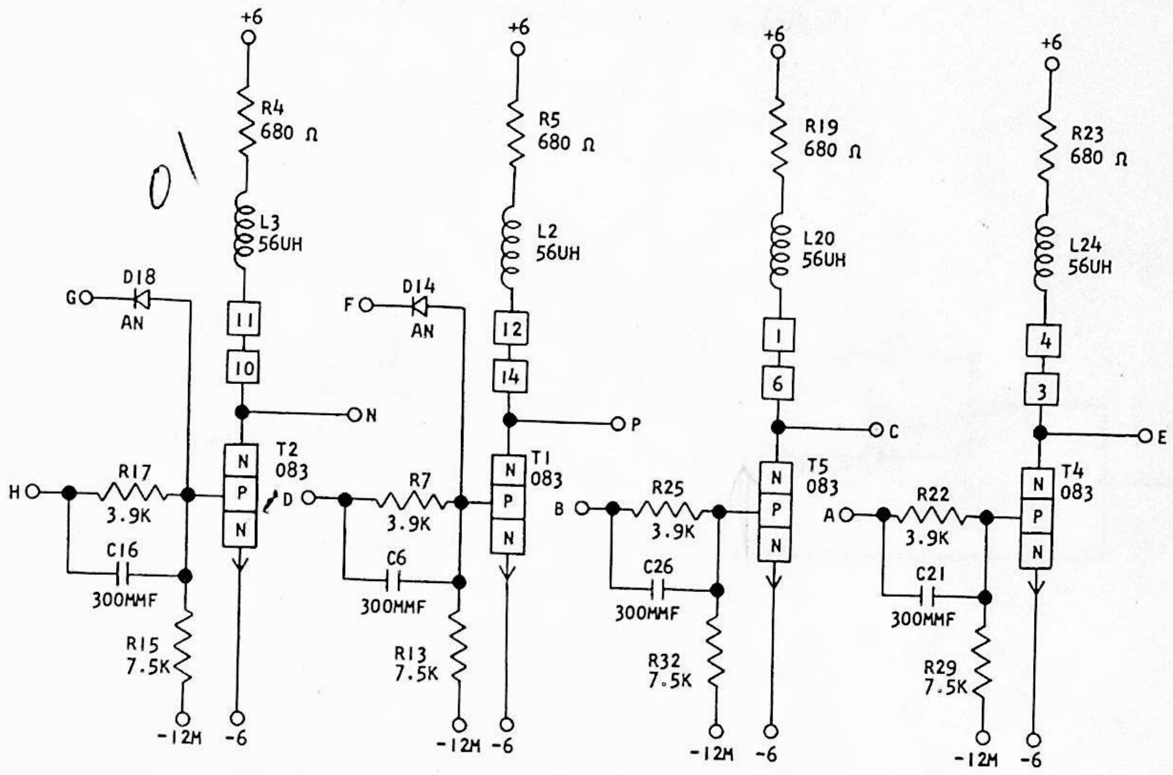
CARD CODE	729880
JM VB	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371079

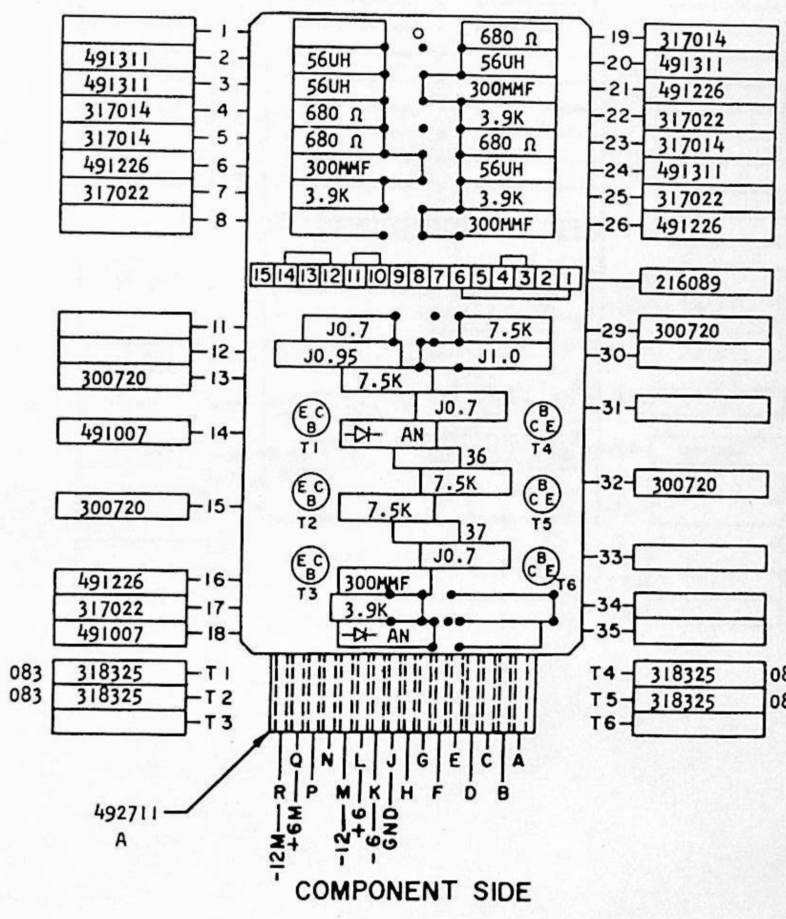
CTDL LOGIC INVERTER NPN ALL LOADS





SEQUENCE OF OPERATION

1. GATE AND SIGNAL UP, TRANSISTOR ON, DOWN OUTPUT.
2. GATE OR SIGNAL DOWN,TRANSISTOR OFF, UP OUTPUT.
3. INPUT DOWN, TRANSISTOR OFF, OUTPUT UP.
4. INPUT UP, TRANSISTOR ON, OUTPUT DOWN.
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
H,D	T	INPUT SIGNAL		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
G,F	U	INPUT GATE		UP	-5.26	+0.24
				DOWN	-7.44	-12.48
N,P	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
B,A	T	INPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
C,E	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	-0.05	0
TURN OFF	-0.05	+0.40

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-CTDL				. -62	115599					
LOGIC INVERTER NPN ALL LOADS										
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

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STANDARDS CODE

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CARD CODE	729881
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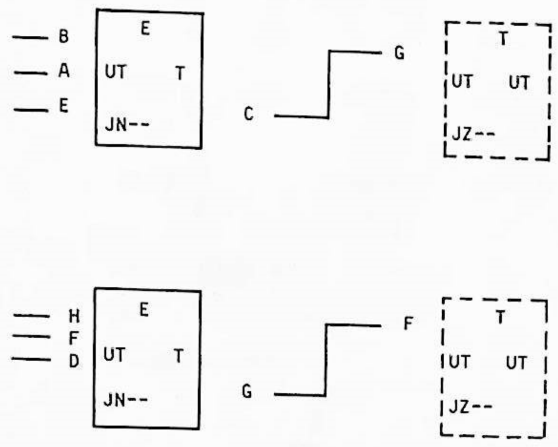
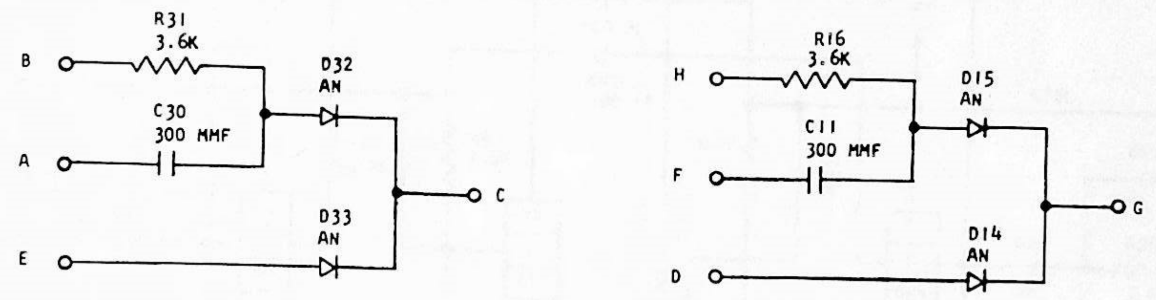
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371081

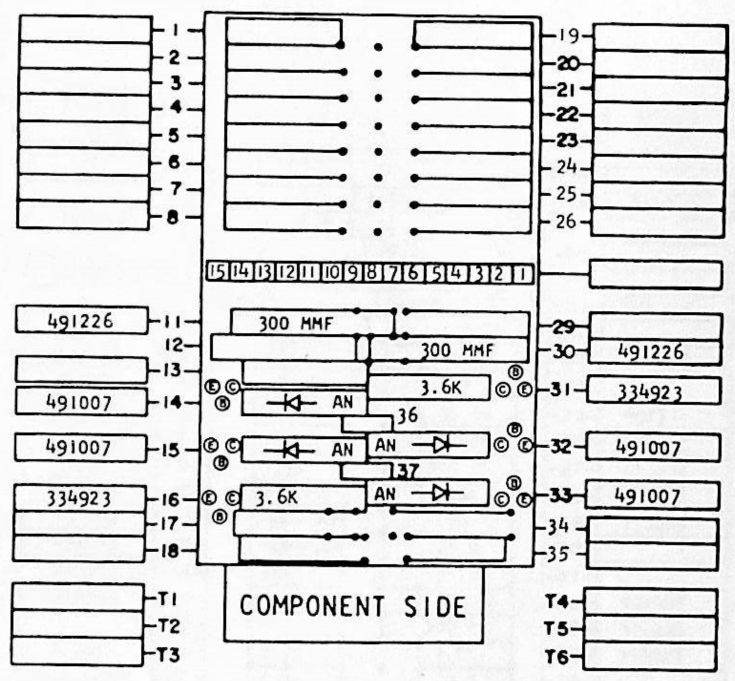
CTDL - TRIGGER GATE EXTENDER





SEQUENCE OF OPERATION

1. AN UP INPUT AT PINS E, D OR AN UP INPUT AT BOTH B, H AND A, F PROVIDES A POSITIVE OUTPUT AT PIN C, G.



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B, H	U	GATE INPUT		UP	-5.3	0.2
				DOWN	-7.4	-12.5
A, F	U	AC SET INPUT		UP	-5.3	0.2
				DOWN	-7.4	-12.5
E, D	T	DC SET INPUT		UP	1.44	6.2
				DOWN	-0.74	-6.2
C, G		EXTENDER OUTPUT		UP	1.44	6.2
				DOWN	-0.2	-0.2

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL- TRIGGER GATE EXTENDER			7-62	115599					
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW LIG	3-17-62							
APPRO		CHECK								

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STANDARDS CODE

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CARD CODE	729882
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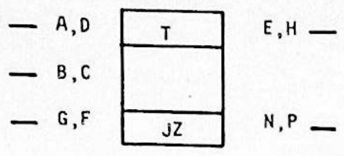
REFERENCE DRAWING

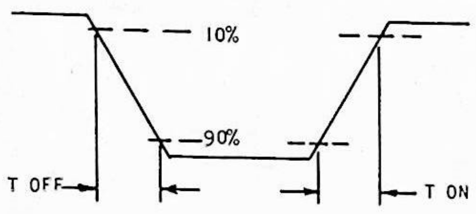
SEE PRODUCTION DRAWING 371082



CTDL TRIGGER NO 2

DELAY - USEC

TYPICAL INVERTER AND EF OUTPUT WAVEFORM

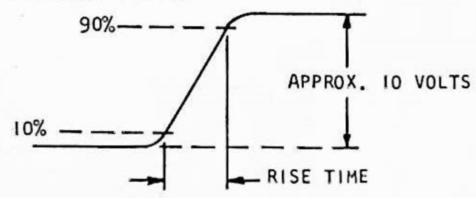


INVERTER DELAY	MINIMUM	MAXIMUM
T OFF	0.15	0.8
T ON	0.10	0.3

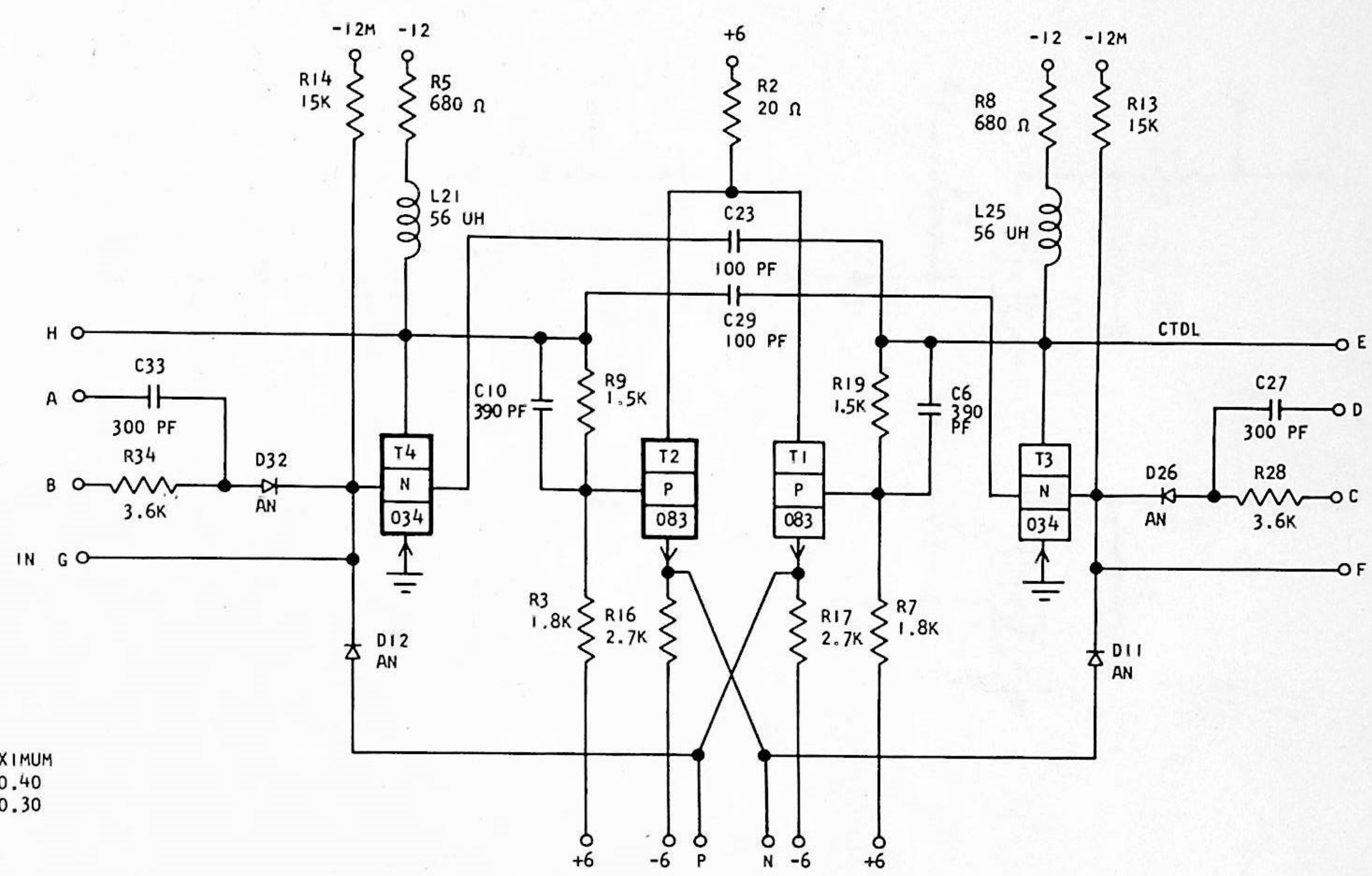
EF DELAY	MINIMUM	MAXIMUM
T OFF	0.05	0.1
T ON	0.10	0.4

THE FOLLOWING DELAY INFORMATION APPLIES WHEN THE AC TRIGGERING INPUT PULSE HAS A RISE TIME OF 0.45 USEC. (SEE FOLLOWING FIGURE)

TRIGGERING PULSE

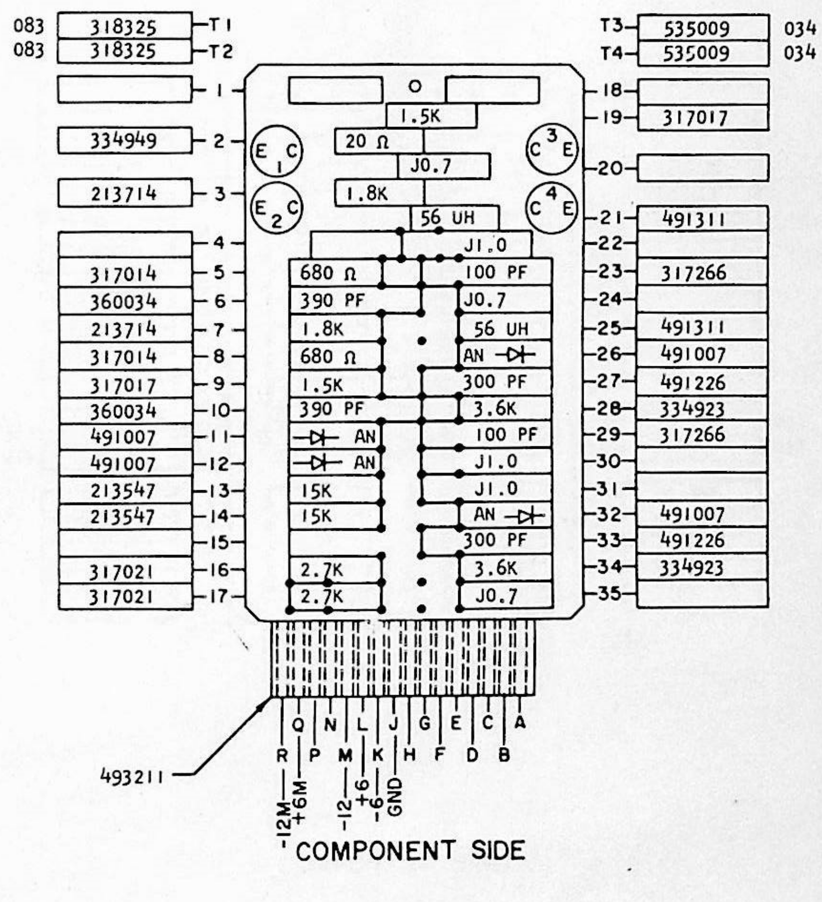


	MINIMUM	MAXIMUM
FROM AC SET TO INVERTER OUTPUTS	0.10	0.40
FROM AC SET TO EF OUTPUTS	0.10	0.30



SEQUENCE OF OPERATION

1. T2 & T4 ON, T1 & T3 OFF
2. PIN B MUST BE CONDITIONED TO AN UP LEVEL 3.75 U SEC BEFORE A POSTIVE SHIFT IS APPLIED TO PIN A TO GIVE AN UP OUTPUT AT PINS E & P AND A DOWN OUTPUT AT PINS H & N. T2 &T4 ARE NOW OFF AND T1 & T3 ON.
3. TO FLIP THE TRIGGER TO ORIGINAL STATE PIN C & D MUST BE CONDITIONED AS WERE PINS A & B ABOVE.
4. COLLECTIVE PULLOVER CAN BE USED ON PINS E & H TO GIVE AN UP OUTPUT.
5. A (JN --) EXTENDER CARD PERMITS ADDITIONAL INPUTS AT PINS G & F TO CONTROL THE TRIGGER.
6. IF SET OR RESET IS ACCOMPLISHED THROUGH PINS G OR F, THE MINIMUM PULSE WIDTH IS 0.5 USEC.



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,D	T	A.C. SET		UP	-0.5	0.2
				DOWN	-7.4	-12.4
B	U	GATE		UP	-0.5	0.2
				DOWN	-7.4	-12.4
C	U	GATE		UP	-0.5	0.2
				DOWN	-7.4	-12.4
E	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2
H	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2
N	T	OUTPUT		UP	1.4	3.1
				DOWN	0.7	-5.2
P	T	OUTPUT		UP	1.4	3.1
				DOWN	0.7	-5.2

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL TRIGGER NO 2				4-27-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

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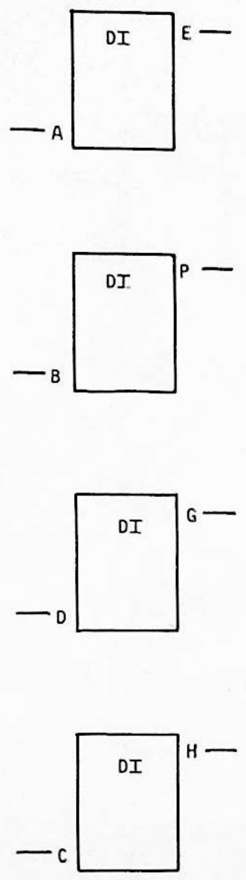
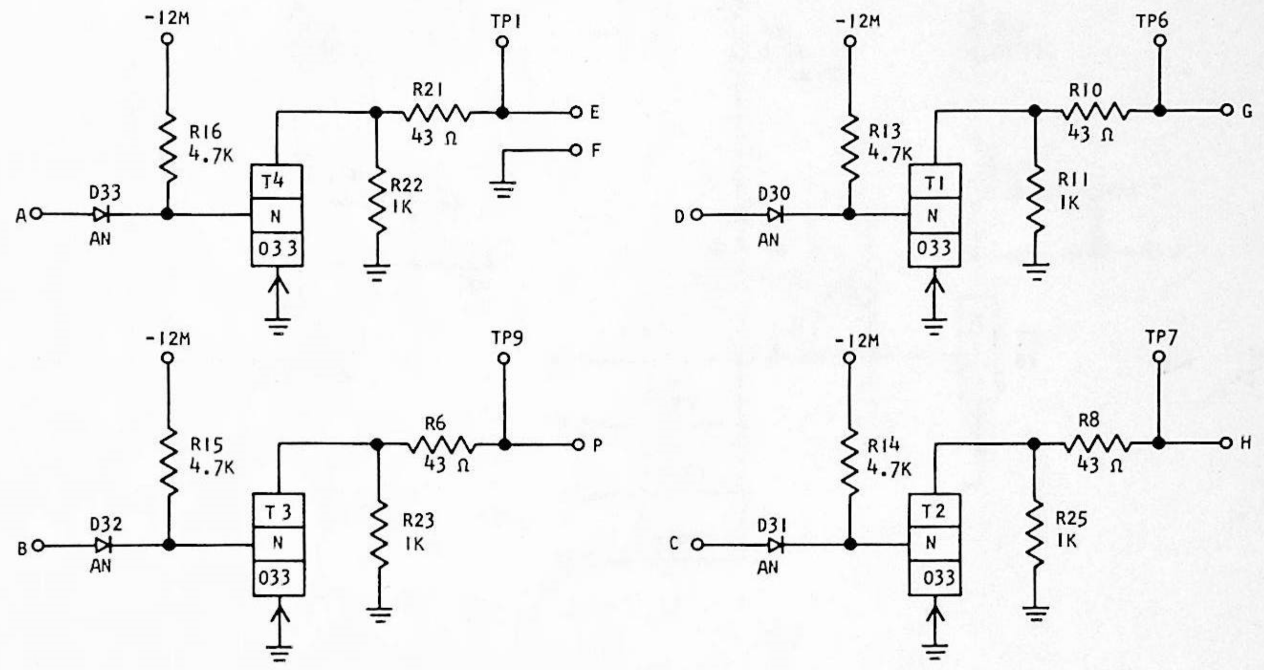
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371546

ALLOY - INDICATOR DRIVER 40 MA

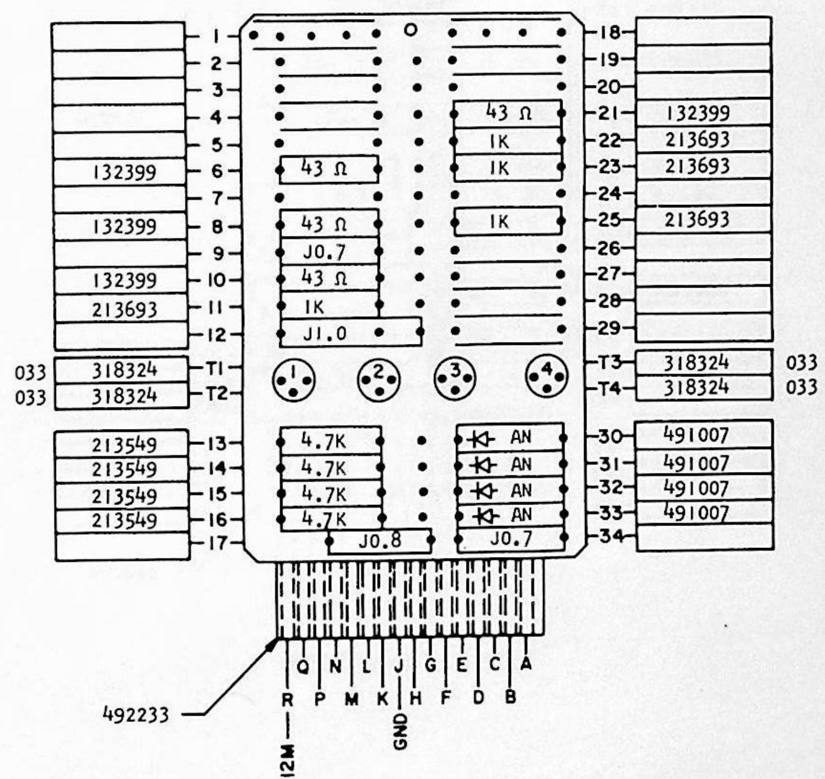




SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
A,D, B,C	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
E,G, P,H	U	OUTPUT		UP	-0.54	0.24
				DOWN		-10



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- ALLOY- INDICATOR DRIVER (40 MA)			/ , -62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

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CARD CODE	729884
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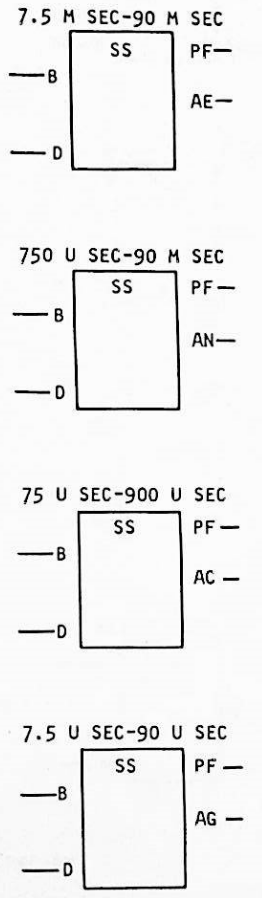
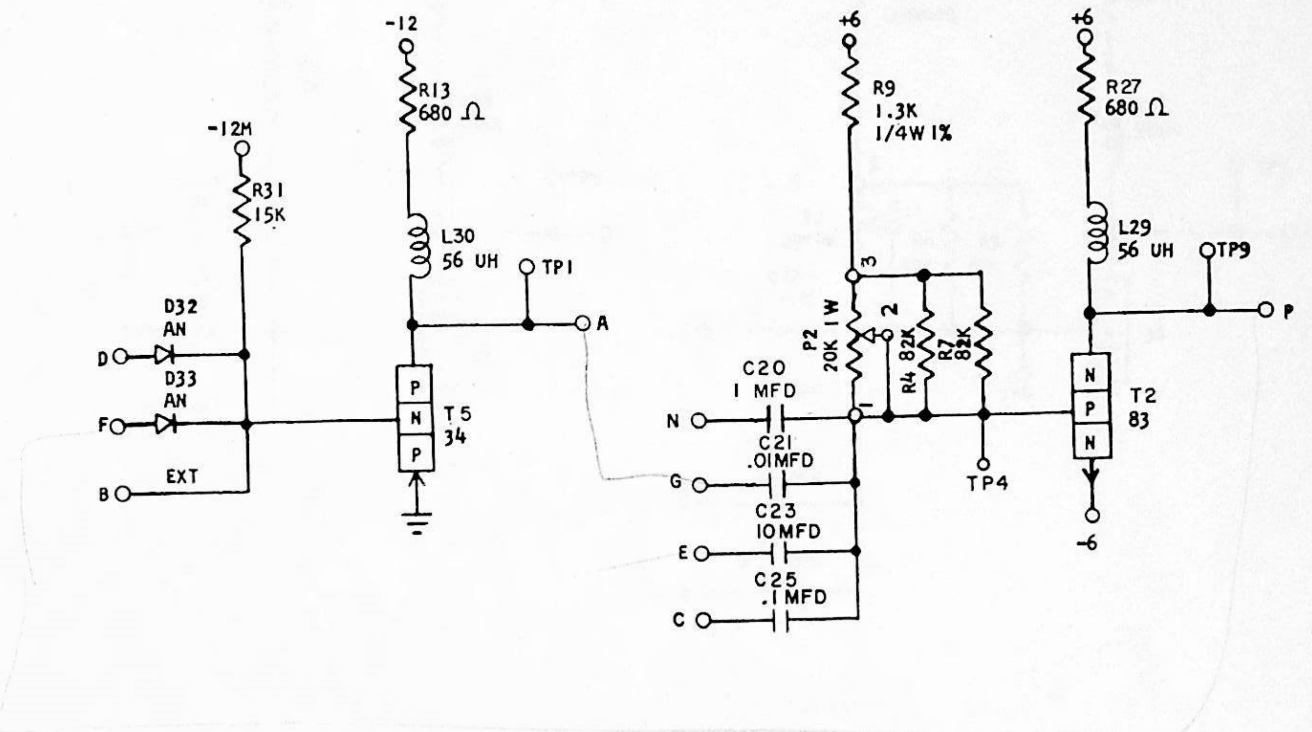
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371591

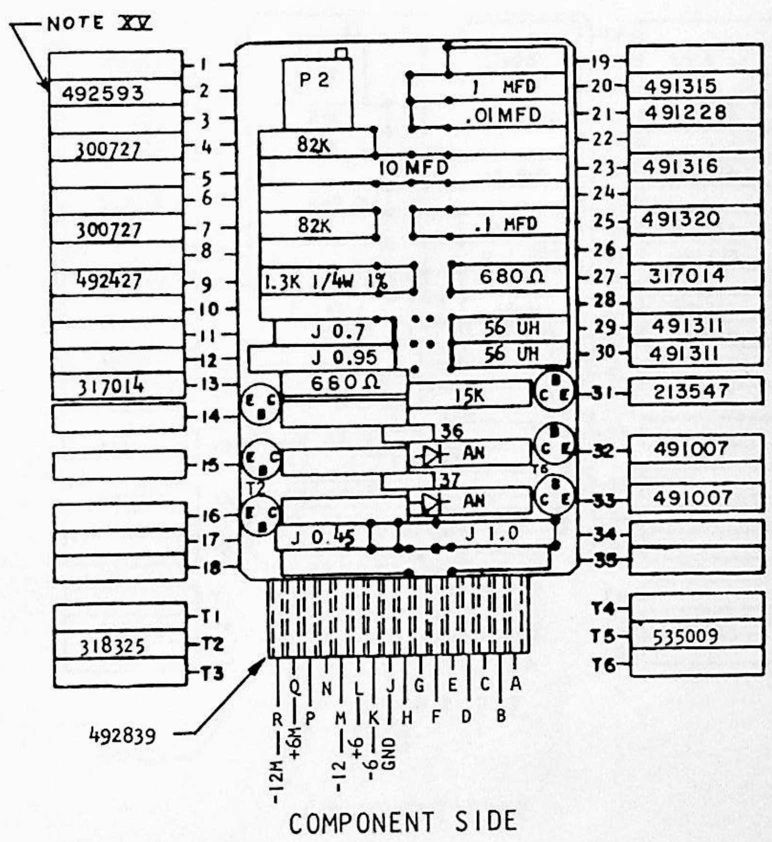
CTDL SINGLE SHOT "T" INPUT





SEQUENCE OF OPERATION

1. T2, T2 ON; P TIED TO F FOR LATCH BACK AND A TO EITHER N,G, E OR C
2. POSITIVE GOING INPUT TO D, T2, T5 OFF
3. R.C. NETWORK DETERMINES LENGTH OF TIME T2 OFF
4. UP INPUT ON EXTENDER CARD WILL GIVE SAME SEQUENCE



PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
D	T	INPUT		UP	1.4	6.2
				DOWN	-0.7	-6.2
B		EXTENDER INPUT		UP	-6	
				DOWN	-12	
F	T	INPUT		UP	1.4	6.2
				DOWN	-0.7	-6.2
P	T	OUTPUT		UP	1.4	6.2
				DOWN	-5.46	-6.2
A	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5
T2 BASE		SWITCH LEVEL		-5.8 -6		

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TSTR - CTDL SINGLE SHOT "T" INPUT			6 27 -62	115599					729884
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

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STANDARDS CODE

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CARD CODE	729885
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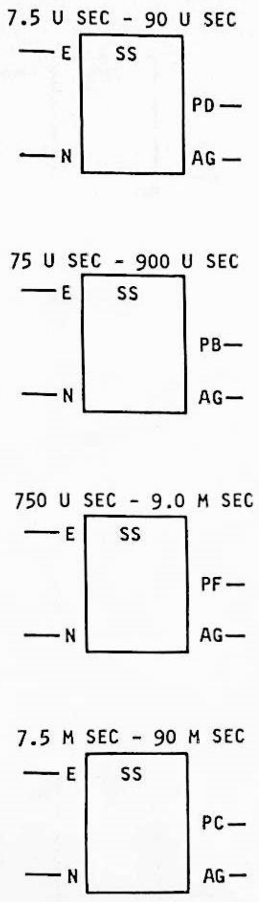
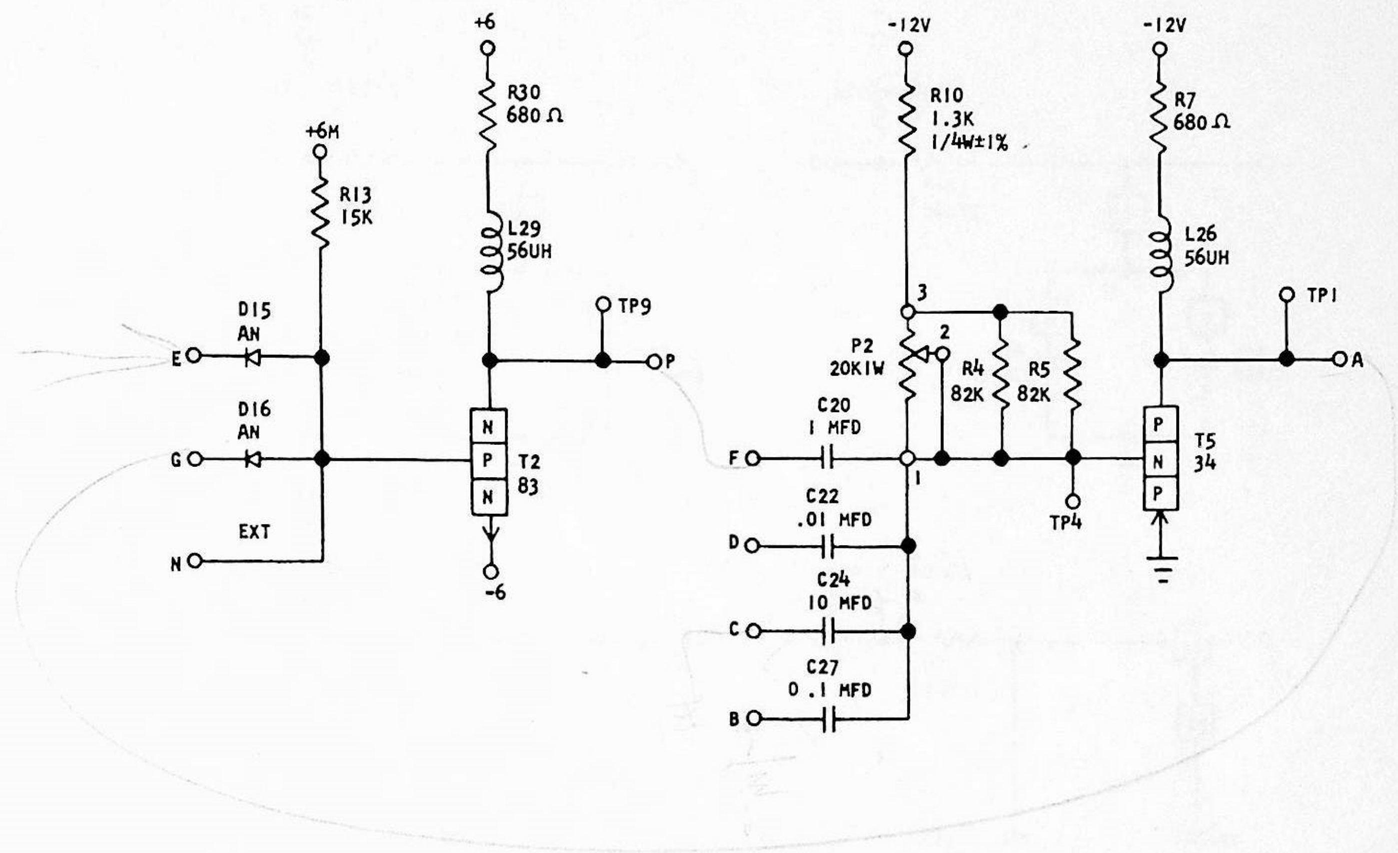
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371592

CTDL SINGLE SHOT "U" INPUT

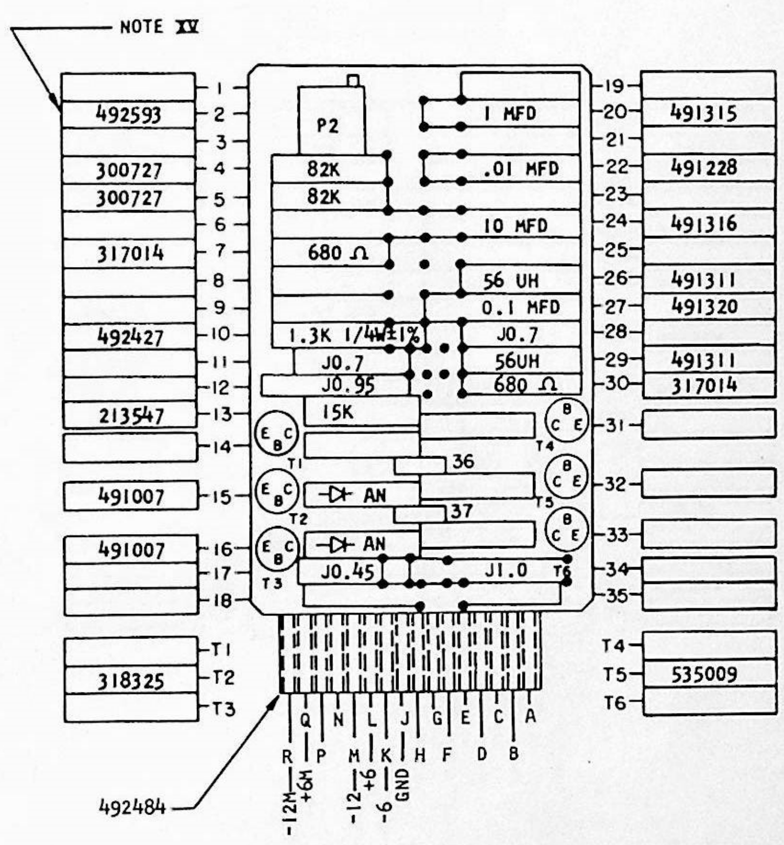




SEQUENCE OF OPERATION

1. T2, T5 ON; A TIED TO G FOR LATCH BACK AND P TO EITHER D, B, F OR C
2. MINUS GOING INPUT TO E, T2, T5 OFF
3. R.C. NETWORK DETERMINES LENGTH OF TIME T5 OFF
4. DOWN INPUT ON EXTENDER CARD WILL GIVE SAME SEQUENCE

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
E	U	INPUT		UP	-0.5	0.2
				DOWN	-7.4	-12.5
N		EXTENDER INPUT		UP	-6	
				DOWN	-12	
G	U	INPUT		UP	-0.5	0.2
				DOWN	-7.4	-12.5
A	U	OUTPUT		UP	-0.5	0.2
				DOWN	-7.44	-12.5
P	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
T5 BASE		SWITCH LEVEL →				



CONPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TSTR - CTDL					6 2? 62	115599					
	SINGLE SHOT "U" INPUT											
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

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CARD CODE	729886
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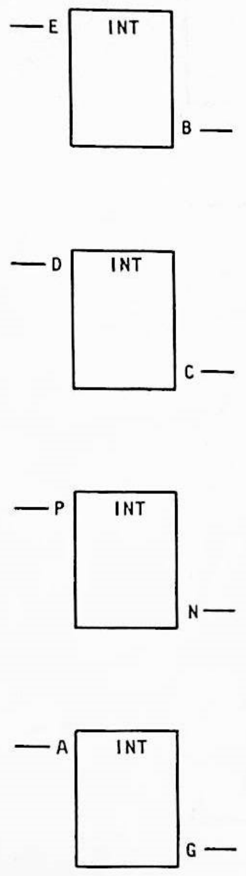
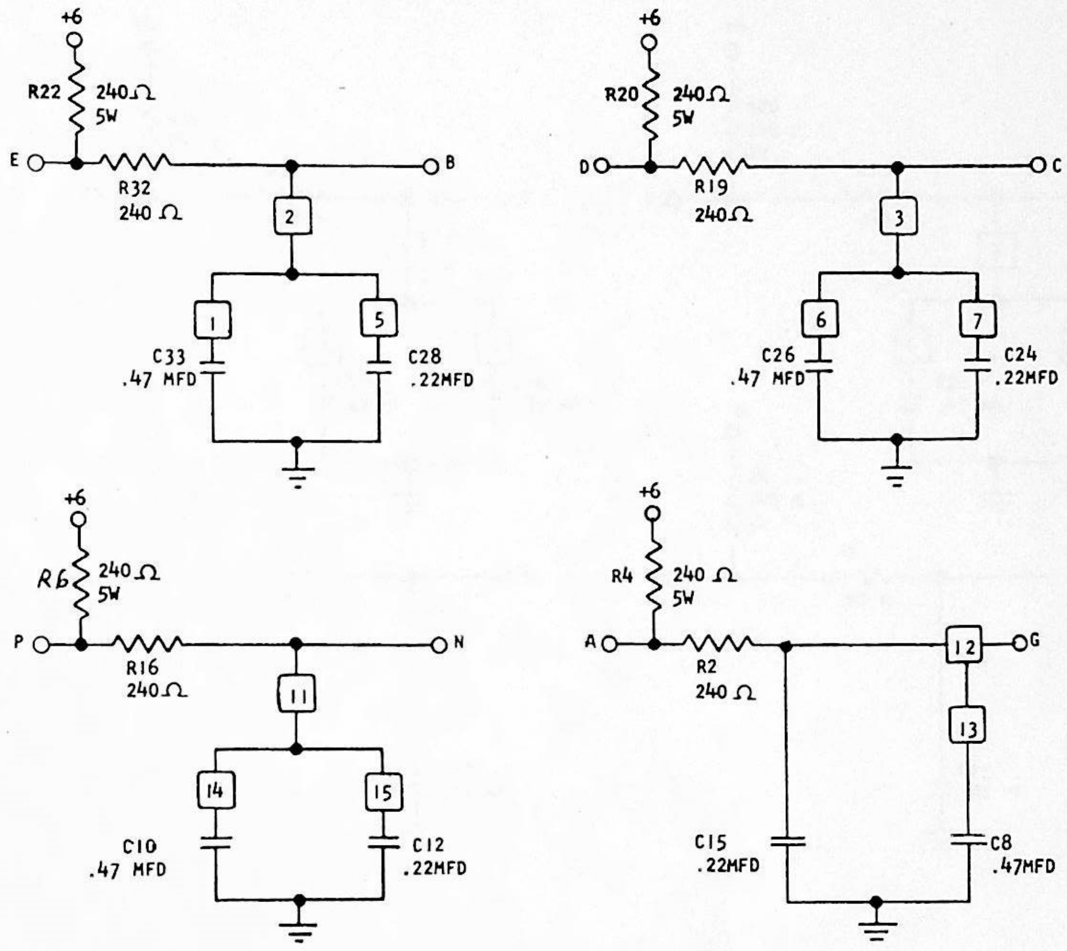
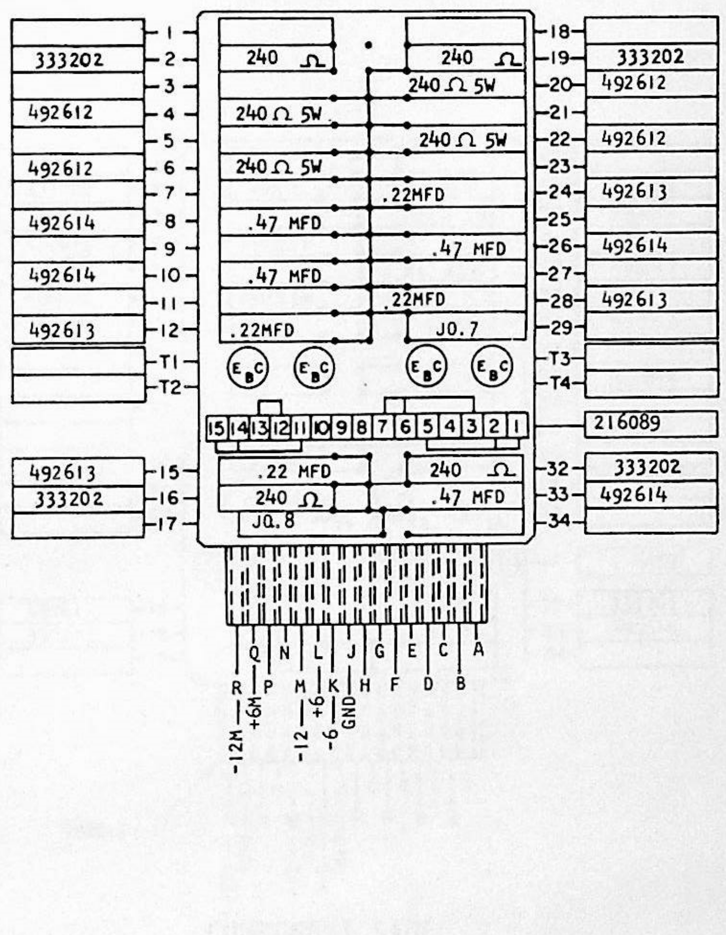
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371635

CTDL - INTEGRATOR - U AND - T







APPLICATION

1. USED TO PROVIDE AN OUTPUT THAT IS FREE OF INTERMITTENT FLUCTUATIONS RESULTING FROM BOUNCING OF MECHANICAL OPERATED CONTACTS

2. B, C, N, G ARE AT +6 LEVEL IF CONTACT IS OPEN AND -6 LEVEL IF CLOSED

3. WHEN THE INPUT IS MADE THROUGH A CAM TO 130 OHMS TIED TO -12 VOLTS, THE OUTPUT IS A-T LINE. DELAY IS AS FOLLOWS: RTH=325 OHMS. 3T=3RTH C.

	MINIMUM	MAXIMUM	CAPACITANCE
TURN ON	3T=510 USEC	3T=845 USEC	.69UF
TURN ON	348	580	.47UF
TURN ON	162	268	.22UF
RTH=480 OHMS			
TURN OFF	3T=755	1250	.69UF
TURN OFF	514	852	.47UF
TURN OFF	240	400	.22UF

4. WHEN THE INPUT IS MADE THROUGH A CAM TO -12 VOLTS, THE OUTPUT IS A-U LINE. DELAY IS AS FOLLOWS: RTH=240 OHMS

	MINIMUM	MAXIMUM	CAPACITANCE
TURN ON	3T=377 USEC	626 USEC	.69UF
TURN ON	257	426	.47UF
TURN ON	120	200	.22UF
RTH=480 OHMS			
TURN OFF	3T=754 USEC	1254 USEC	.69UF
TURN OFF	514	852	.47UF
TURN OFF	240	400	.22UF

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL- INTEGRATOR - U AND T					6 -62	115599					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

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CARD CODE	729887
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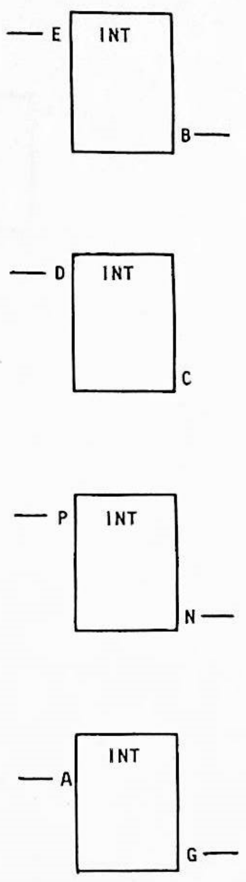
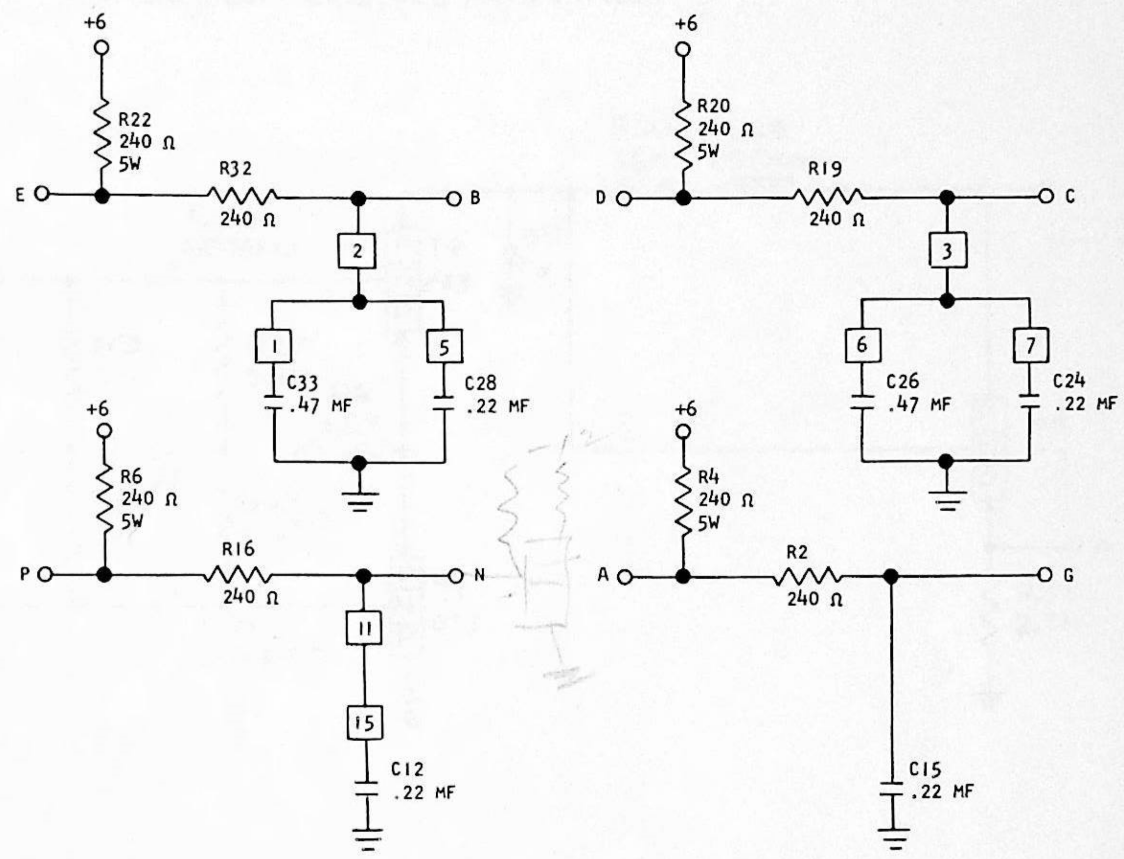
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371996

CTDL - INTEGRATOR - U AND - T





APPLICATION

1. USED TO PROVIDE AN OUTPUT THAT IS FREE OF INTERMITTENT FLUCTUATIONS RESULTING FROM BOUNCING OF MECHANICAL OPERATED CONTACTS

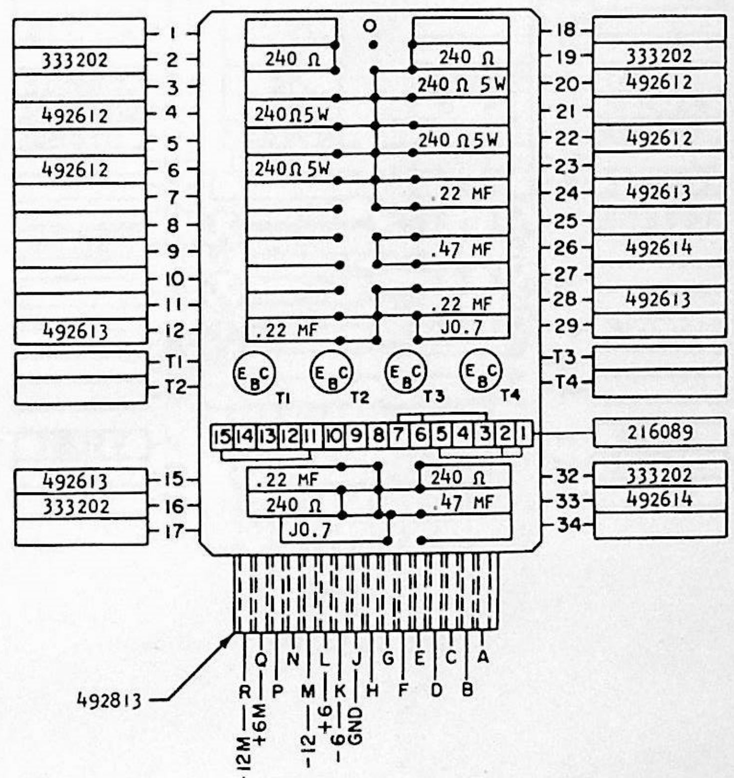
2. B, C, N, G ARE AT +6 LEVEL IF CONTACT IS OPEN AND -6 LEVEL IF CLOSED

3. WHEN THE INPUT IS MADE THROUGH A CAM TO 130 OHMS TIED TO -12 VOLTS. THE OUTPUT IS A-T LINE. DELAY IS AS FOLLOWS. RTH=325 OHMS. 3T=3RTH C.

	MINIMUM	MAXIMUM	CAPACITANCE
TURN ON	3T=510 USEC	3T=845 USEC	.69UF
TURN ON	348	580	.47UF
TURN ON	162	268	.22UF
	RTH=480 OHMS		
TURN OFF	3T=755	1250	.69UF
TURN OFF	514	852	.47UF
TURN OFF	240	400	.22UF

4. WHEN THE INPUT IS MADE THROUGH A CAM TO -12 VOLTS. THE OUTPUT IS A-U LINE. DELAY IS AS FOLLOWS: RTH=240 OHMS

	MINIMUM	MAXIMUM	CAPACITANCE
TURN ON	3T=377 USEC	626 USEC	.69UF
TURN ON	257	426	.47UF
TURN ON	120	200	.22UF
	RTH=480 OHMS		
TURN OFF	3T=754 USEC	1254 USEC	.69UF
TURN OFF	514	852	.47UF
TURN OFF	240	400	.22UF



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				
NAME	CARD ASM TSTR - CTDL- INTEGRATOR - U AND - T			
DESIGN			MODEL	SMS
DETAIL	RQ	3-1-62	SCALE	NONE
CHECK	WH	3-1-62	DRAW	LIG 3-17-62
APPRO			CHECK	

	DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
ℓ	-62	115599					

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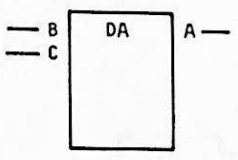
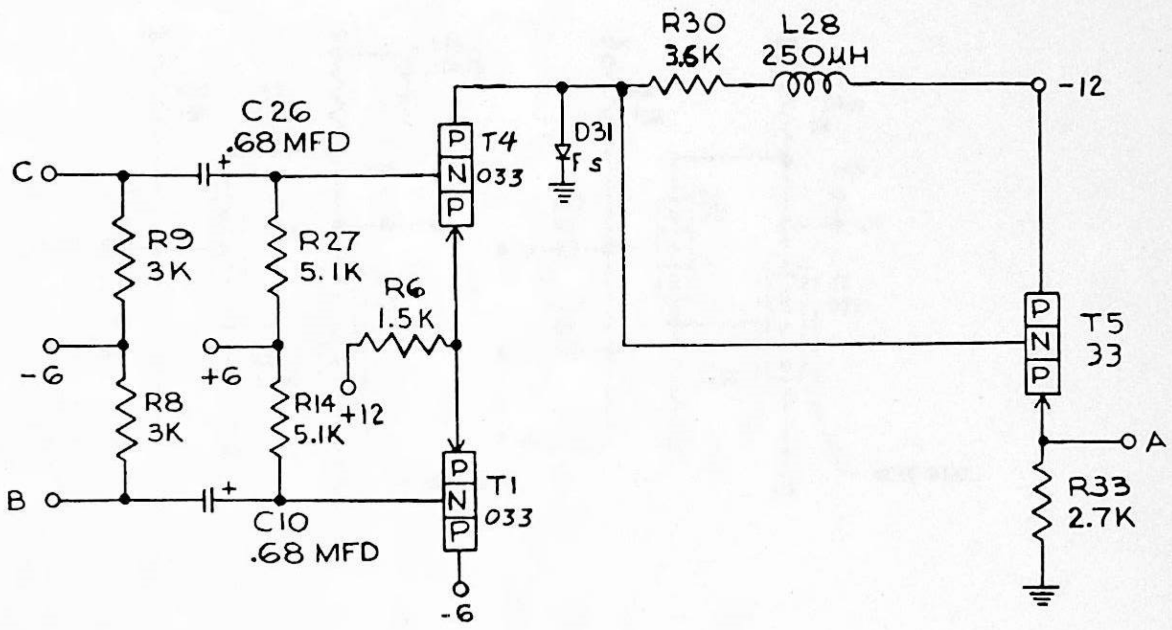
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371671

ALLOY DIFFERENCE AMPLIFIER

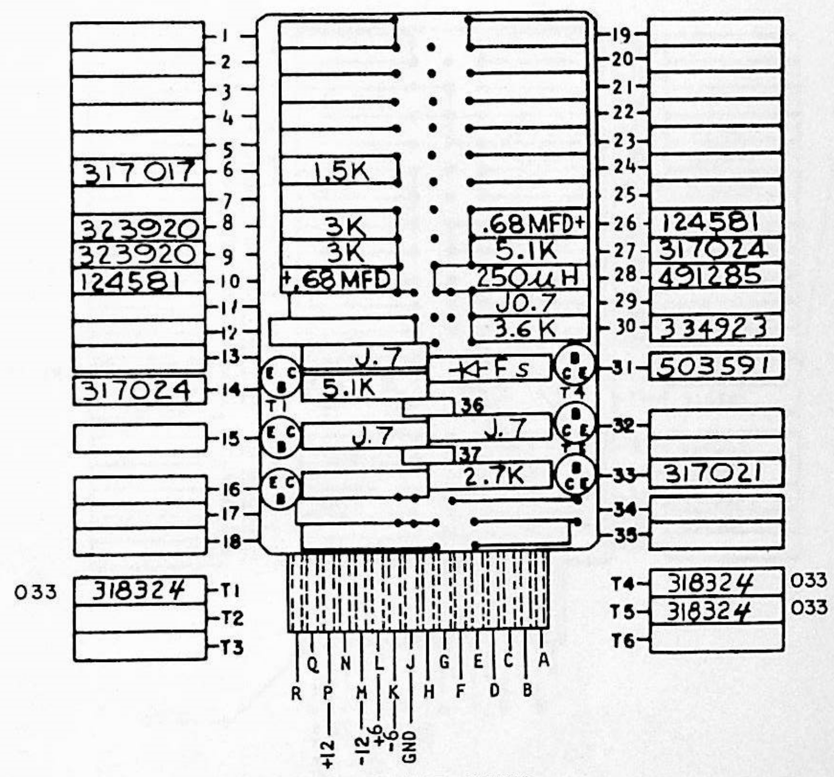




SEQUENCE OF OPERATION

1. 50 TO 100 MV P-P INPUT SIGNAL REQUIRED
2. OUTPUT WILL FOLLOW B INPUT

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
C		INPUT		UP		
				DOWN		
B		INPUT		UP		
				DOWN		
A	U	OUTPUT		UP		0.0
				DOWN		-9.0



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TSTR - ALLOY DIFFERENCE AMPLIFIER			6-26-62	115599					729888
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

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STANDARDS CODE

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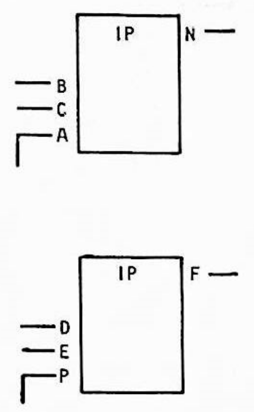
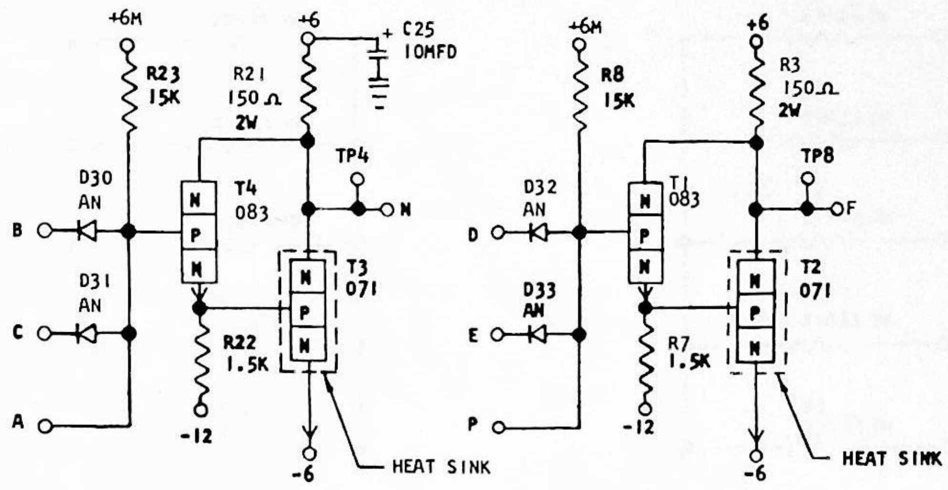
CARD CODE	729889
NU --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371676

CTDL POWER INVERTER "P" TYPE

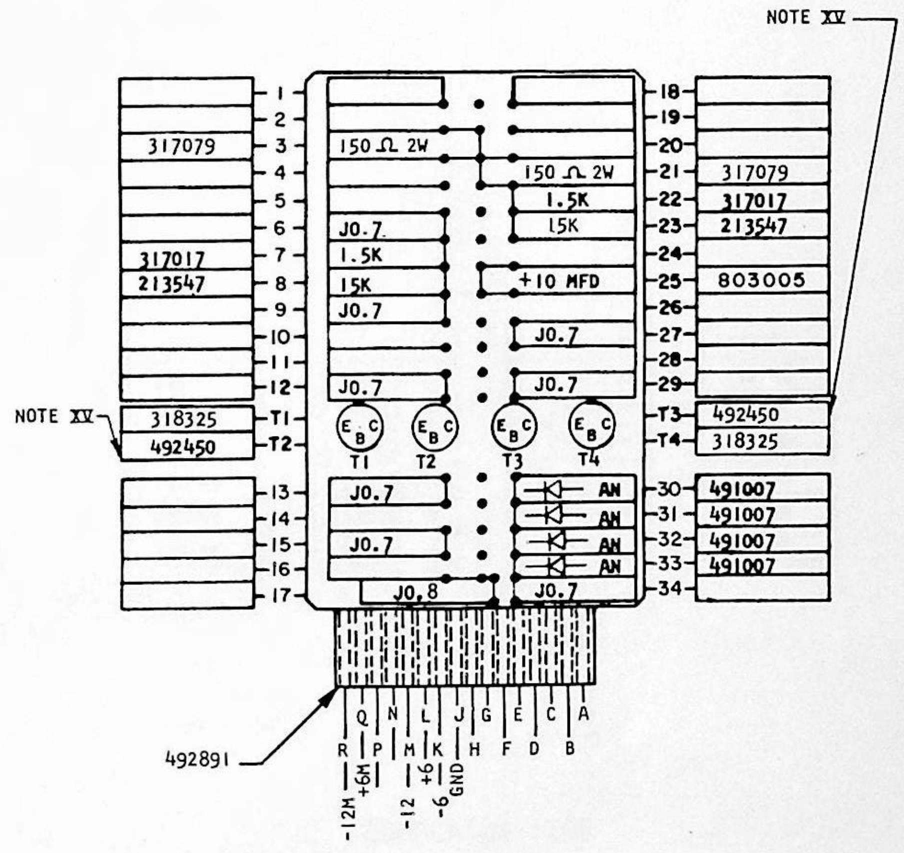




SEQUENCE OF OPERATION

1. ALL INPUTS UP TRANSISTORS ON OUTPUT DOWN.
2. ANY INPUT DOWN TRANSISTORS OFF OUTPUT UP.
3. INPUTS TO EXTENDER CARD MUST BE UP IN COINCIDENCE WITH INPUTS TO CARD FOR DOWN OUTPUT.
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

NOTE XV



COMPONENT SIDE

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
B,O	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
C,E	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
A,P		EXTENDER INPUT		UP	-6	
				DOWN	-12	
N,F	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.40
TURN OFF	0.10	0.15

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.

NAME	CARD ASSEMBLY TSTR-CTDL				
	POWER INVERTER P TYPE				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
[illegible]-62	115599					

729889

C

STANDARDS CODE

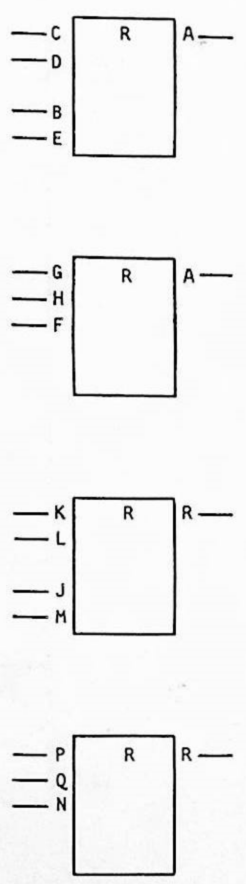
729890

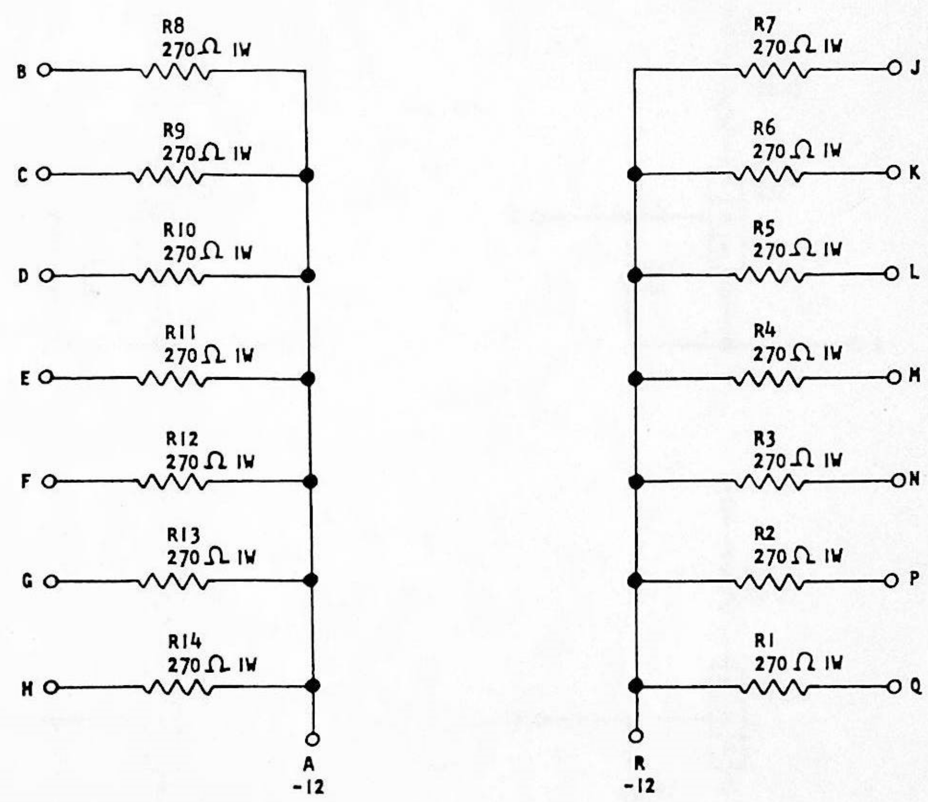
CARD CODE	729890
NW --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371598

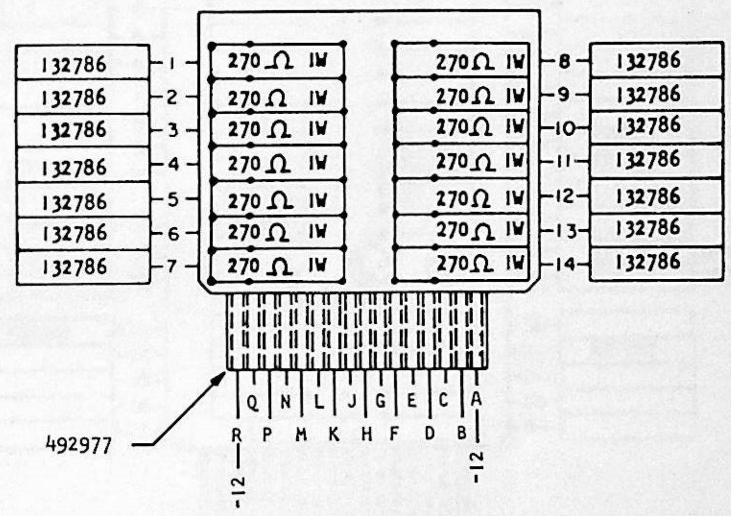
270Ω RESISTOR CARD





APPLICATION

1. ALLOWS MECHANICAL SWITCH INPUT TO CTDL BLOCK
2. SWITCH OPEN OUTPUT -12V, SWITCH CLOSED OUTPUT GROUND LEVEL
3. EACH RESISTOR IS USED INDIVIDUALLY



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM RESISTOR -270Ω				1 -62	115599					729890
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

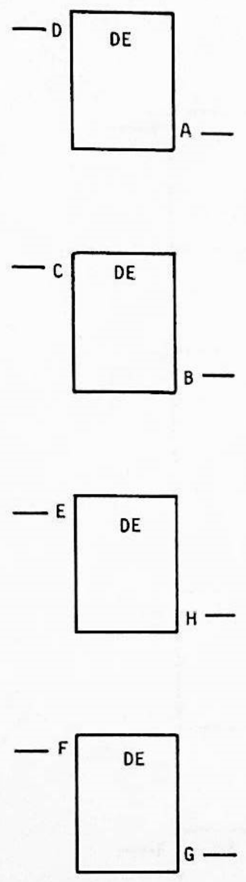
STANDARDS CODE
729891

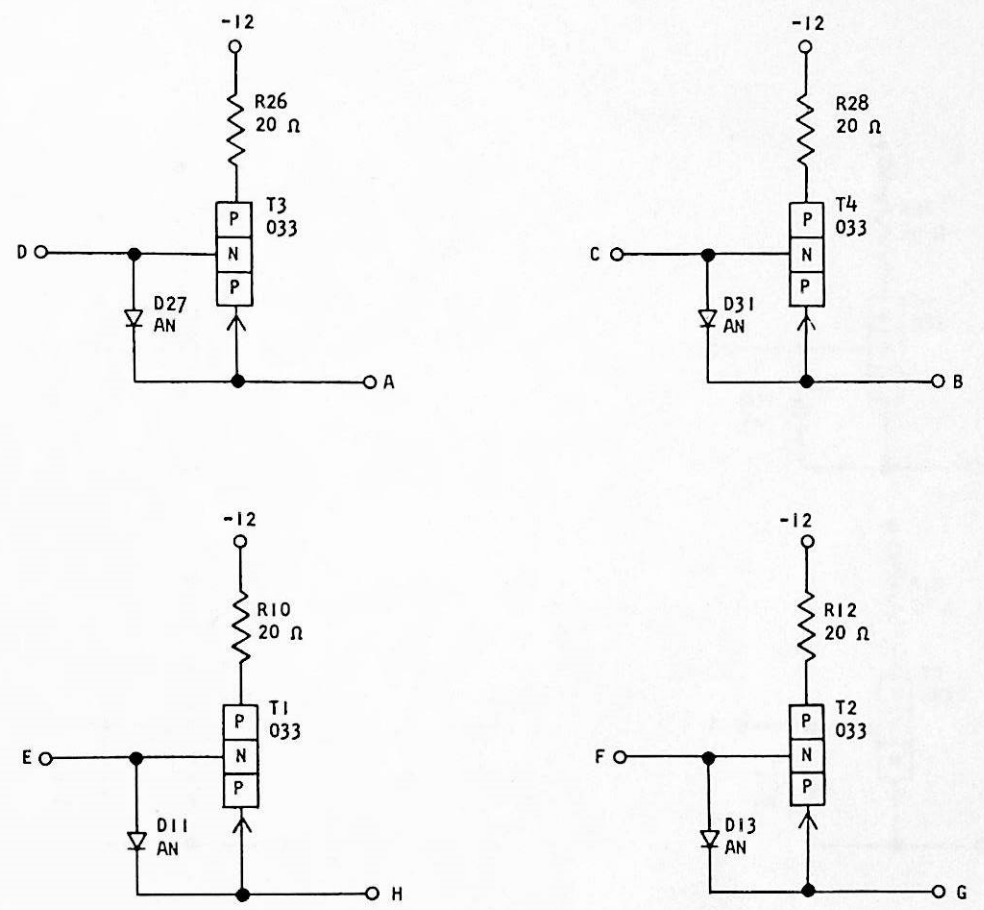
CARD CODE	729891
PP --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371365

CTDL EMITTER FOLLOWER - PNP





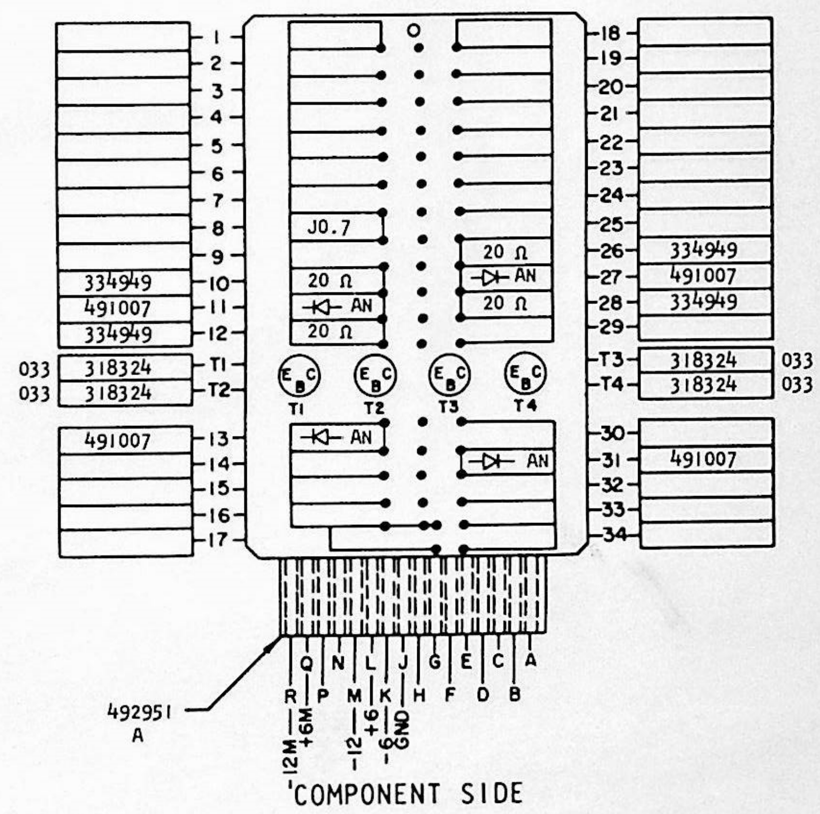
SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT DOWN
2. INPUT UP TRANSISTOR OFF OUTPUT UP
3. CIRCUIT MAY DRIVE UP TO 40 1-WAY LOGIC BLOCKS.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
D,E, C,F	U	INPUT		UP	-0.54	0.24
				DOWN	-9.66	-12.5
A,H, B,G	U	OUTPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

NO APPRECIABLE DELAY BETWEEN THE INPUT AND OUTPUT OF THE HIGH DRIVE EF.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- CTDL EMITTER FOLLOWER-PNP			-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729891

C

STANDARDS CODE

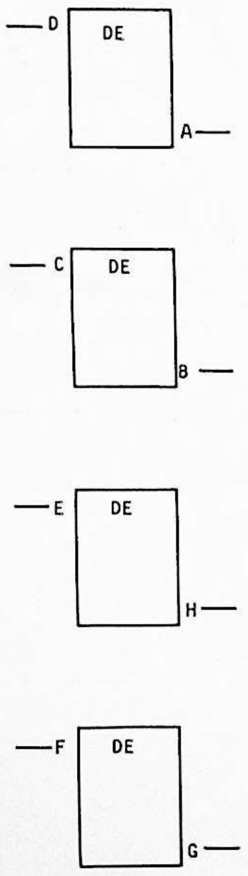
729892

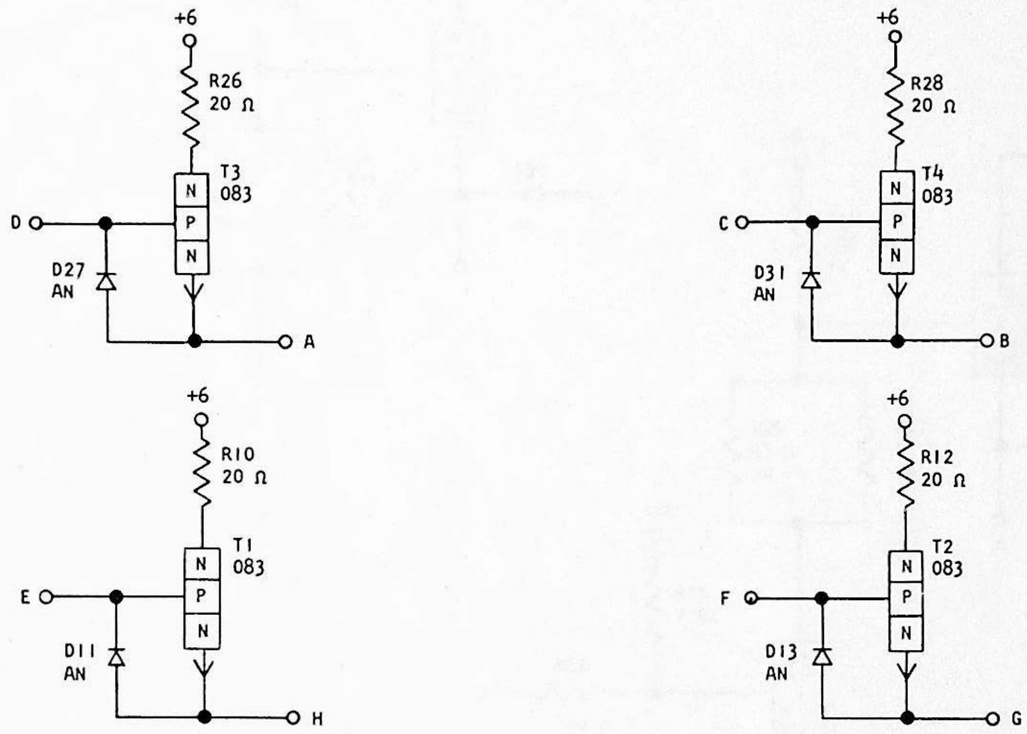
CARD CODE	729892
PQ --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371370

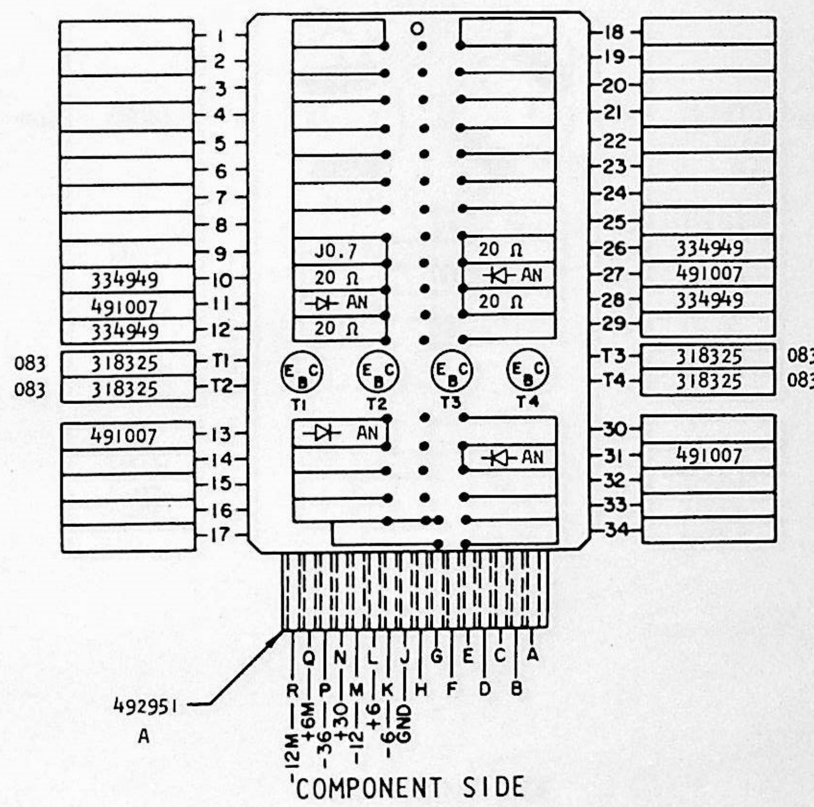
CTDL EMITTER FOLLOWER - NPN





SEQUENCE OF OPERATION

1. OUTPUT WILL FOLLOW INPUT
2. CIRCUIT MAY DRIVE UP TO 40 1-WAY LOGIC BLOCKS.



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D,C, E,F	T	INPUT		UP	4.26	6.24
				DOWN	-5.46	-6.24
A,B, H,G	T	OUTPUT		UP	3.89	6.24
				DOWN	-4.46	-6.24

DELAY - USEC

NO APPRECIABLE DELAY BETWEEN THE INPUT AND OUTPUT OF THE HIGH DRIVE EF.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL EMITTER FOLLOWER-NPN				6-26-62	115599					729892
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

STANDARDS CODE

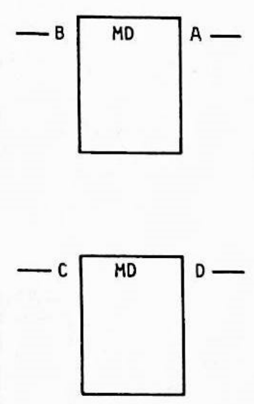
729893

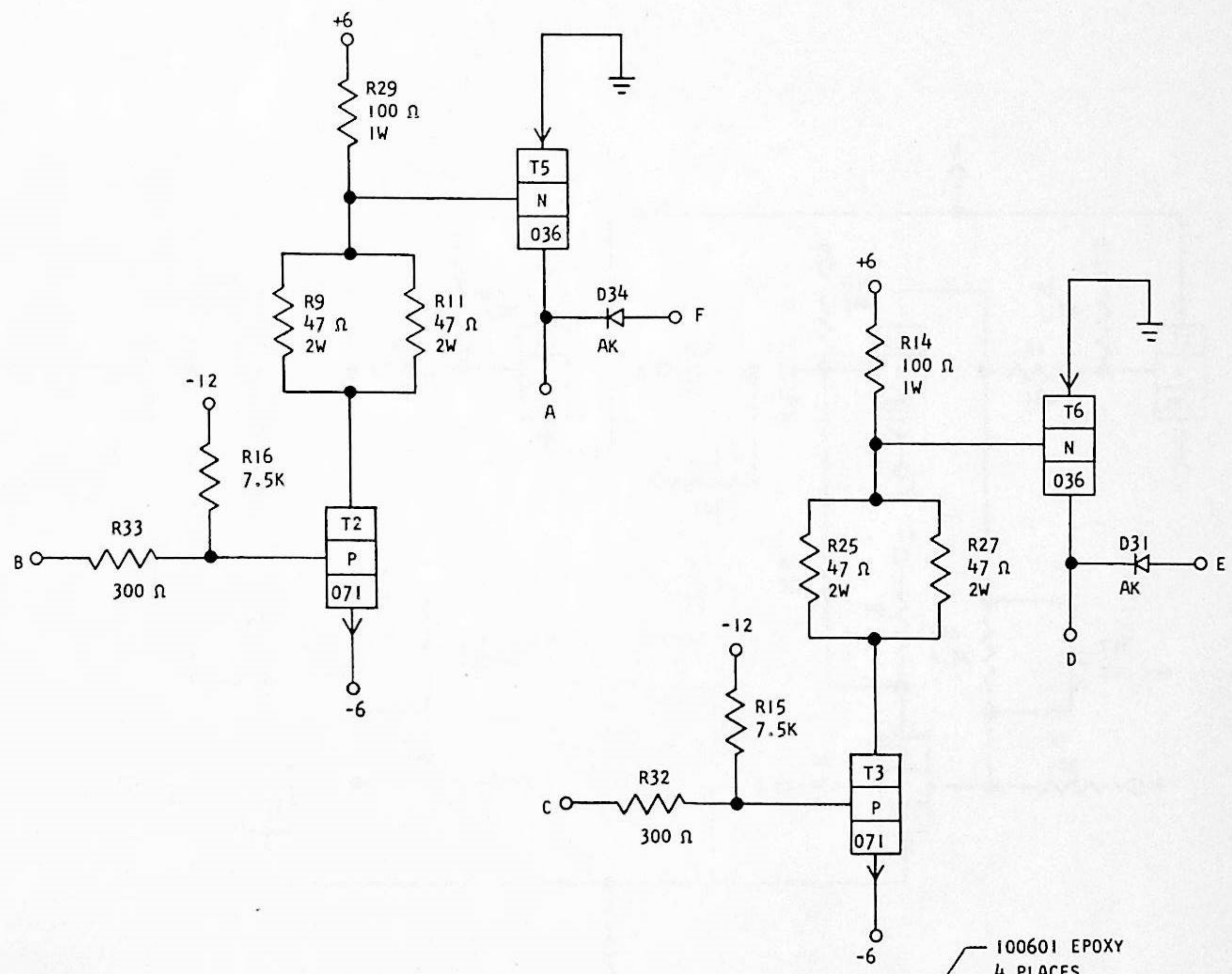
CARD CODE	729893
QC --	

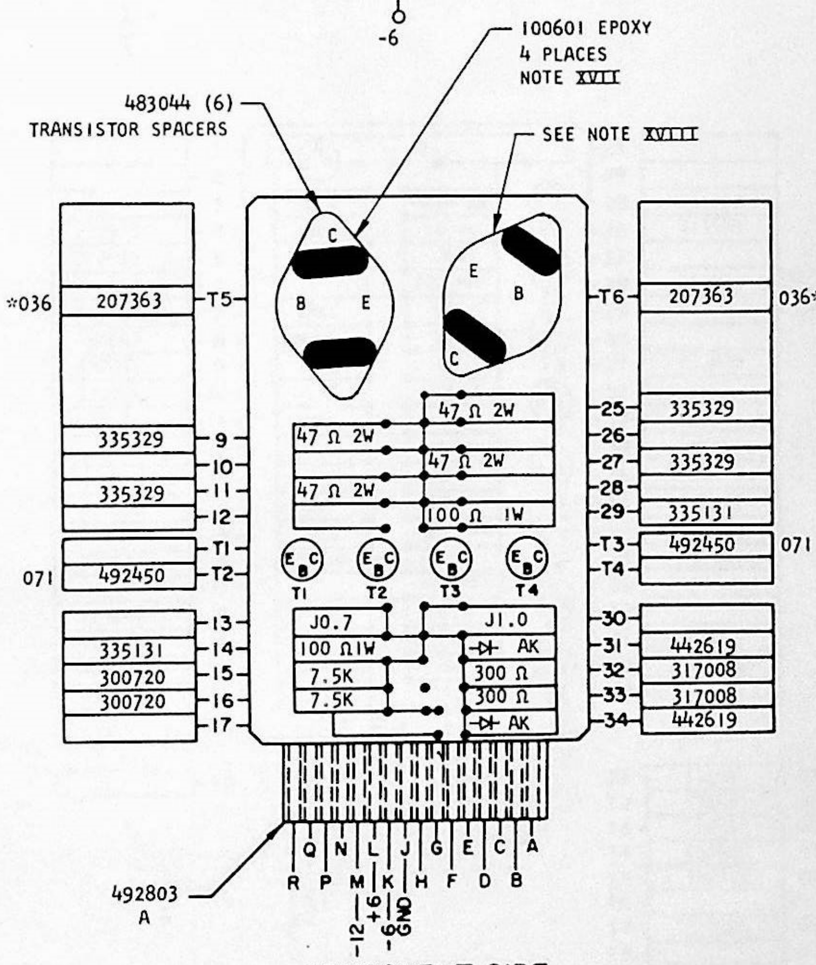
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371633

ALLOY-CLUTCH MAGNETIC DRIVER







COMPONENT SIDE

SEQUENCE OF OPERATION

INPUT UP TRANSISTORS ON OUTPUT UP

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
B,C	U	INPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
A,D		OUTPUT		UP	-1.24	+.24
				DOWN	-20	-20
F,E		CLAMP		UP	-20	-20
				DOWN	-20	-20

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.			
NAME	CARD ASM TSTR-ALLOY CLUTCH MAGNETIC DRIVER		
DESIGN		MODEL	SMS
DETAIL	RQ 3-1-62	SCALE	NONE
CHECK	WH 3-1-62	DRAW	LIG 3-17-62
APPRO		CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-?-62	115599					729893

C

STANDARDS CODE

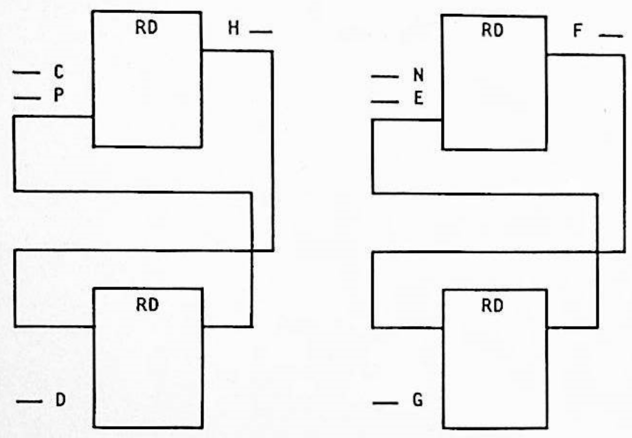
729894

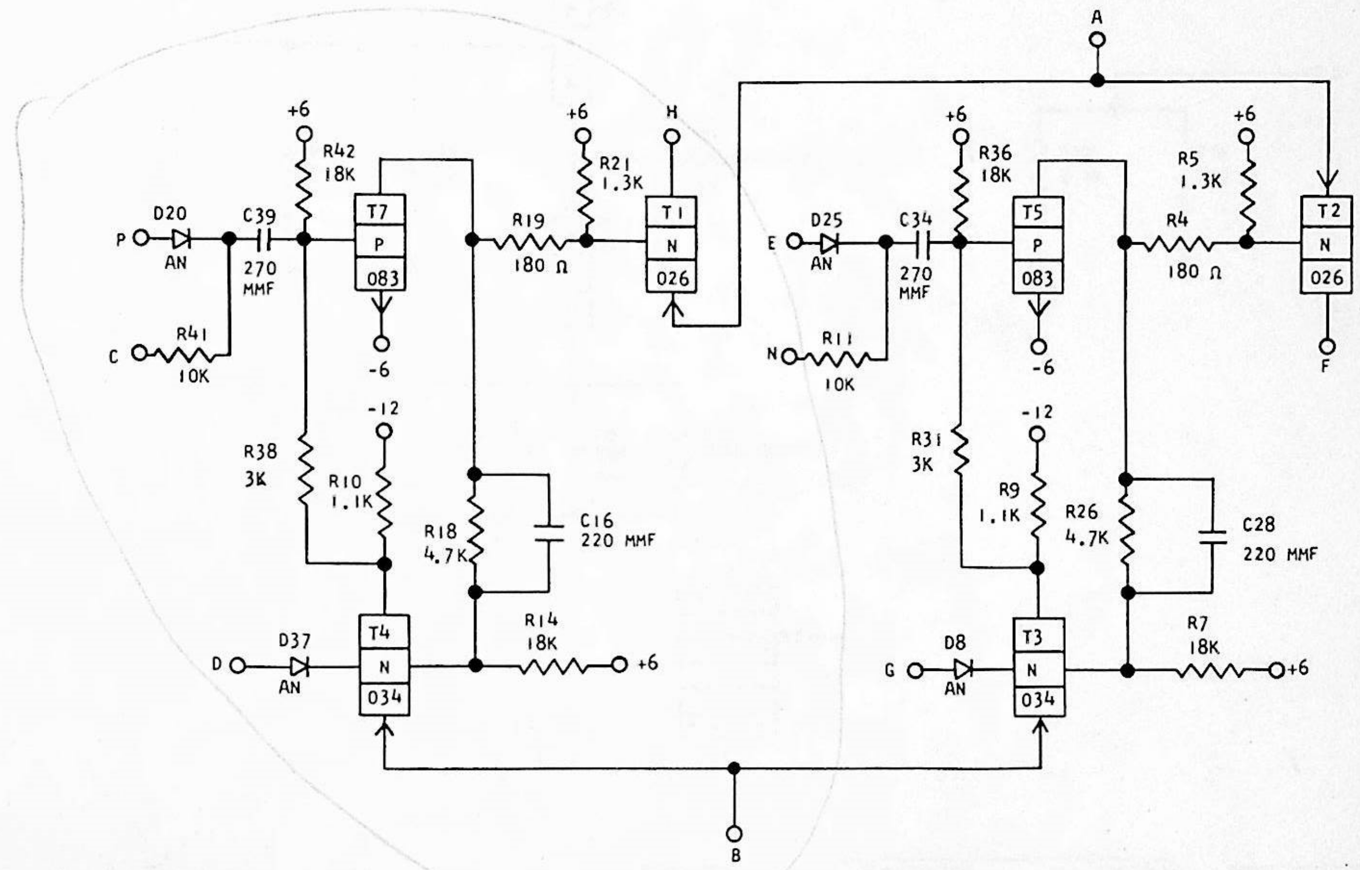
CARD CODE	729894
QD --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371078

ALLOY-RELAY DRIVER



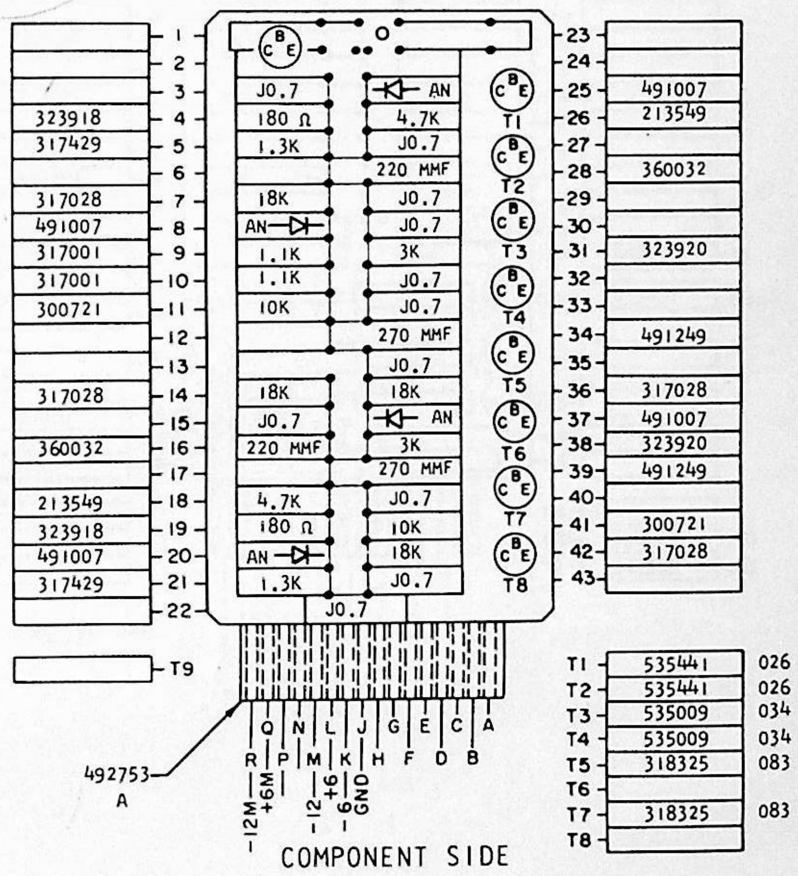


SEQUENCE OF OPERATION

1. PIN C MUST BE DOWN 7.5 U SEC BEFORE P GOES TO UP LEVEL, TURNING T7 ON. T7 ON TURNS T1 & T4 ON. T4 PROVIDES LATCH BACK TO HOLD T7 ON.

2. UP LEVEL AT D OR MECHANICAL RESET AT B WILL TURN T4 OFF AND OPEN LATCH BACK TO T7.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
C, N	U	INPUT		UP	-3.0	0.2
				DOWN	-10.0	-12.5
P, E	U	INPUT		UP	-0.5	0.2
				DOWN	-8.5	-12.5
D, G	T	RESET		UP	1.4	6.2
				DOWN	-0.7	-6.2
H, F	W	OUTPUT		UP	0.2	
				DOWN		-45



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR DRIVER			6 . . 62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729894

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STANDARDS CODE

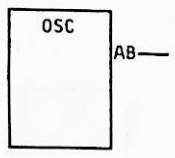
729895

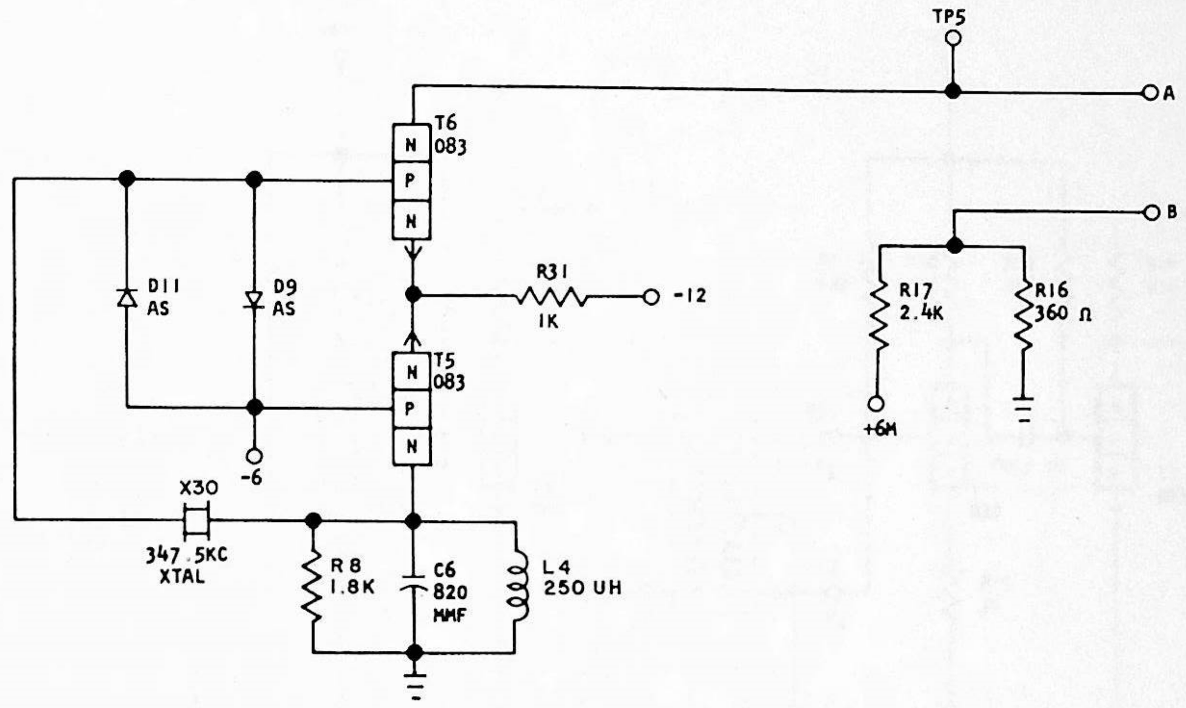
CARD CODE	729895
RK --	

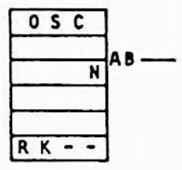
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371788

ALLOY - OSCILLATOR 347.5KC FREE RUNNING (CRYSTAL)

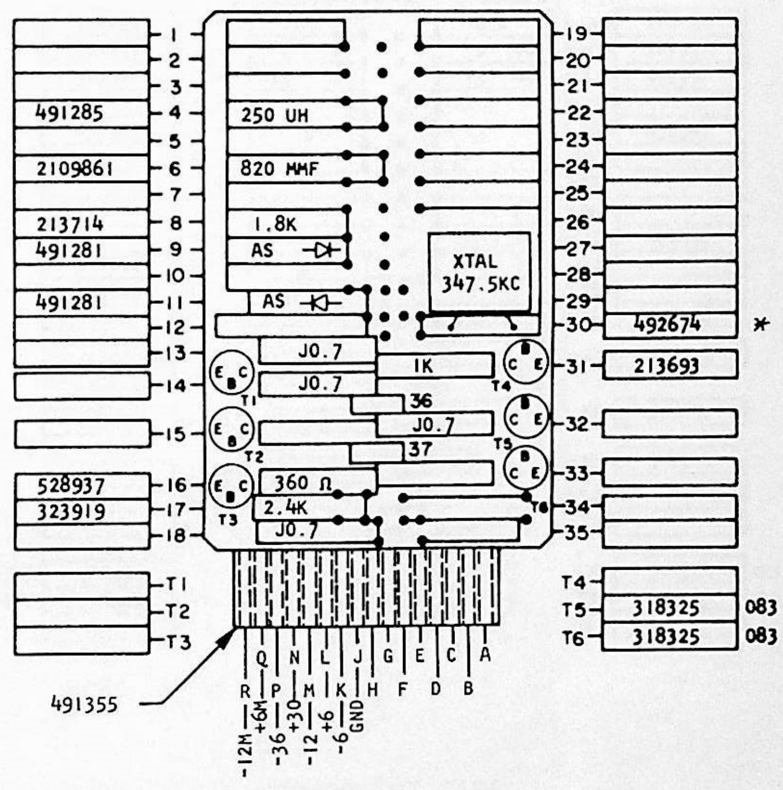






SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR IS TURNED ON
2. PIN A MUST BE TIED TO PIN B FOR LOAD



PINS	SIGNAL NAME	WAVE SHAPE	LEVEL	MIN	MAX
A	OUTPUT		UP	.69	.86
			DOWN	-.9	-2.04

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-ALLOY-OSC 347.5KC FREE RUNNING (CRYSTAL)				-62	115599					
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW LIG	3-17-62							
APPRO		CHECK								

729895

C

STANDARDS CODE

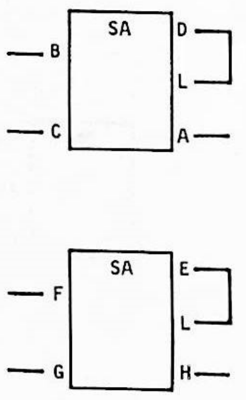
729896

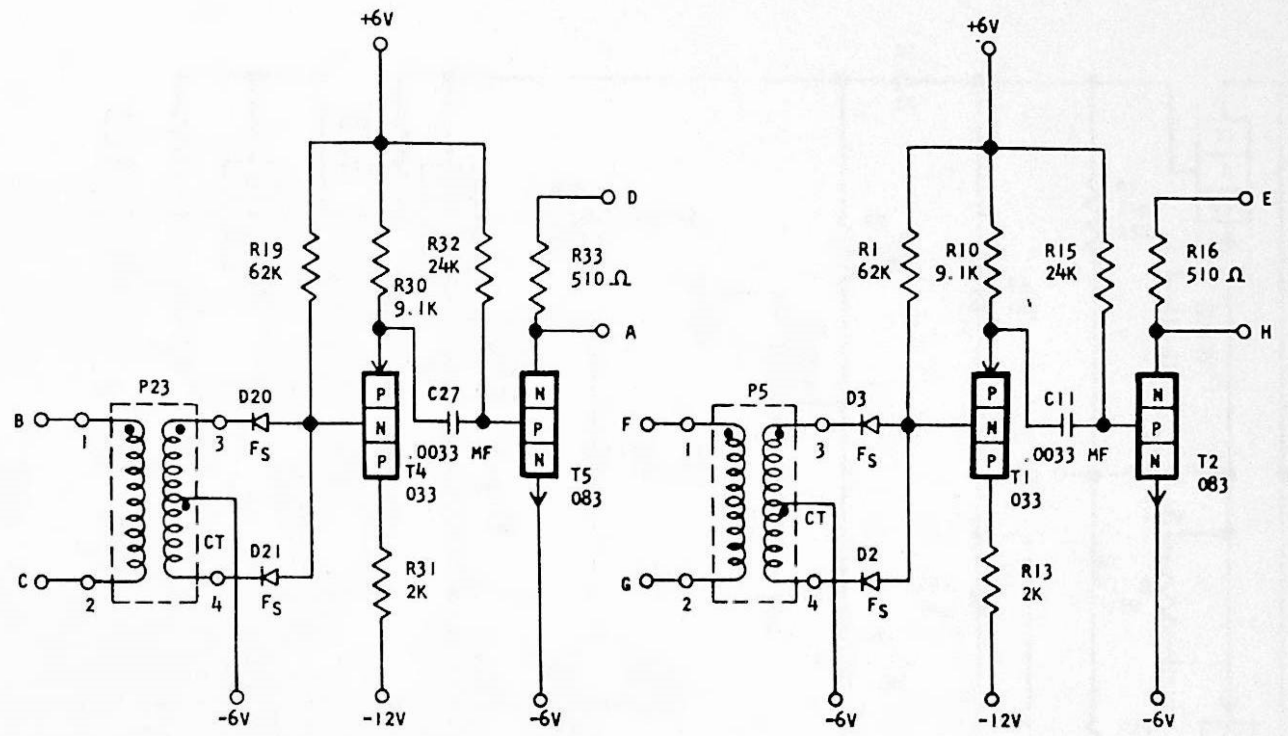
CARD CODE	729896
WL --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371898

ALLOY-SENSE AMPLIFIER NO. 2
MOUNT CARD ON ONE INCH CENTERS





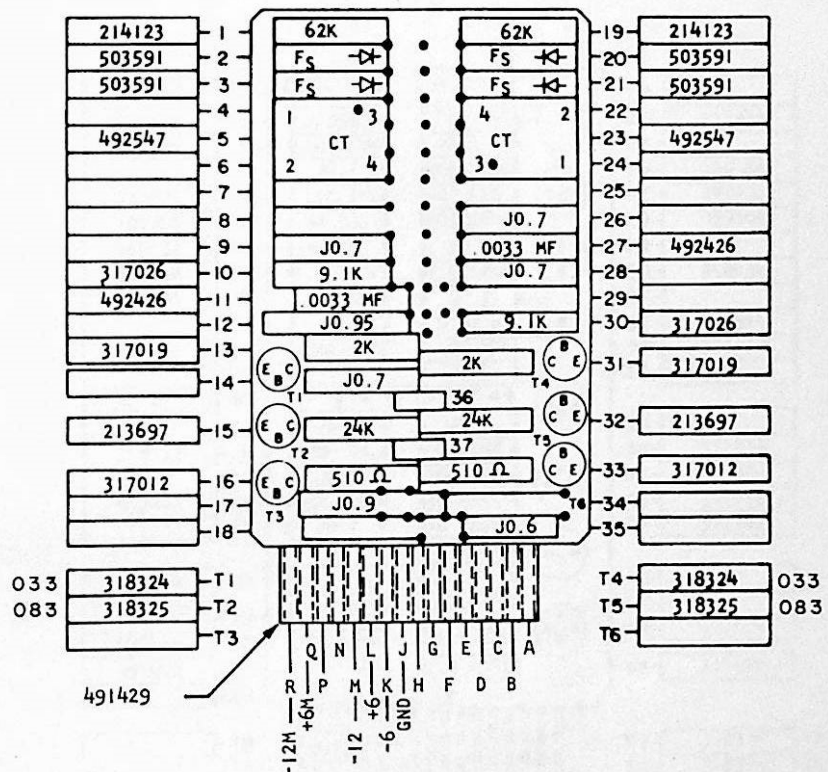
SEQUENCE OF OPERATION

1. WITH NO INPUT ALL TRANSISTORS ARE IN CONDUCTION; OUTPUT IS DOWN. E AND D ARE TIED TO +6V.

2. 50 MV MIN. P-P ACROSS B AND C IS STEPPED UP AND RECTIFIED APPEARING AS NEGATIVE SHIFT ON BASE OF T4. A NEGATIVE IV SHIFT FROM T4 EMITTER THEN TURNS T5 OFF AND THE OUTPUT IS UP.

3. AMPLIFIER OUTPUT DELAY IS 1.0 USEC MAXIMUM. AMPLIFIER DELAY SHALL BE DEFINED AS THE TIME TAKEN FROM THE 50% POINT ON THE RISE OF THE "ONE" SIGNAL TO THE 10% POINT OF THE LEADING EDGE VOLTAGE TRANSITION AT THE OUTPUT.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS	
					MIN	MAX
A,H	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY SENSE AMPLIFIER NO. 2				4 62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729896

C

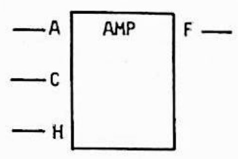
STANDARDS CODE

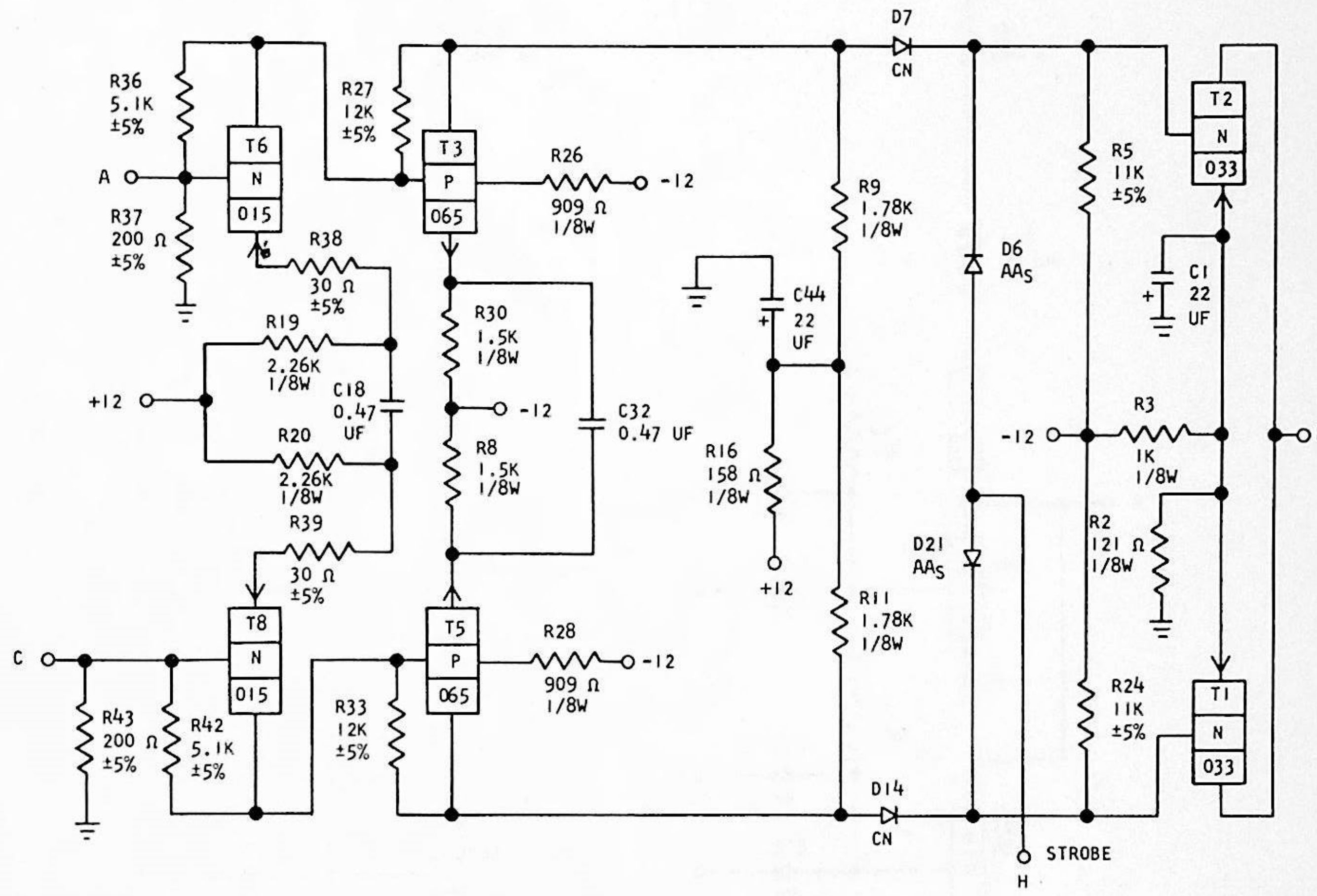
CARD CODE	729897
WX --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371899

ALLOY-AMPLIFIER, PRE SENSE NUMBER I



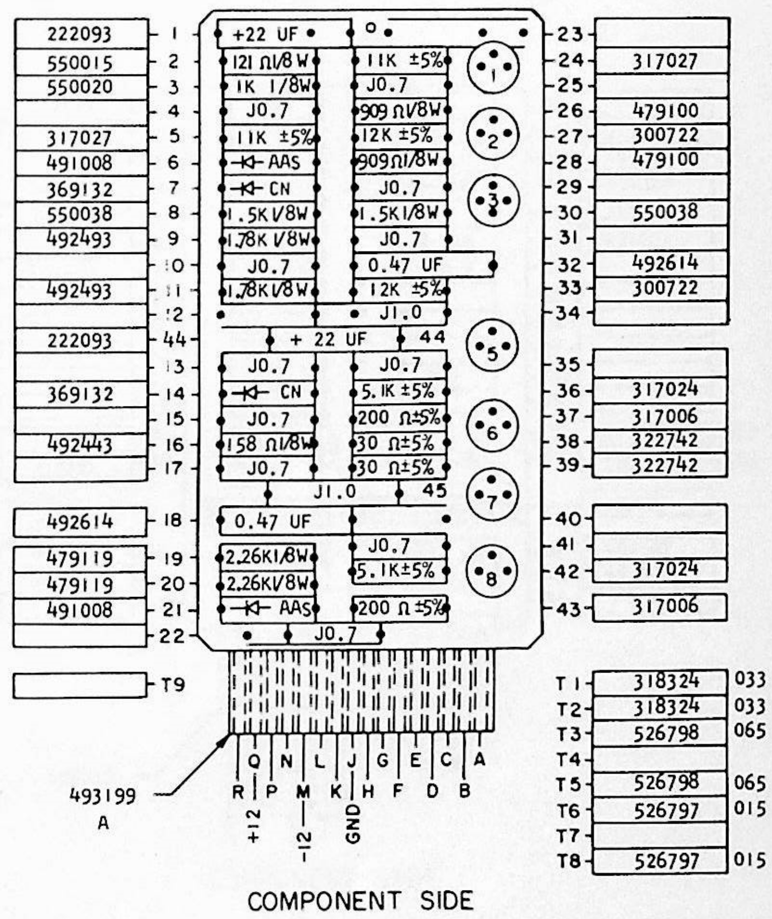


SEQUENCE OF OPERATION

1. THE T-LINE STROBE PLUSE GATES THE CORE PULSE FROM THE DIFFERENTIAL AMPLIFIER INTO EITHER 033, WHICH THEN GOES INTO THE FINAL SENSE AMPLIFIER (370836)

2. AMPLIFIER OUTPUT DELAY IS <0.4 USEC.
AMPLIFIER OUTPUT DELAY SHALL BE DEFINED AS THE TIME TAKEN FROM 10% POINT ON THE RISE OF THE INPUT SIGNAL TO THE 10% POINT OF THE LEADING EDGE VOLTAGE TRANSITION AT THE OUTPUT.

PINS	SIGNAL NAME	WAVE SHAPE		LEVELS MIN	MAX
A,C	INPUT		UP	40 M VOLTS	
			DOWN	0	
F	OUTPUT		UP	-5.2	+.24
			DOWN	-11.52	-12.48
H	STROBE		UP	+1.44	+6.24
			DOWN	-.74	-6.24



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR - ALLOY AMPLIFIER PRE SENSE NUMBER I				[illegible]-62	115599					
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729897

C

STANDARDS CODE

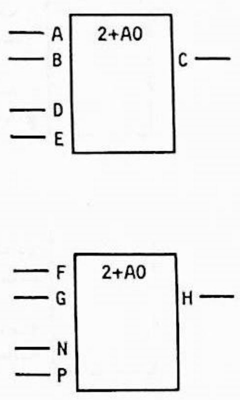
729898

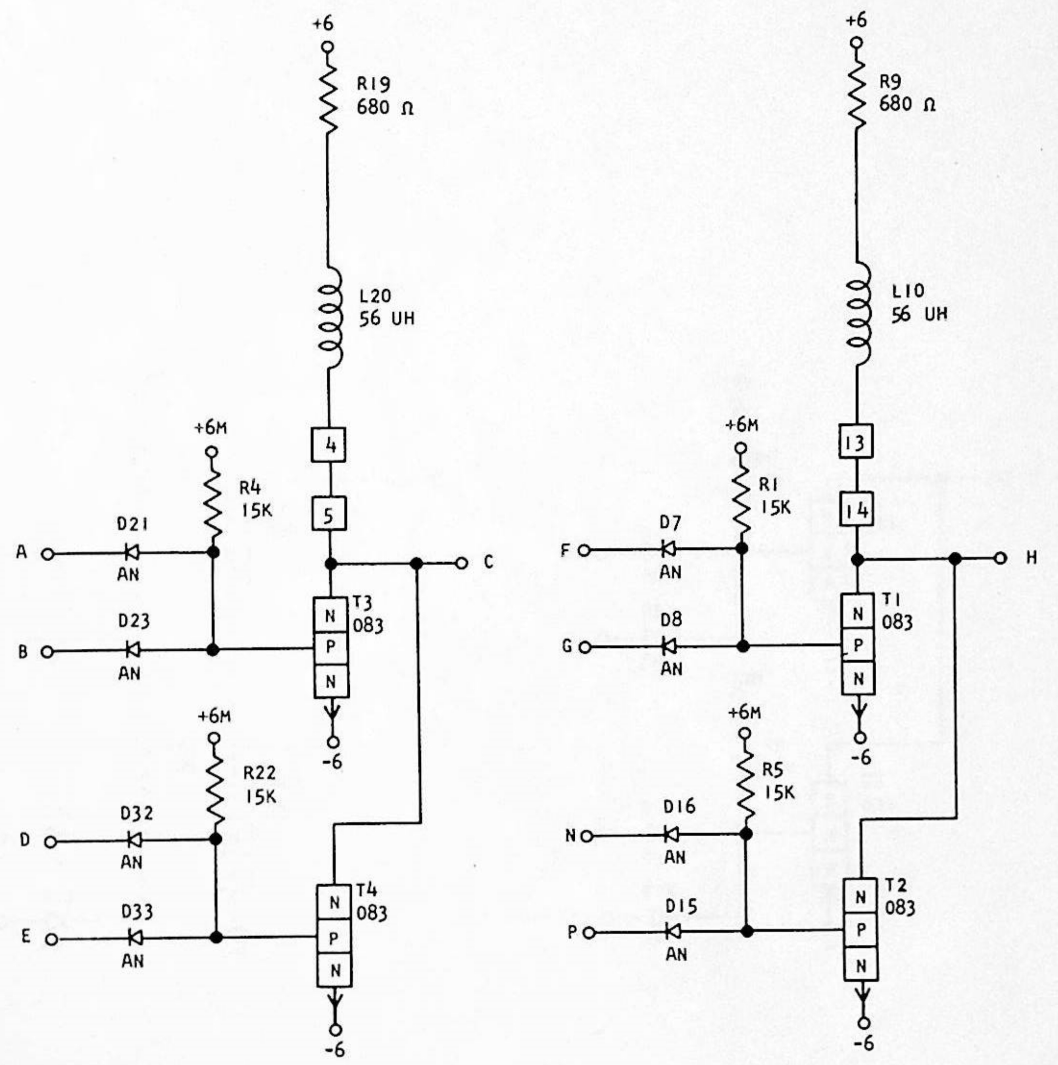
CARD CODE	729898
2J MX	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370144

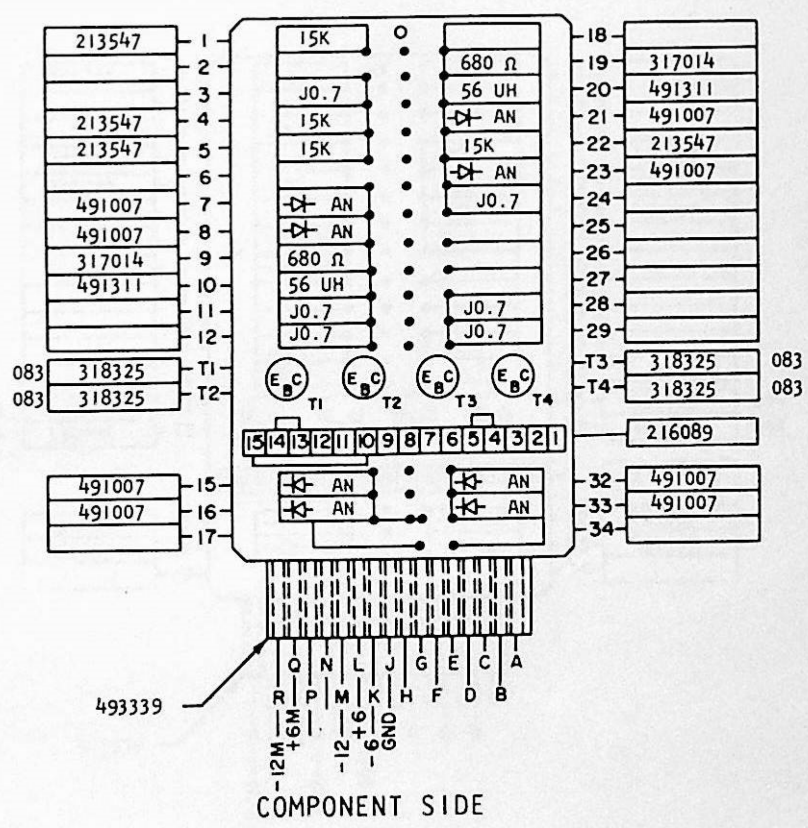
CTDL NPN TWO WAY GATE W/ COLLECTOR LOAD





SEQUENCE OF OPERATION

1. BOTH INPUTS TO A TRANSISTOR UP, TRANSISTOR ON OUTPUT DOWN
2. FOR UP OUTPUT, EITHER INPUT TO BOTH TRANSISTORS MUST BE DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
A,D, F,N	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
B,G, E,P	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
C,H	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.70
TURN OFF	0.05	1.50*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-CTDL NPN TWO WAY GATE W/ COLLECTOR LOAD				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
· · -62	115599					

729898

C

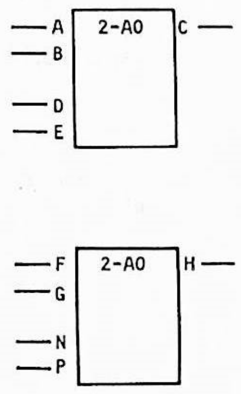
STANDARDS CODE

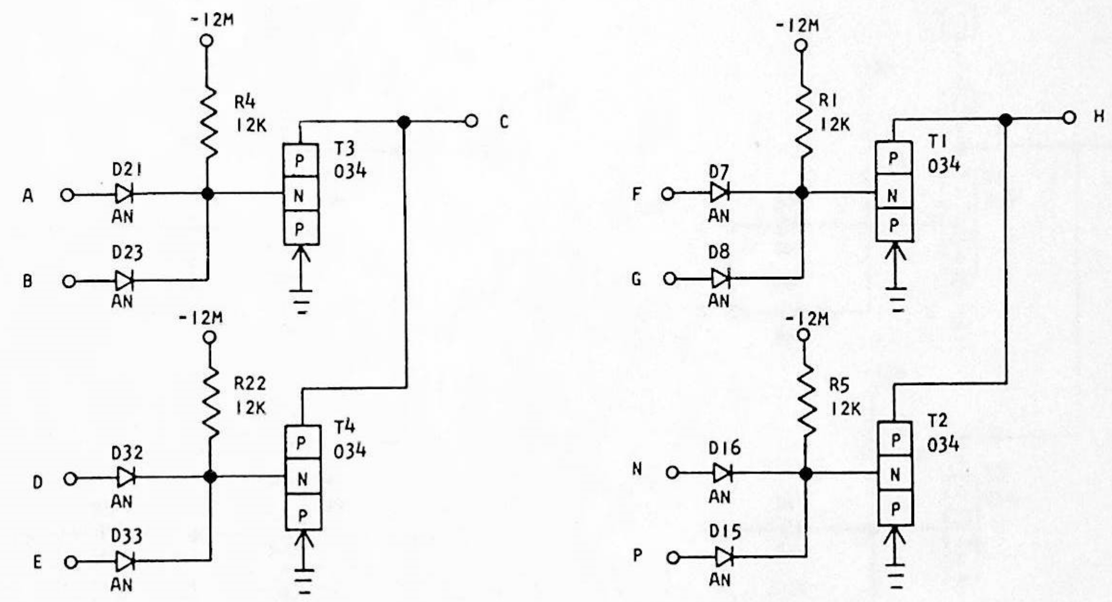
729899

CARD CODE	729899
3J MX	

REFERENCE DRAWING
SEE PRODUCTION DRAWING 370141

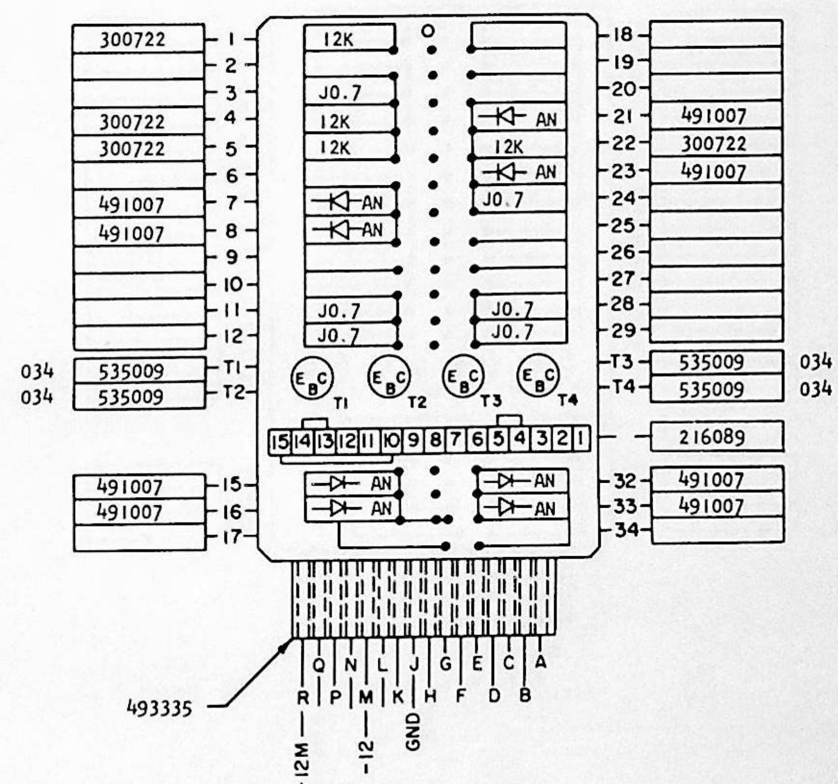
CTDL PNP TWO WAY GATE WITHOUT COLLECTOR LOAD





SEQUENCE OF OPERATION

1. BOTH INPUTS TO A TRANSISTOR DOWN, TRANSISTOR ON OUTPUT UP
2. FOR DOWN OUTPUT, EITHER INPUT TO BOTH TRANSISTORS MUST BE UP
3. EXTERNAL LOADING OF COLLECTORS REQUIRED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,D, F,N	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
B,G, E,P	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C,H	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL PNP TWO				[illegible] 62	115599					
WAY GATE WITHOUT COLLECTOR LOAD											
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729899

C

STANDARDS CODE

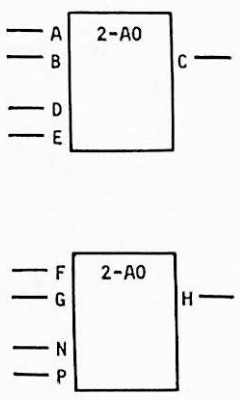
729900

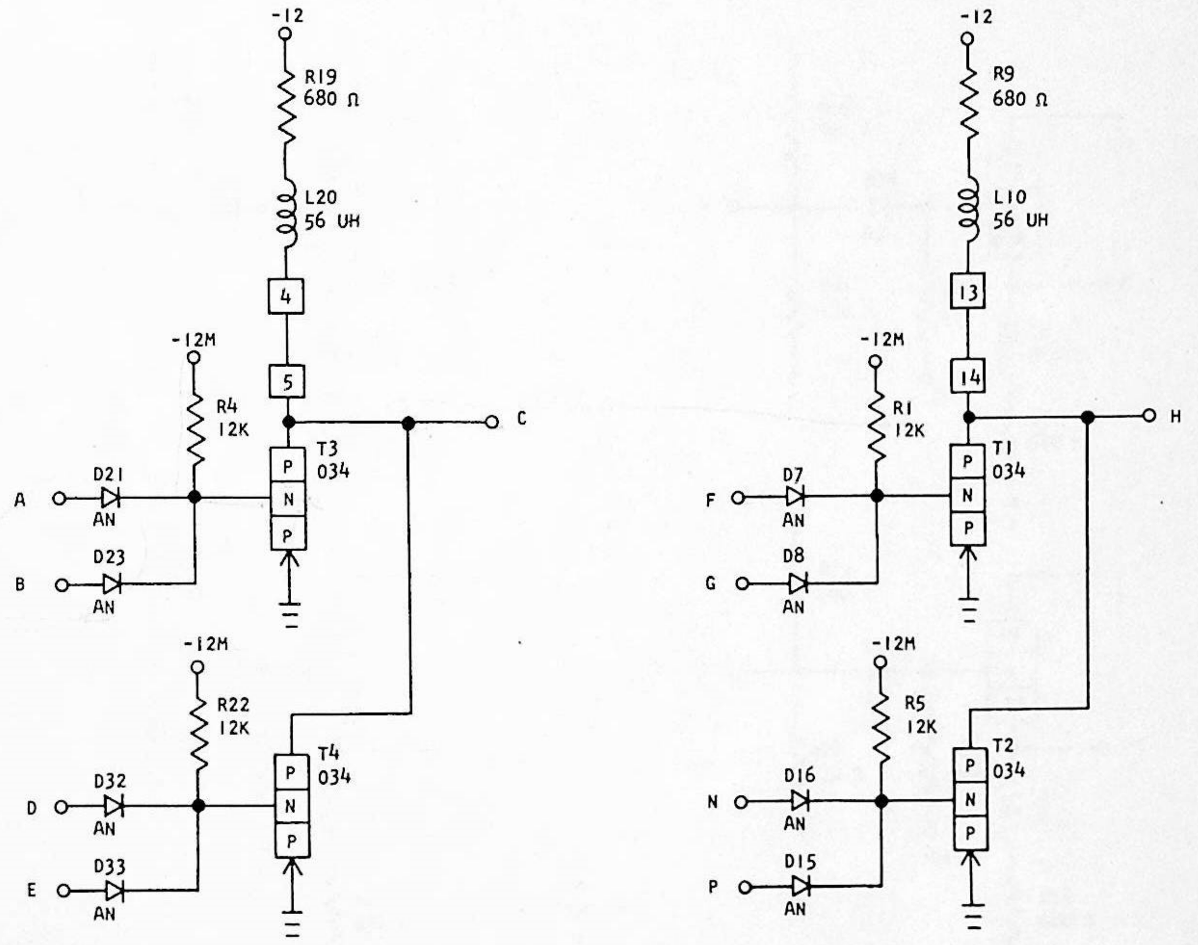
CARD CODE	729900
4J MX	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370142

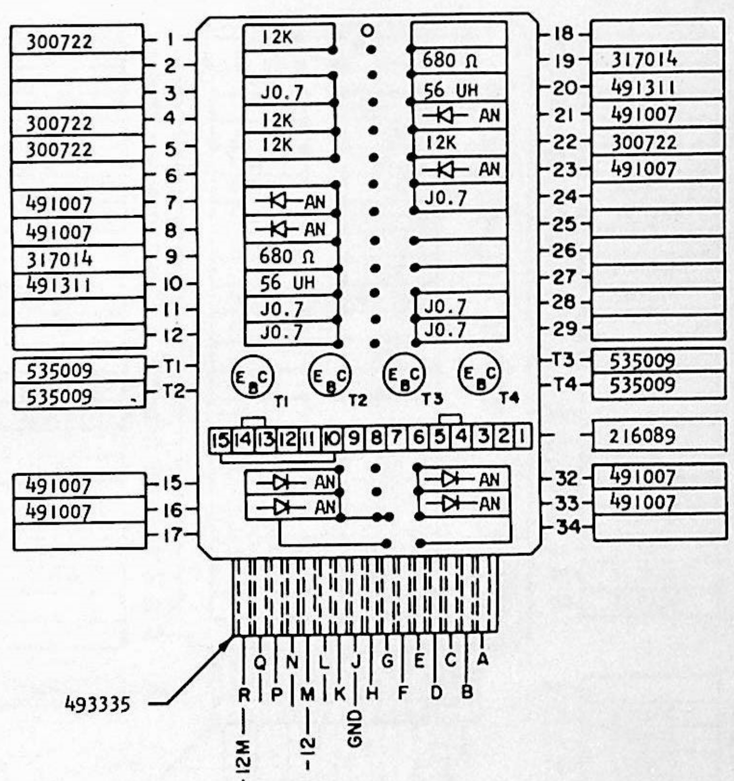
CTDL PNP TWO WAY GATE WITH COLLECTOR LOAD





SEQUENCE OF OPERATION

1. BOTH INPUTS TO A TRANSISTOR DOWN, TRANSISTOR ON OUTPUT UP
2. FOR DOWN OUTPUT, EITHER INPUT TO BOTH TRANSISTORS MUST BE UP
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN



COMPONENT SIDE

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
A,F D,N	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
B,G E,P	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C,H	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-CTDL PNP				
TWO WAY GATE WITH COLLECTOR LOAD					
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6 27 62	115599					

729900

C

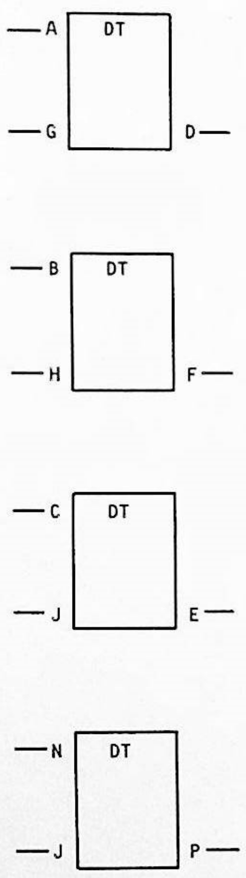
STANDARDS CODE
729815

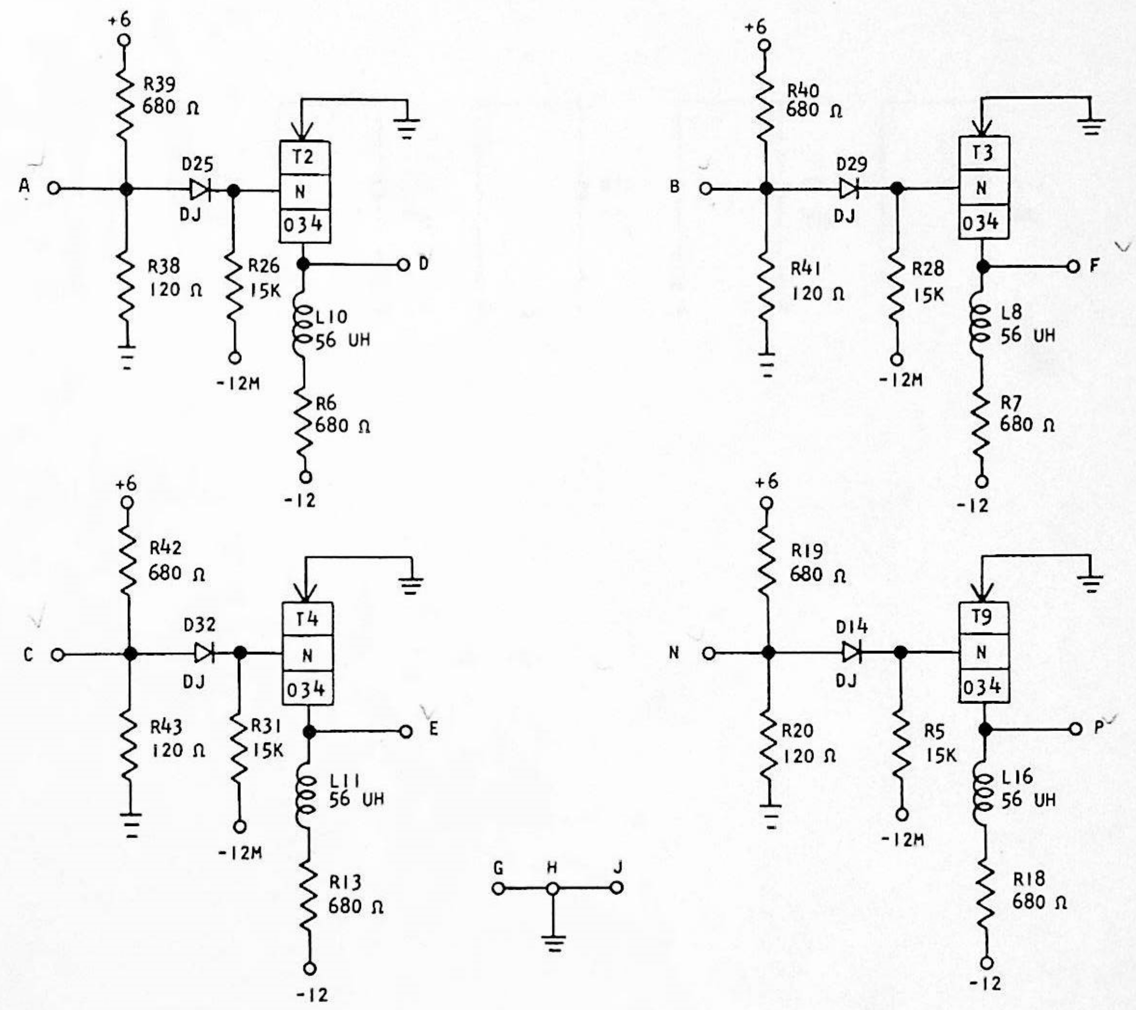
CARD CODE	729815
C E D -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370145

STANDARD CABLE TERMINATOR





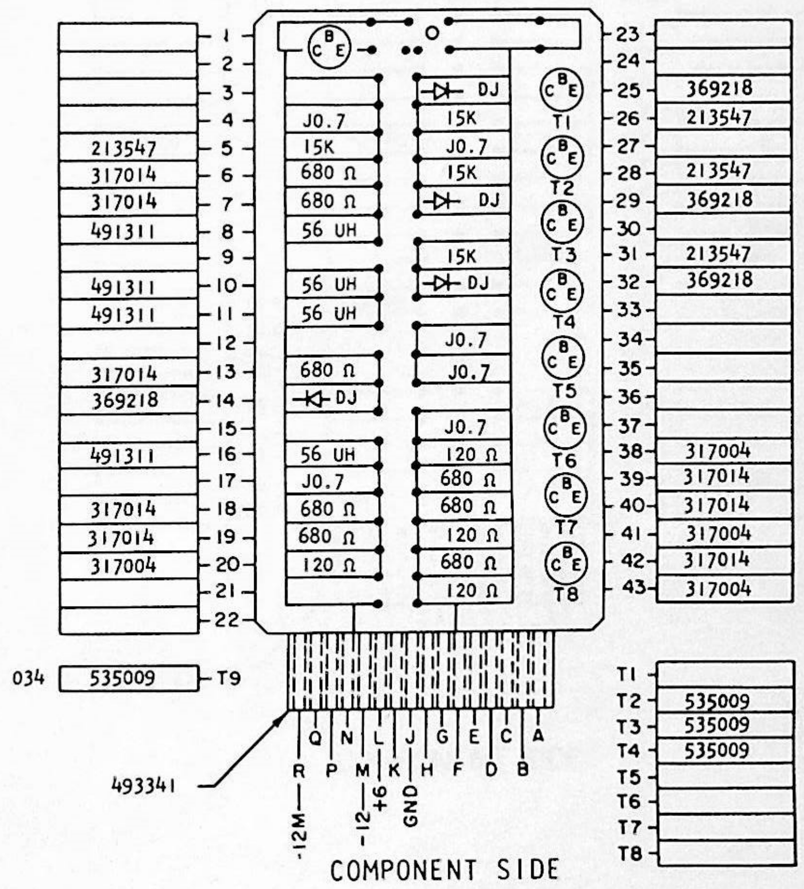
SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,B, C,N	N	INPUT		UP	0.65	1.03
				DOWN	-0.37	-4.46
G,H, J		GROUND				
D,F, E,P	U	OUTPUT		UP	-.54	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	115.0	220.0
TURN OFF	127.0	312.0



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - STANDARD CABLE TERMINATOR			4 - -62	115599					729815
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

FORM 85-001

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STANDARDS CODE

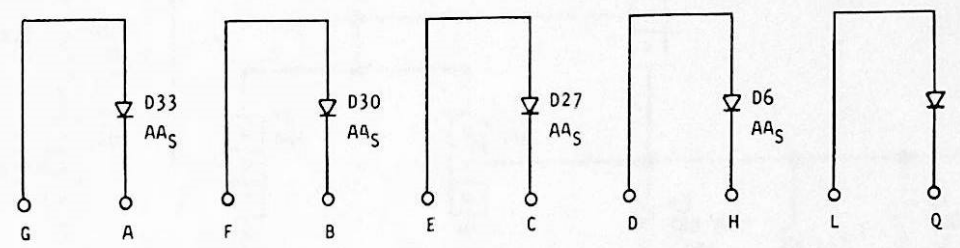
729902

CARD CODE	729902
A J T -	

REFERENCE DRAWING

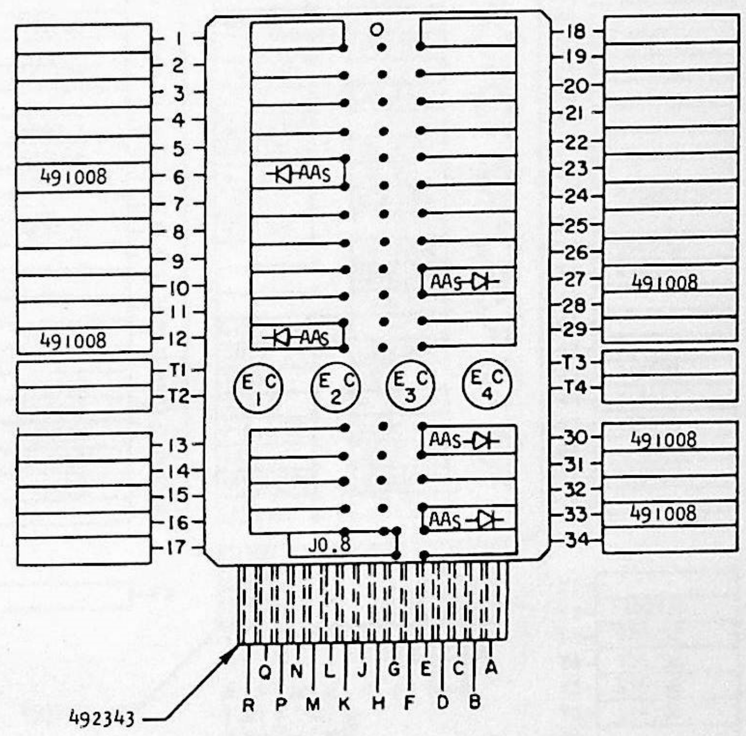
SEE PRODUCTION DRAWING 370564

ALLOY-DIODES, TYPE AA_S



APPLICATION NOTES

THESE DIODES CAN BE USED AS INPUTS TO EITHER P OR N TYPE LOGIC BLOCKS DEPENDING ON HOW THE PINS ARE CONNECTED.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - ALLOY - DIODES, TYPE AAS				/ · 62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729902

C

STANDARDS CODE

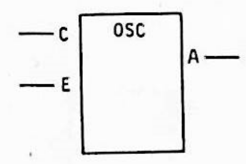
729903

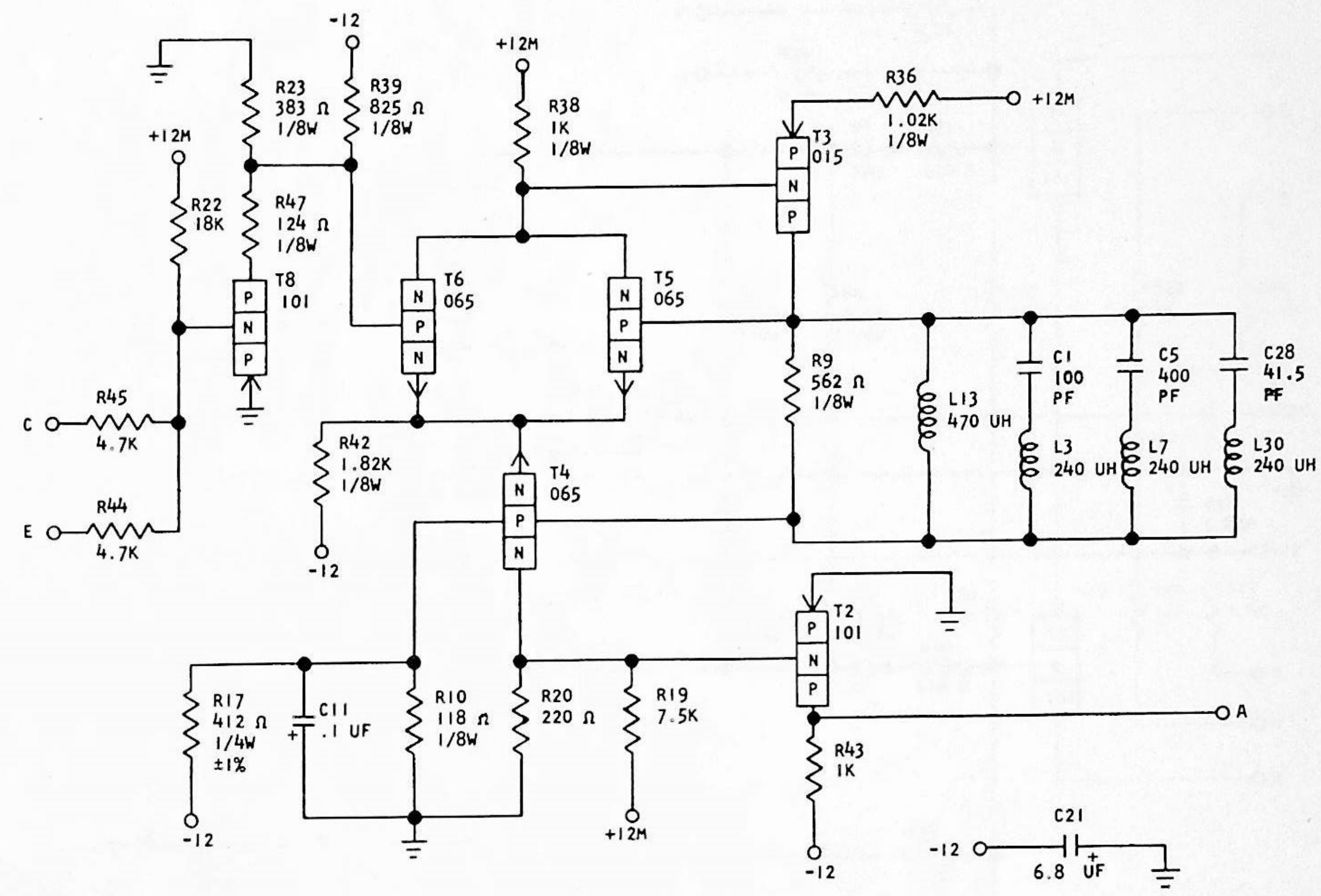
CARD CODE	729903
DAZ-	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370127

DIFF BASE - OSCILLATOR, 240 KC S LINE GATED





SEQUENCE OF OPERATION

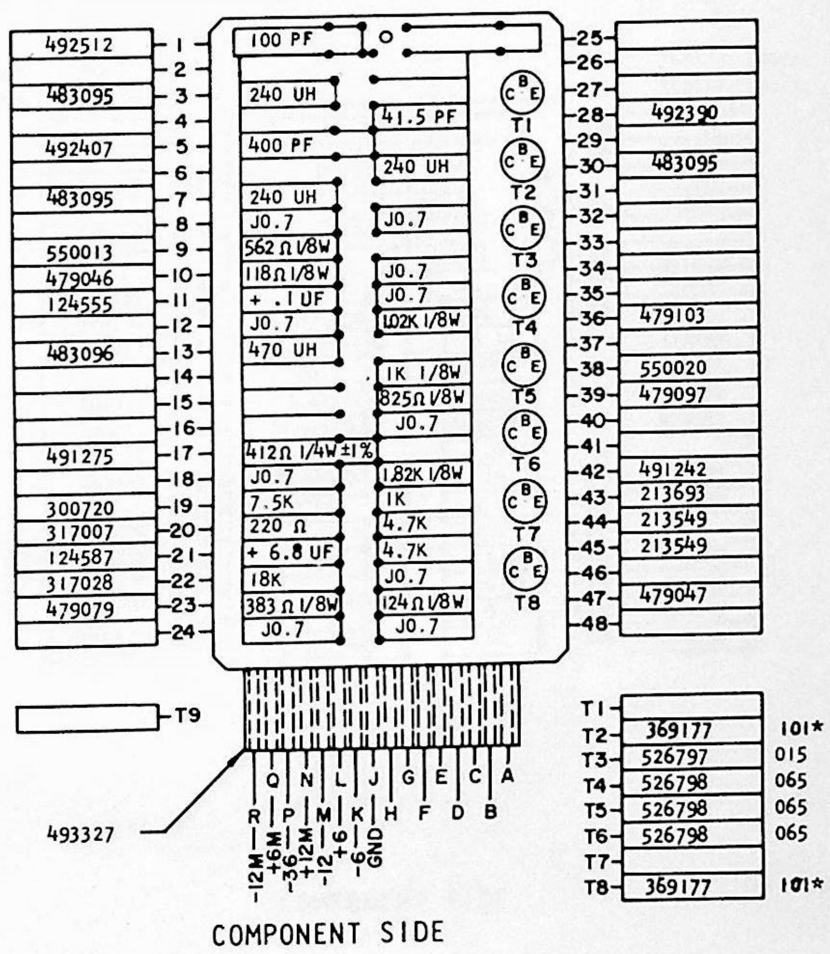
1. WHEN INPUTS CE ARE UP, T8 TURNS OFF OSCILLATOR TURNS ON
2. WHEN C OR E IS DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT	240 KC	UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	70	120
TURN OFF*	160	200

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-DIFF, BASE OSCILLATOR 240 KC S LINE GATED			' -62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729903

C

STANDARDS CODE

729904

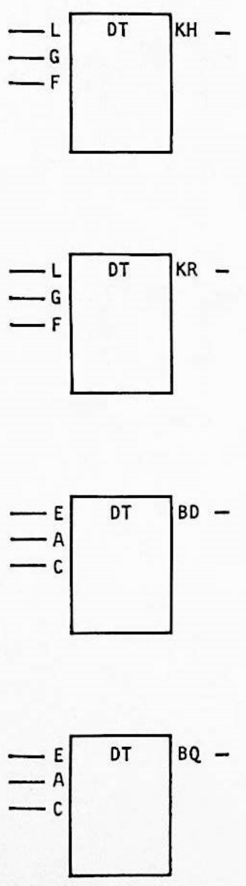
CARD CODE 729904

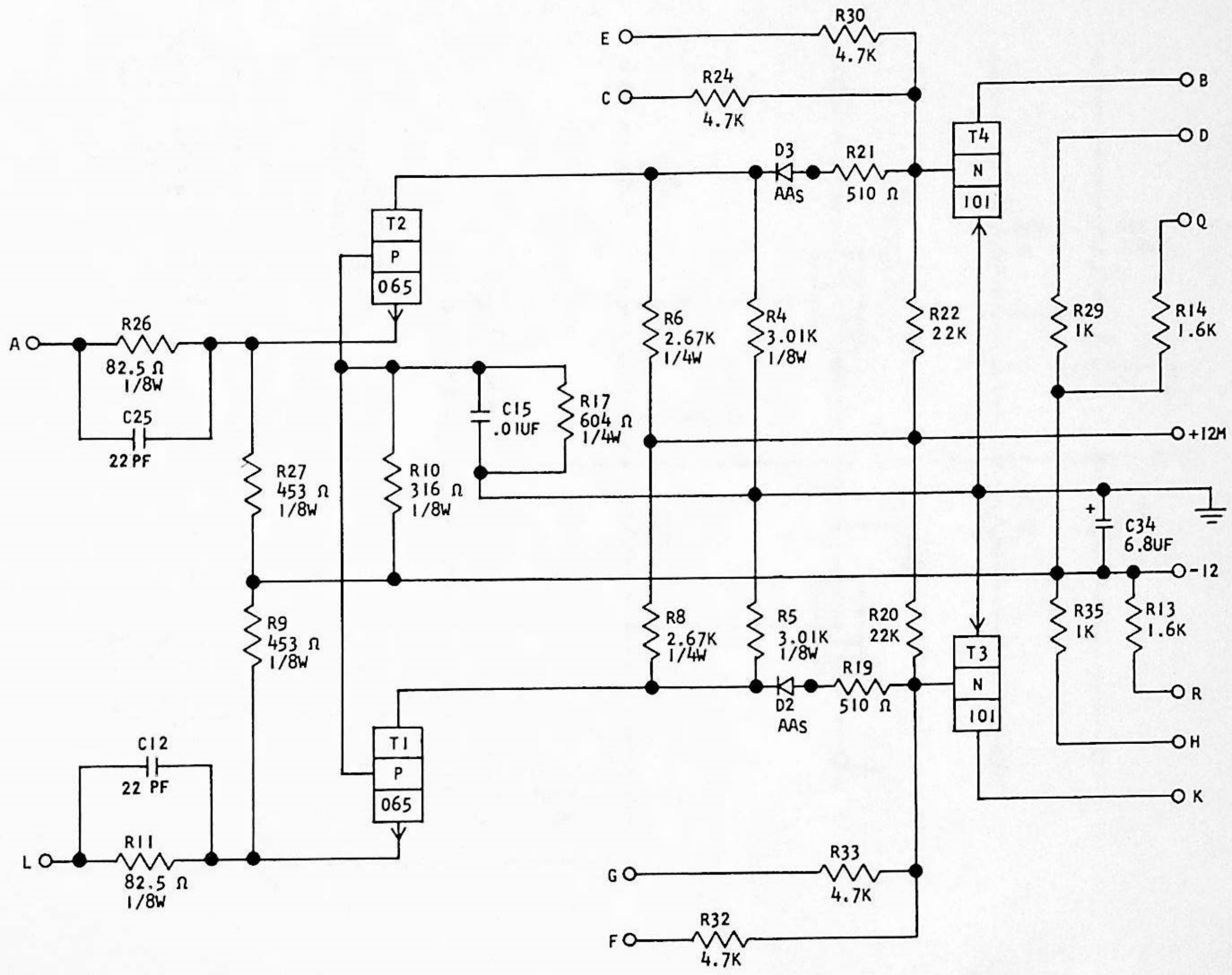
D B Z -

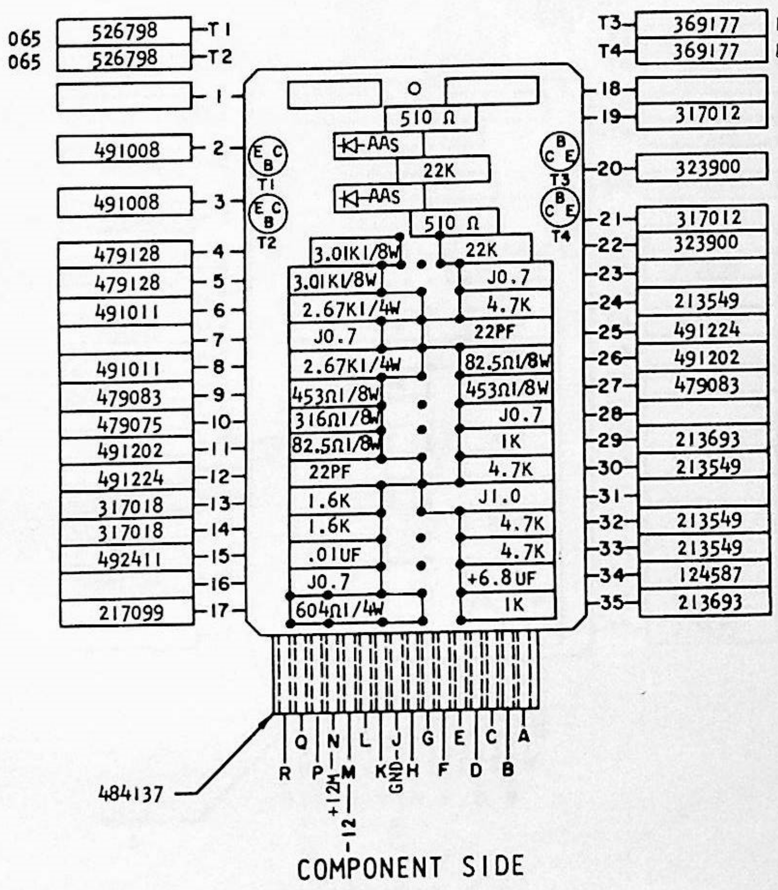
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370385

CONVERTER-DIFFUSED BASE P-LINE TO SDTRL, OR SDTDL







SEQUENCE OF OPERATION

INPUT A UP LEVEL, T2 CONDUCTS. THIS CAUSES T4 TO CONDUCT AND THE OUTPUT IS UP. EITHER PIN D OR Q IS TIED TO B DEPENDING IF SDTRL OR SDTDL BLOCKS ARE DRIVEN. THE OTHER CIRCUIT WITH INPUT L WORKS IN THE SAME MANNER. THE CIRCUIT ACCEPTS A P-LINE SIGNAL FROM THE COAXIAL LINE AND CONVERTS IT TO AN S LEVEL. THE GATES ACCOMPLISH A THREE WAY NOR FUNCTION; THAT IS, ANY NEGATIVE INPUT ON E, C OR OUTPUT OF T2 IN DOWN LEVEL WILL GIVE AN UP LEVEL OUTPUT FROM T4. IF THE 4.7K GATE IS NOT TO BE USED, IT MUST BE TIED TO GROUND.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
L,A	P	INPUT		UP	-5.6	5.2
				DOWN	-6.52	-6.4
E,C, F,G	S	GATE		UP	-.45	-.05
				DOWN	-6.87	-12.48
B,D, Q	S	OUTPUT		UP	-.45	-.05
				DOWN	-6.87	-12.48
R,H, K	S	OUTPUT		UP	-.45	-.05
				DOWN	-6.87	-12.48

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	50	80
TURN OFF	50	80

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CONV-DIFF BASE					6 21 -62	115599					
S P-LINE TO SDTRL, OR SDTDL												
DESIGN			MODEL									
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729904

FORM 82-001

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STANDARDS CODE

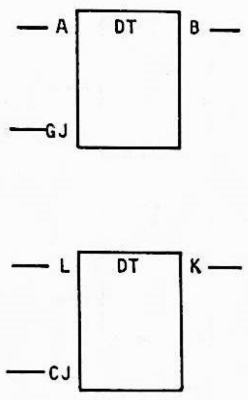
729905

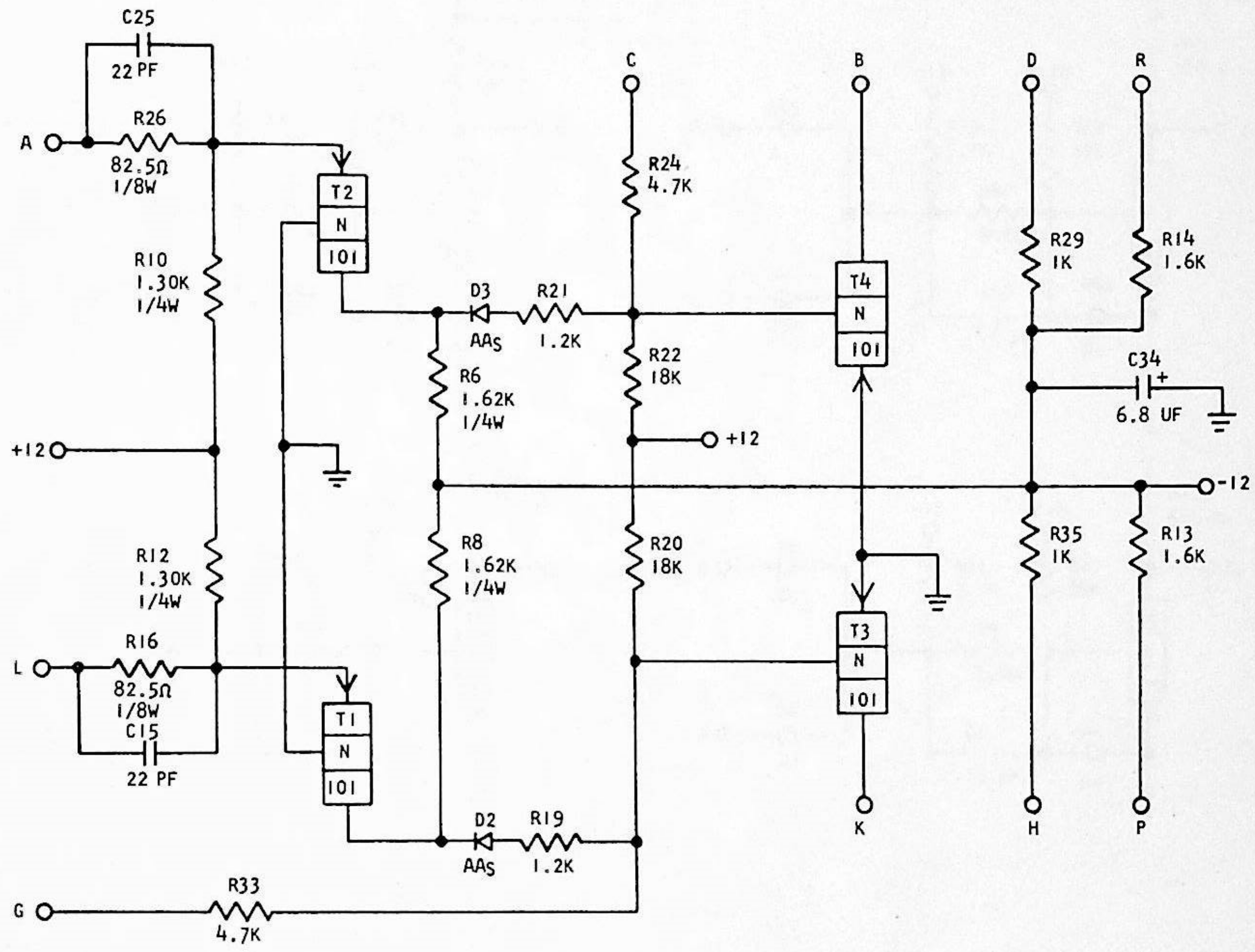
CARD CODE	729905
DCK -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370468

CONVERTER-DIFFUSED BASE N-LINE TO SDTRL OR SDTDL





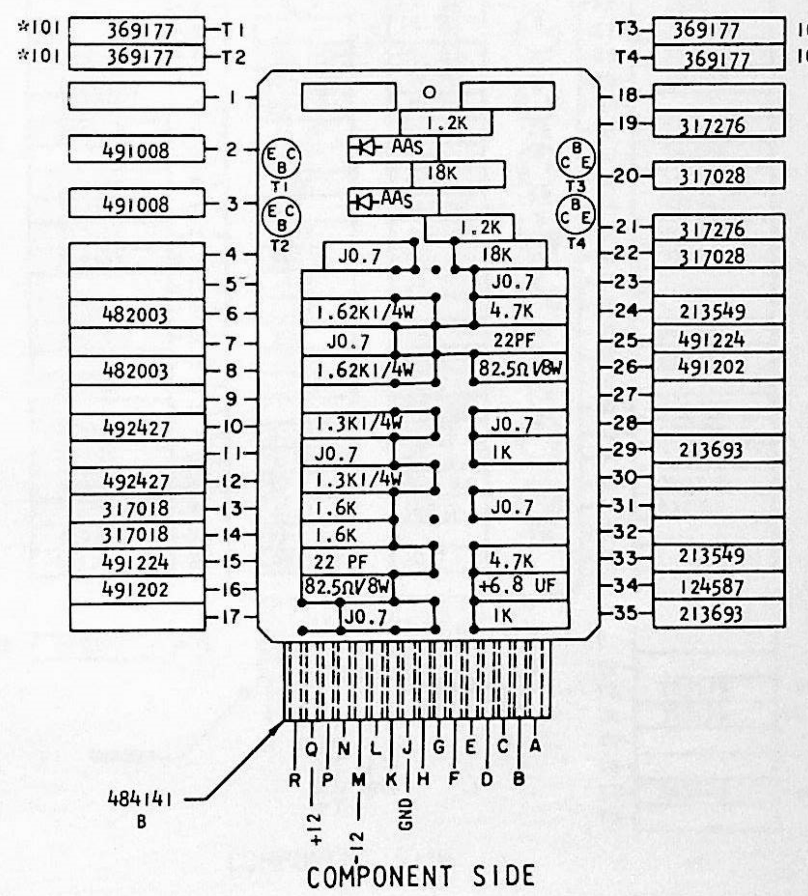
SEQUENCE OF OPERATION

1. WITH GATE INPUT UP OR TIED TO GROUND A DOWN INPUT AT A TURNS T2 OFF AND T4 ON AND GIVES AN UP OUTPUT
2. T4 AND T3 COLLECTORS MUST BE LOADED:
   1.6K RESISTOR FOR SDTDL OUTPUT
   1 K RESISTOR FOR SDTRL OUTPUT
3. IF THE 4.7K RESISTOR (PIN C, G) IS NOT TO BE USED, IT MUST BE TIED TO GROUND.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,L	N	INPUT		UP	+0.4	+0.5
				DOWN	-0.4	-0.8
G,C	S	GATE INPUT		UP	-0.5	-.05
				DOWN	-6.9	-12.5
B,K	S	SDTDL OUTPUT		UP	-.65	-0.1
				DOWN	-5.81	-12.5
B,K	S	SDTRL OUTPUT		UP	-0.45	-0.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	50.0	72.0
TURN OFF	60.0	72.0



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- CONVERTER-DIFFUSED BASE N-LINE TO SDTRL OR SDTDL			4-?-62	115599					729905
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

C

STANDARDS CODE	

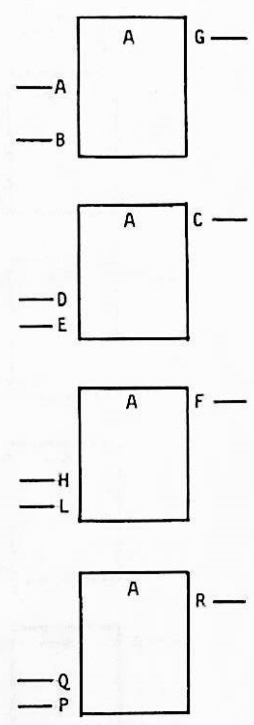
729906

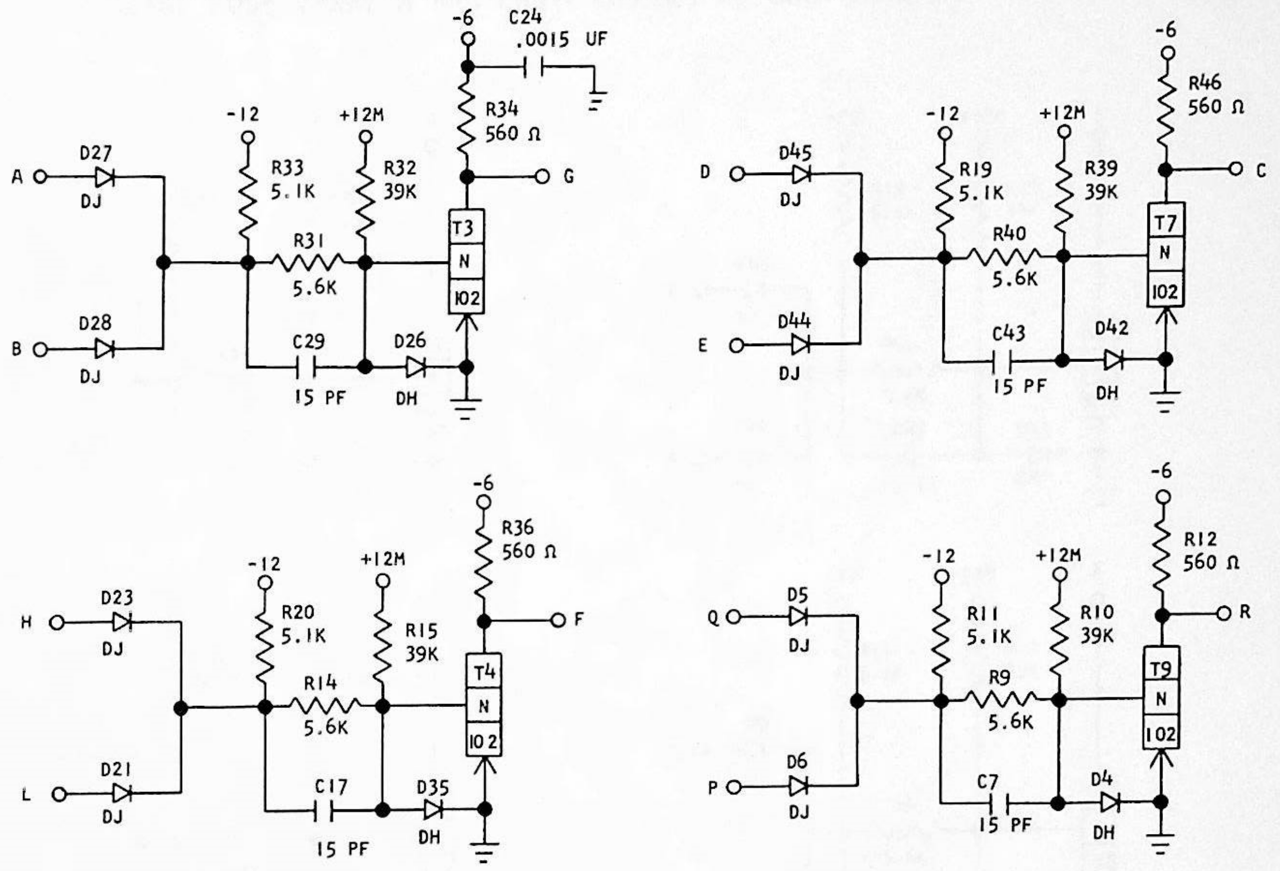
CARD CODE	729906
D E F -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370216

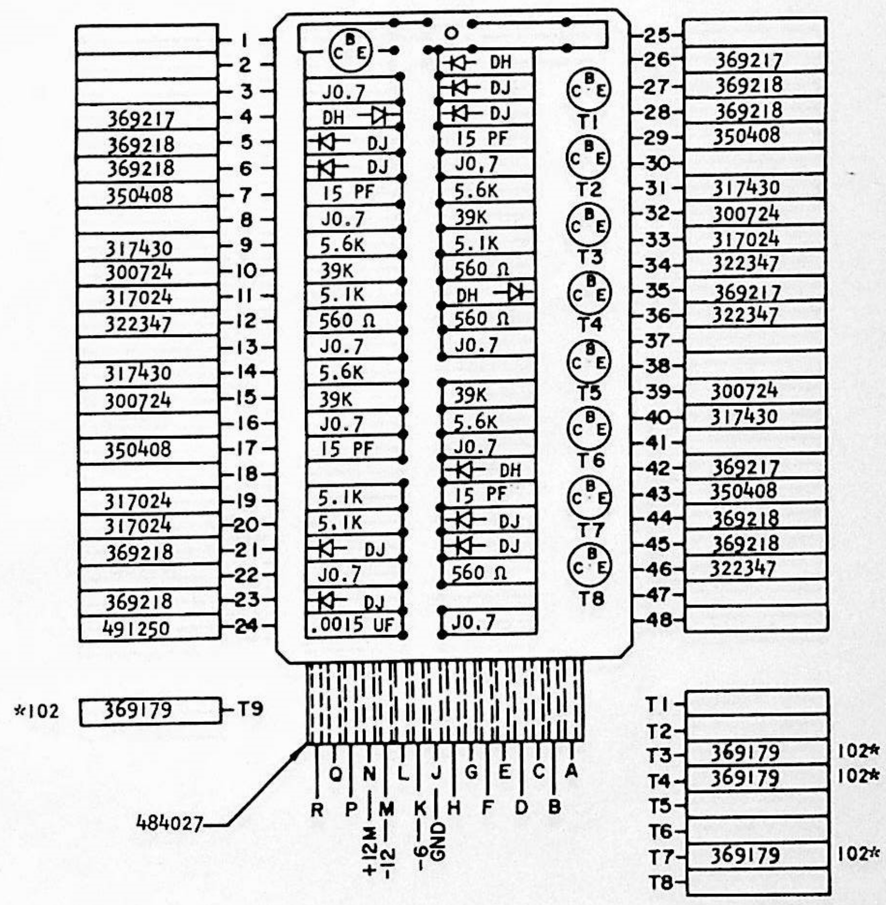
SDTDL - FOUR 2 WAY N AND LOGIC BLOCKS WITH LOADS





SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



COMPONENT SIDE

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,C, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8

DELAY: SDTDL - HIGH SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	5	30*
TURN OFF (NSEC)	10	80**

*THIS DELAY CAN INCREASE TO 75 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 120 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL-FOUR				62	115599					
	2-WAY N AND LOG BCKS WITH LOADS										
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729906

C

729907

STANDARDS CODE

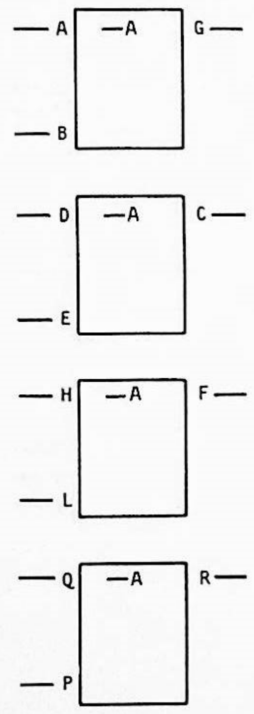
CARD CODE 729907

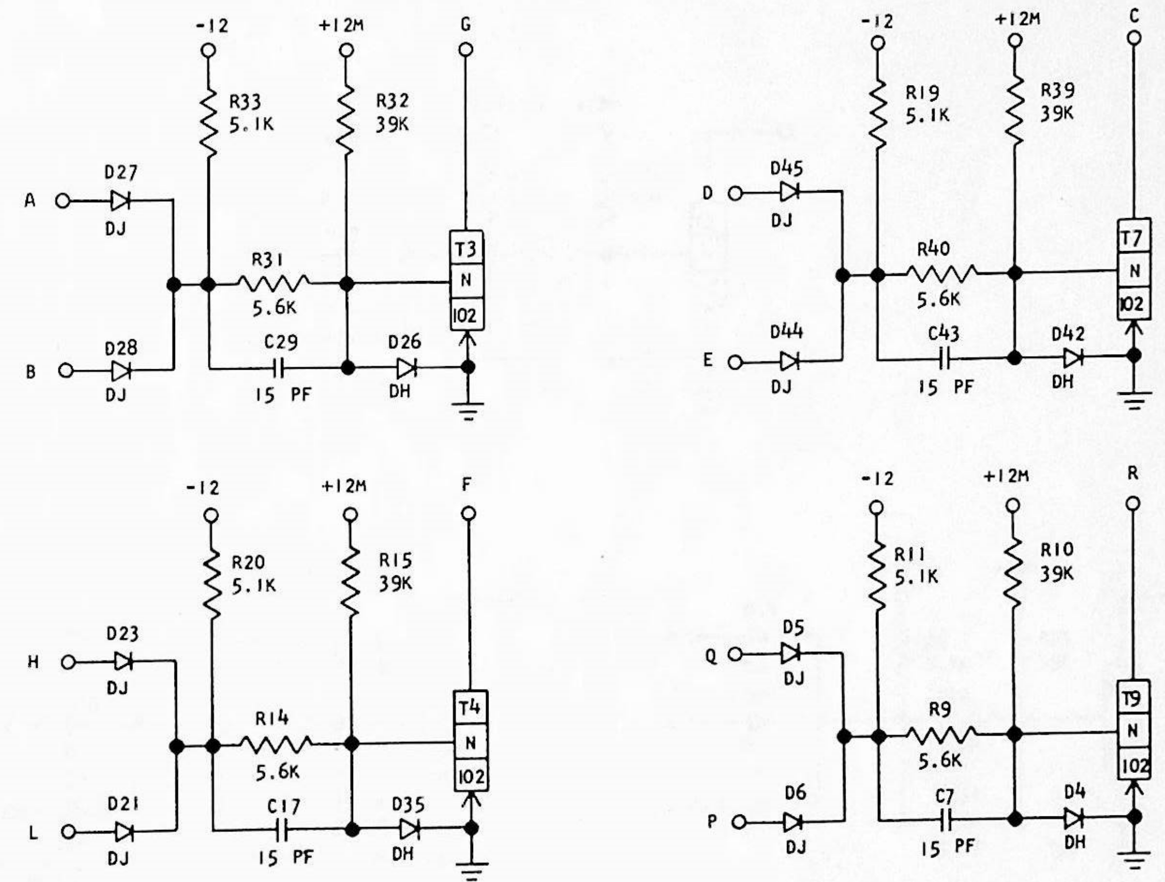
D E G -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370217

SDTDL FOUR 2-WAY N AND LOGIC BLOCKS WITHOUT LOADS

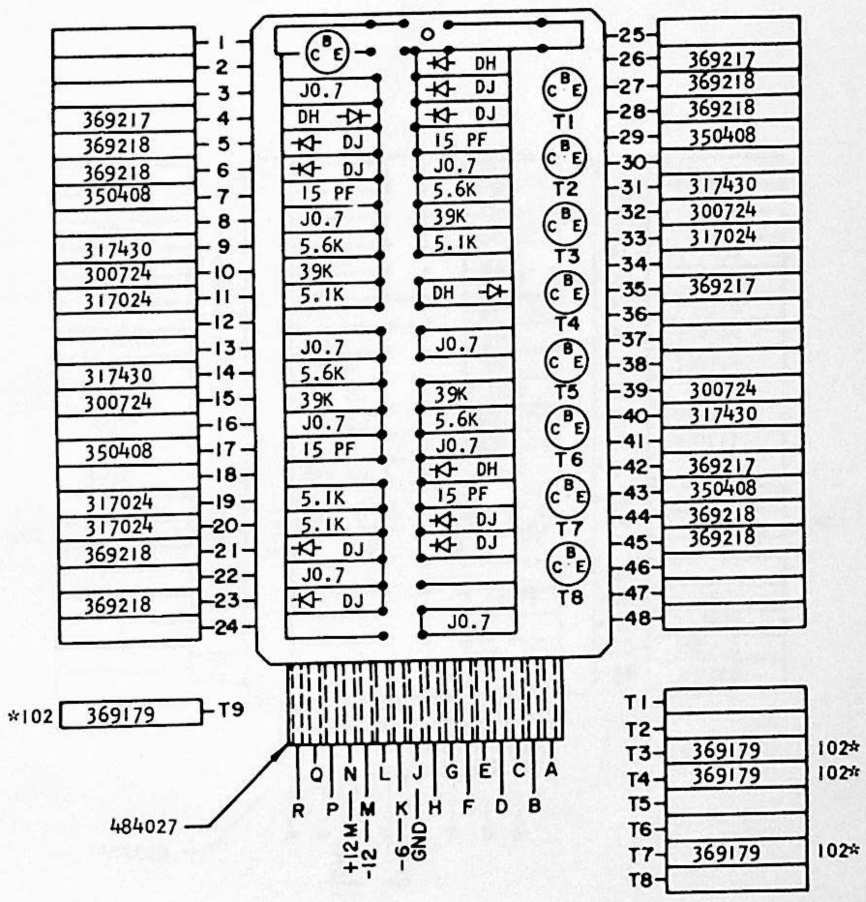




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,C, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8



COMPONENT SIDE

DELAY: SDTDL - HIGH SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	5	30*
TURN OFF (NSEC)	10	80**

*THIS DELAY CAN INCREASE TO 75 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 120 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 4 2-WAY N AND LOGIC BLOCKS WITHOUT LOADS			(' -62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729907

C

STANDARDS CODE

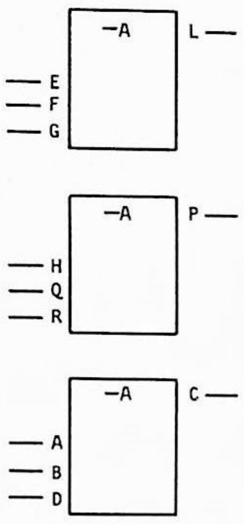
729908

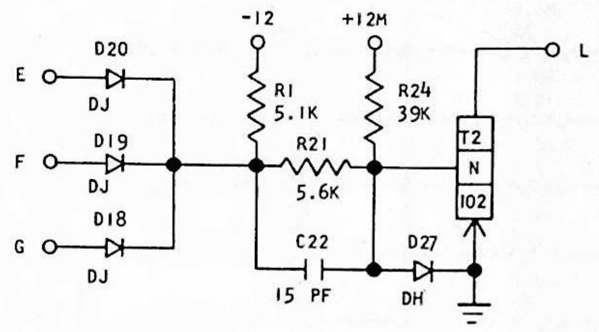
CARD CODE	729908
D E J -	

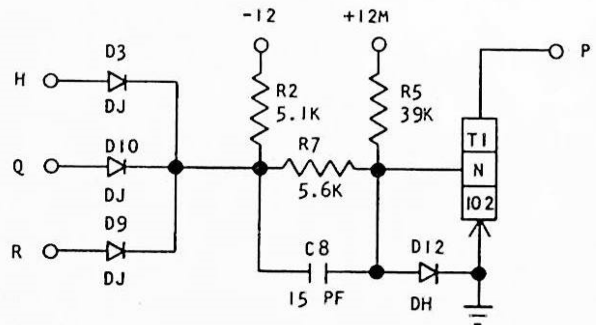
REFERENCE DRAWING

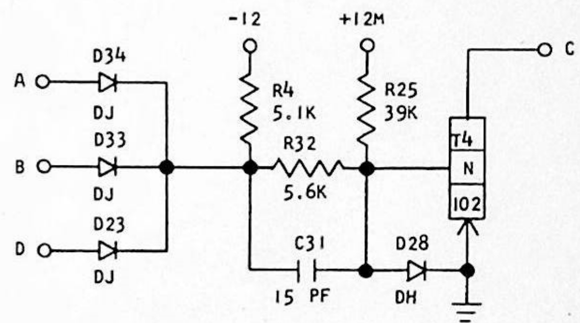
SEE PRODUCTION DRAWING 370219

SDTDL THREE 3-WAY N AND LOGIC BLOCKS WITHOUT LOADS





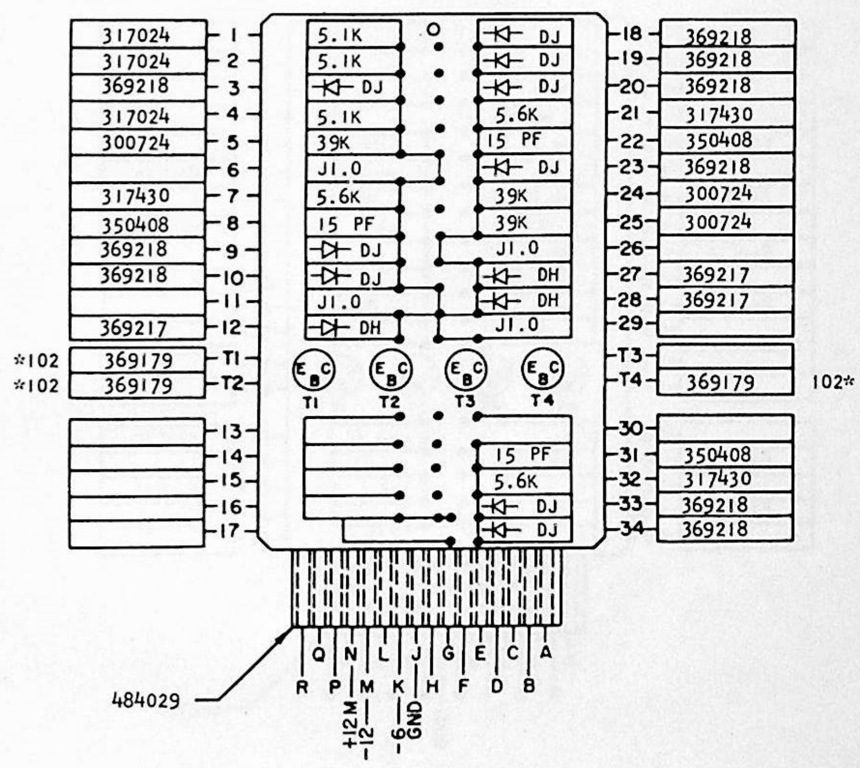




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
E, H, A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F, Q, B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G, R, D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L, P, C	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8



COMPONENT SIDE

DELAY: SDTDL - HIGH SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	5	30*
TURN OFF (NSEC)	10	80**

*THIS DELAY CAN INCREASE TO 75 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 120 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-SDTDL THREE				
3-WAY N AND LOG BCKS WITHOUT LDS					
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
4 [illegible] 62	115599					

729908

FORM 82-001

C

STANDARDS CODE

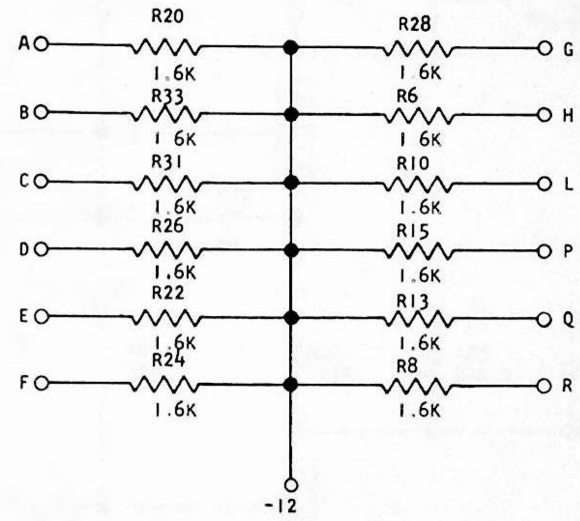
729909

CARD CODE	729909
D F J -	

REFERENCE DRAWING

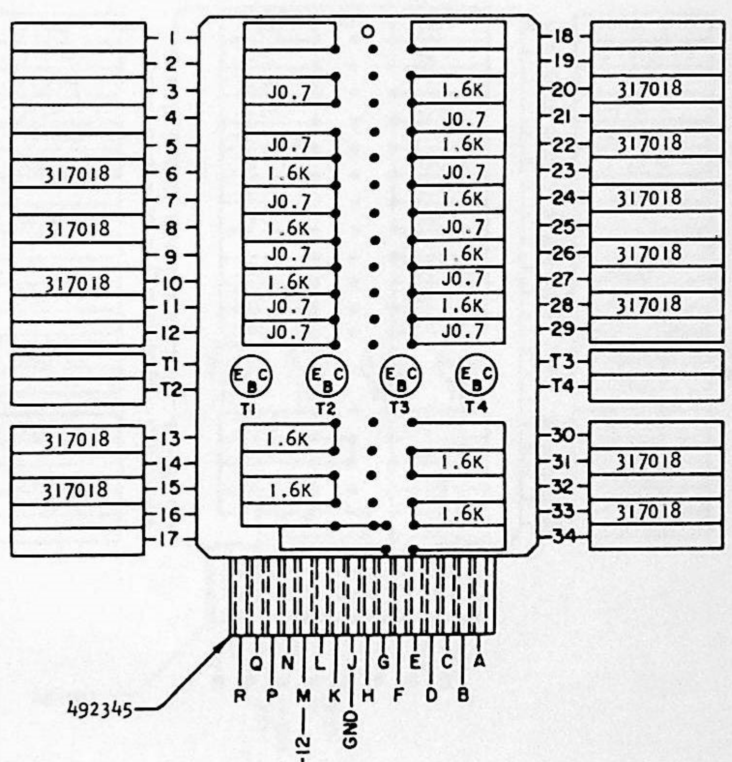
SEE PRODUCTION DRAWING 370232

TDL & TRL LOAD CARD



APPLICATION

1. USED FOR TDL AND TRL COLLECTOR LOADING
2. MAY BE USED IN PARALLEL IN CERTAIN APPLICATIONS.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-TDL AND TRL LOAD CARD			4-27-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729909

C

STANDARDS CODE

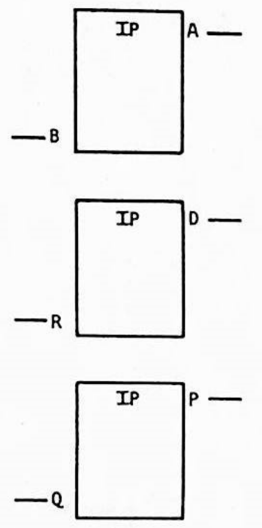
729910

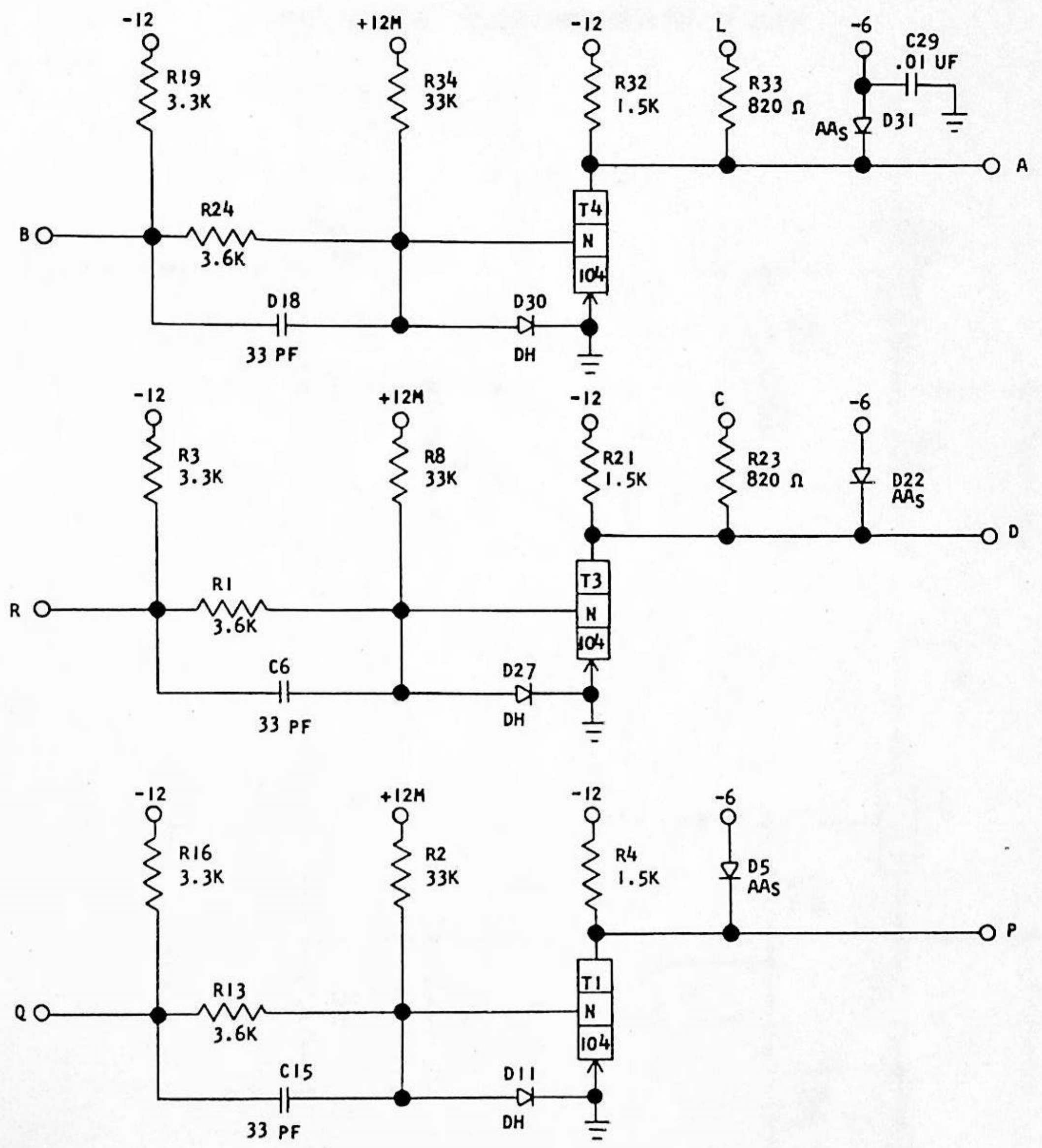
CARD CODE	729910
D F Q -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370225

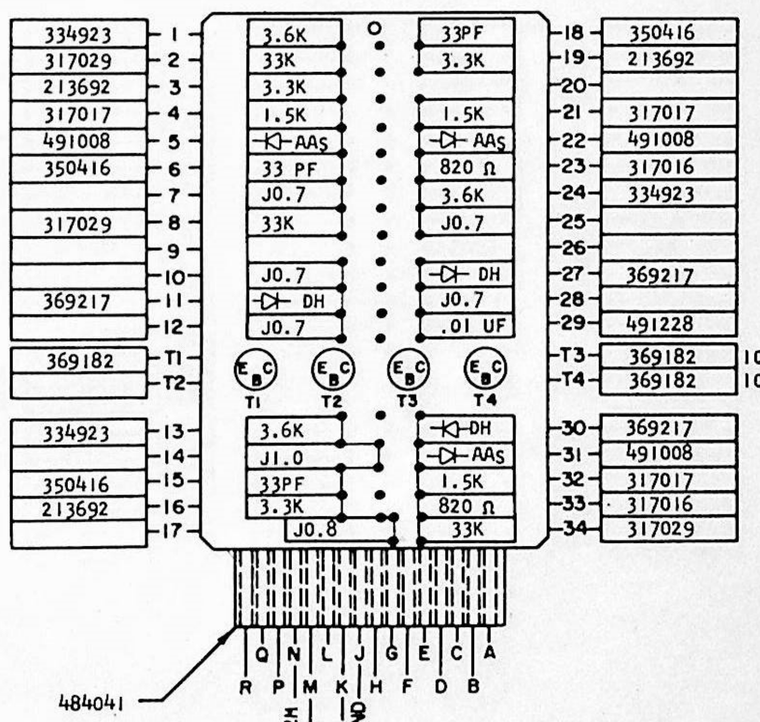
SDTDL INVERTING POWER DRIVER





SEQUENCE OF OPERATION

1. INPUT DOWN, TRANSISTOR ON, OUTPUT UP
2. INPUT UP, TRANSISTOR OFF, OUTPUT DOWN
3. 820Ω COLLECTOR RESISTOR RETURNED TO -12 VOLTS WHEN DRIVING NEGATIVE "OR" INPUTS OF DOUBLE LEVEL LOGIC BLOCKS & WHEN DRIVING TRIGGER AC INPUTS



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B, R, Q	Y	INPUT		UP	-0.65	-0.10
				DOWN	-7.14	-5.84
A, D, P	Y	OUTPUT		UP	-0.65	-0.10
				DOWN	-6.06	-6.8

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	10.0**	50.0*
TURN OFF	14.0**	35.0*

*ASSUMES LOAD OF 10 LOGIC BLOCKS AND TR INPUT OF 70 NSEC AND INPUT TF OF 135 NSEC.
**ASSUMES LOAD OF 4 LOGIC BLOCKS AND INPUT TR OF 35 NSEC AND INPUT TF OF 70 NSEC.

RISE TIME	16.0	70.0# TO 110.0##
FALL TIME	75.0	125.0## TO 190.0#

#OCCURS WHEN DRIVING TRIGGERS
##OCCURS WHEN DRIVING LOGIC BLOCKS

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL				6-29-62	115599					
	INVERTING POWER DRIVER										
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729910

C

STANDARDS CODE

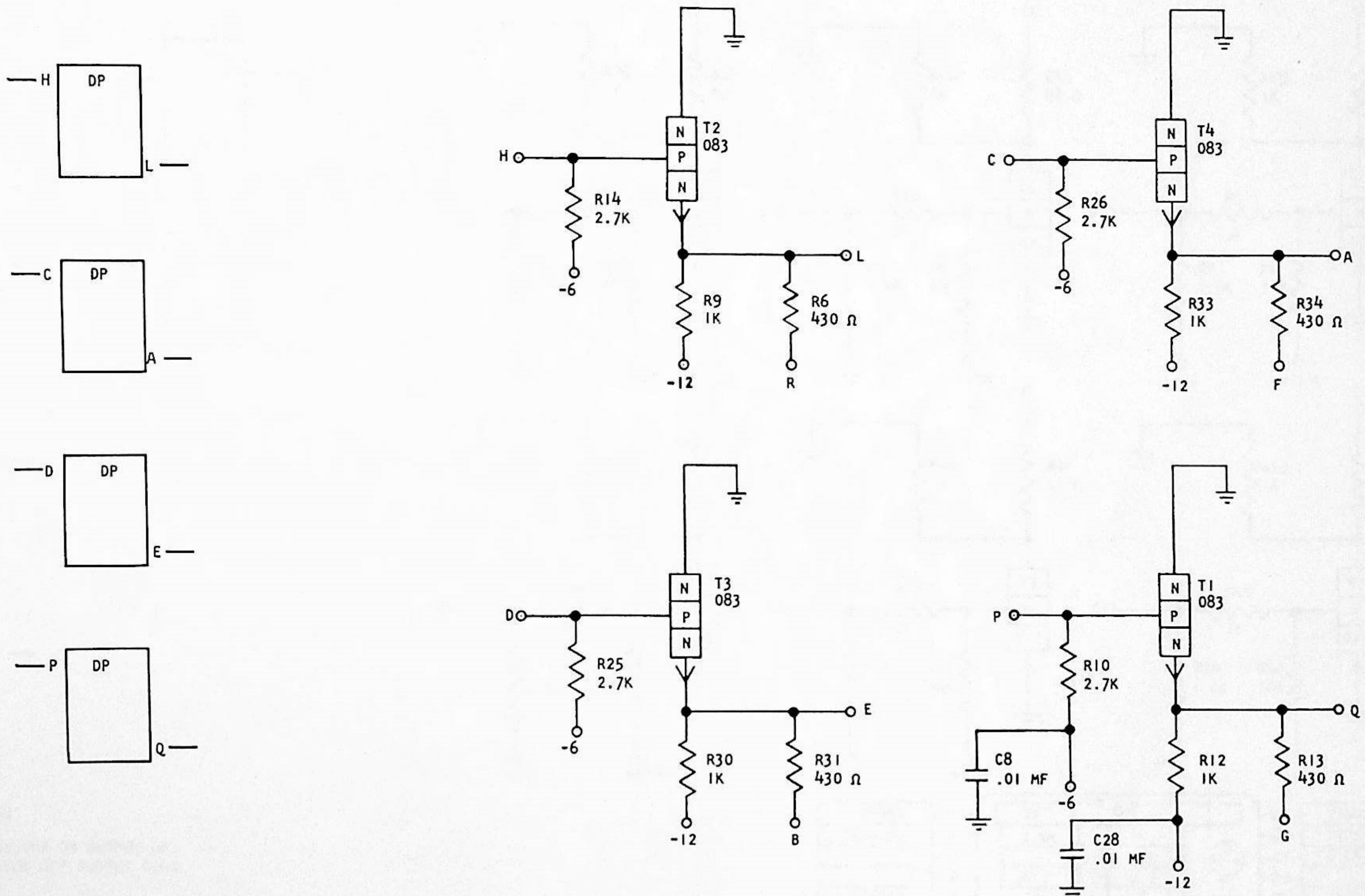
729911

CARD CODE	729911
D F R -	

REFERENCE DRAWING

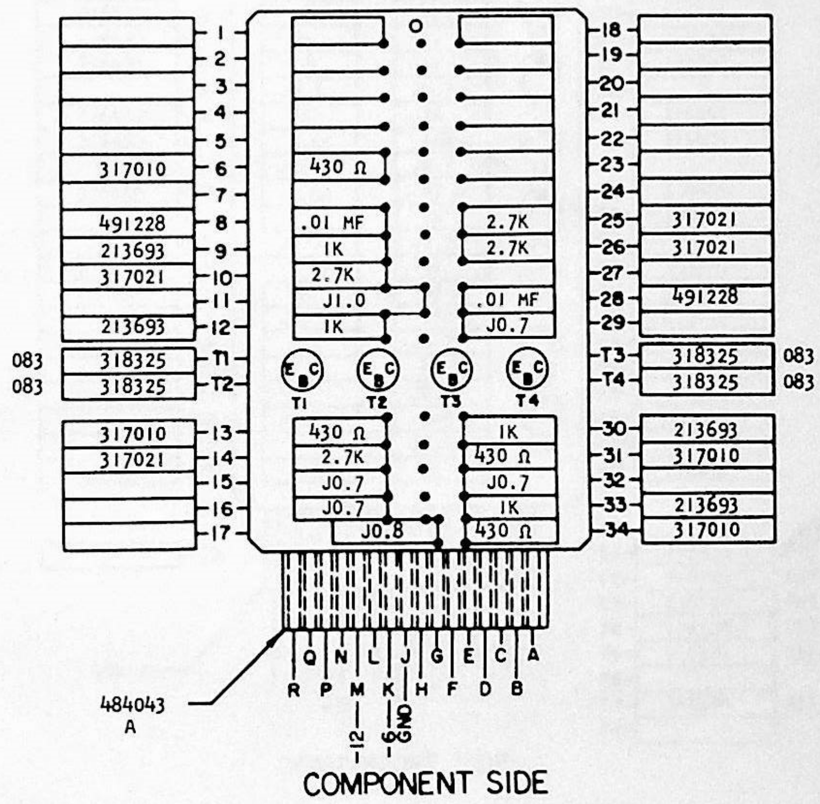
SEE PRODUCTION DRAWING 370226

SDTDL NON-INVERTING POWER DRIVER



SEQUENCE OF OPERATION

1. OUTPUT WILL FOLLOW INPUT
2. PINS R, F, B, AND G MAY BE CONNECTED TO PIN M (-12) FOR CERTAIN APPLICATIONS.



PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
H,C, D,P	Y	INPUT		UP	-0.65	-0.10
				DOWN	-5.81	-8.8
L,A, E,Q	Y	OUTPUT		UP	-1.10	-0.22
				DOWN	-7.30	-5.83

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	6.0	20.0
TURN OFF	6.0	28.0

OUTPUT RISE AND FALL TIMES ARE WITHIN ±10 NSEC'S OF THE INPUT RISE AND FALL TIMES, RESPECTIVELY.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-SDTDL				
NON-INVERTING POWER DRIVER					
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
[illegible]-62	115599					

729911

C

STANDARDS CODE

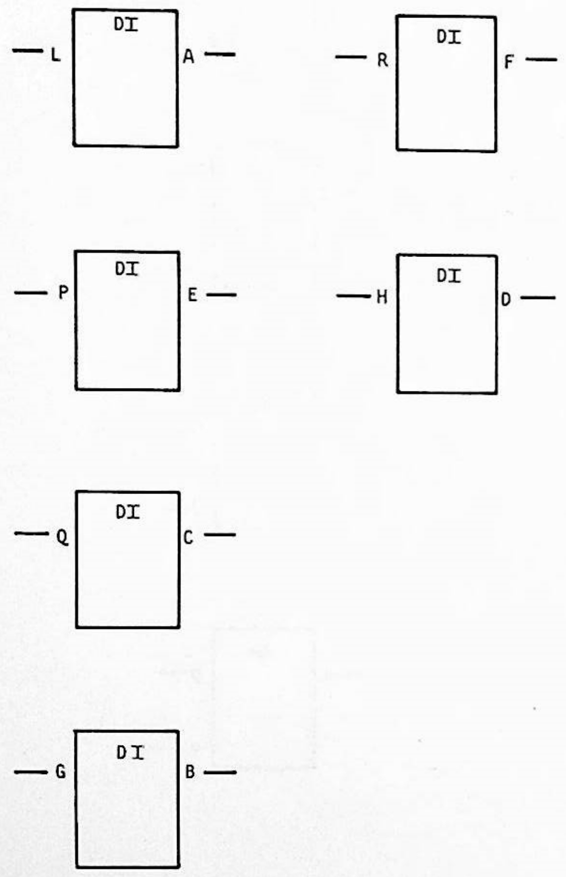
729912

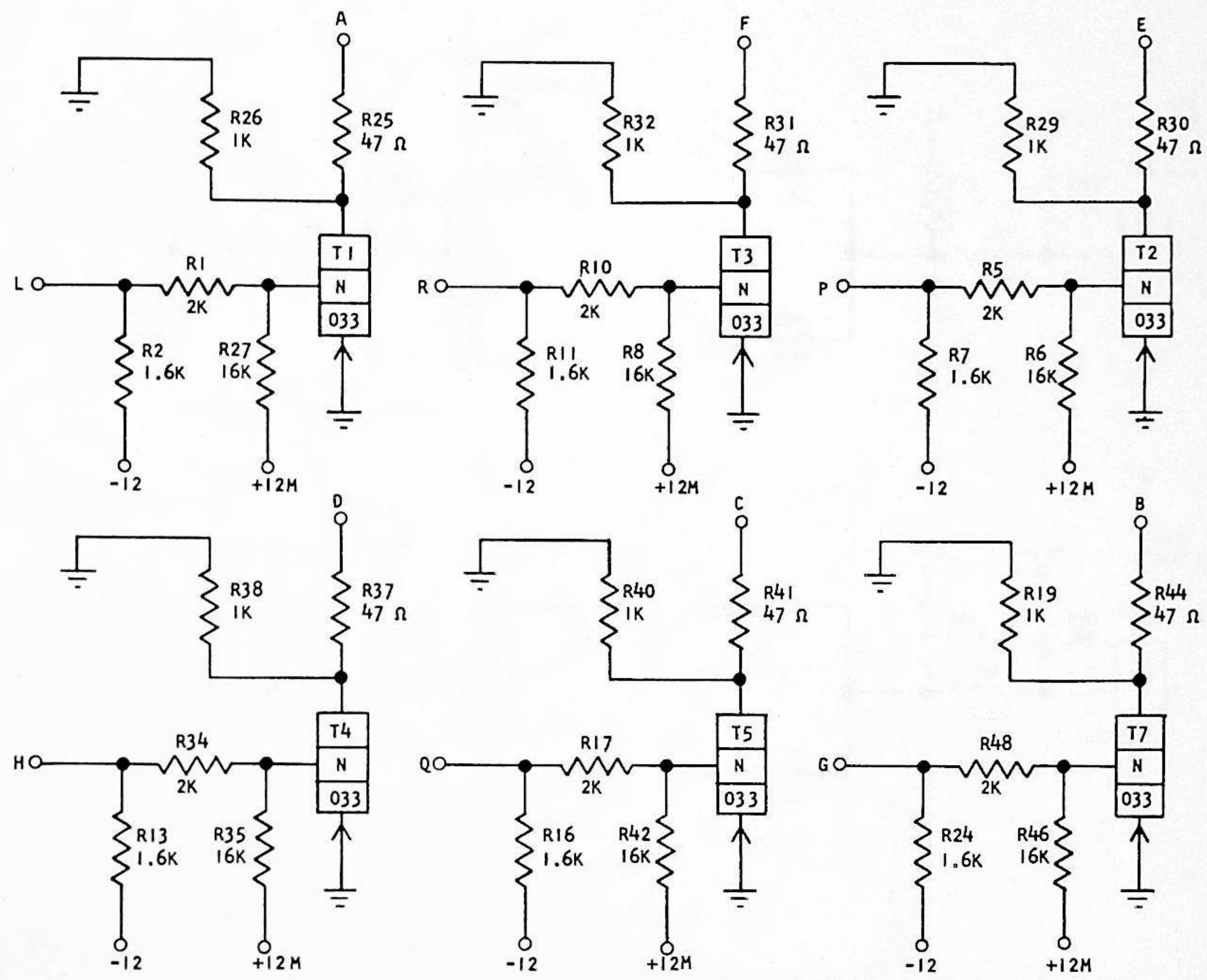
CARD CODE	729912
D G S -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370347

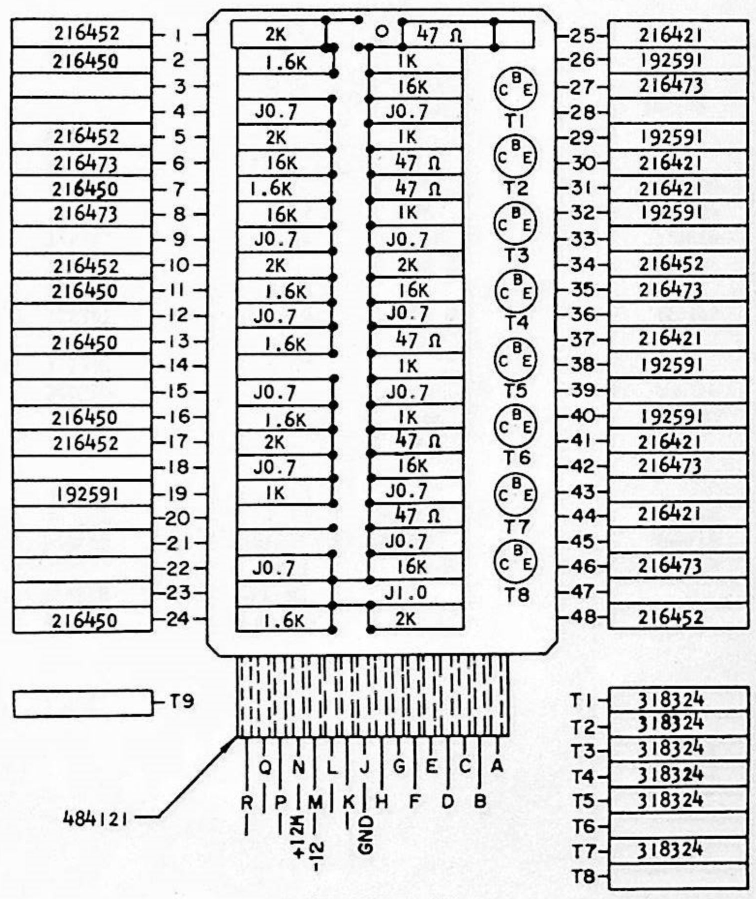
SDTDL INDICATOR DRIVER





SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
L,R,P, H,Q,G	Y	INPUT		UP	-0.65	0.10
				DOWN	-5.81	-7.64
A,F,E, D,C,B	S	OUTPUT		UP	-1.67	
				DOWN	-9.62	

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- SDTDL			4-27-62	115599					
	INDICATOR DRIVER									
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729912

C

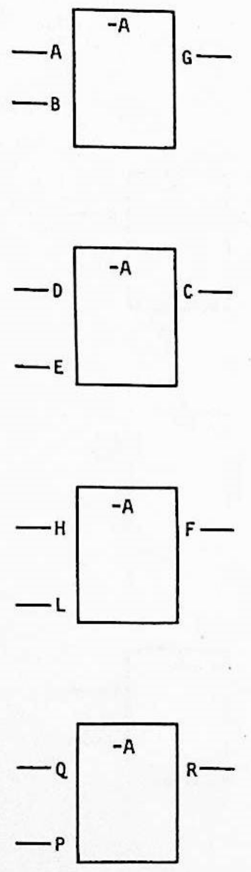
729913	STANDARDS CODE

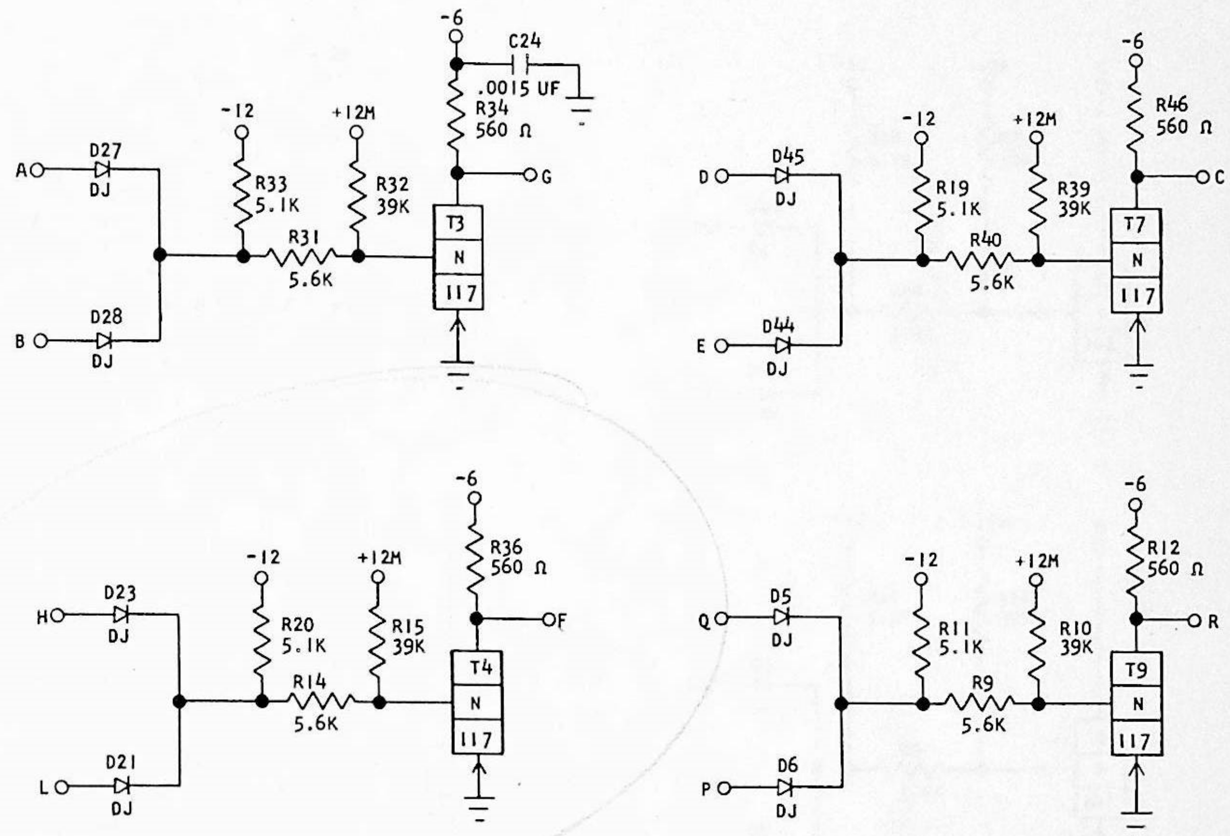
CARD CODE	729913
D G T -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370380

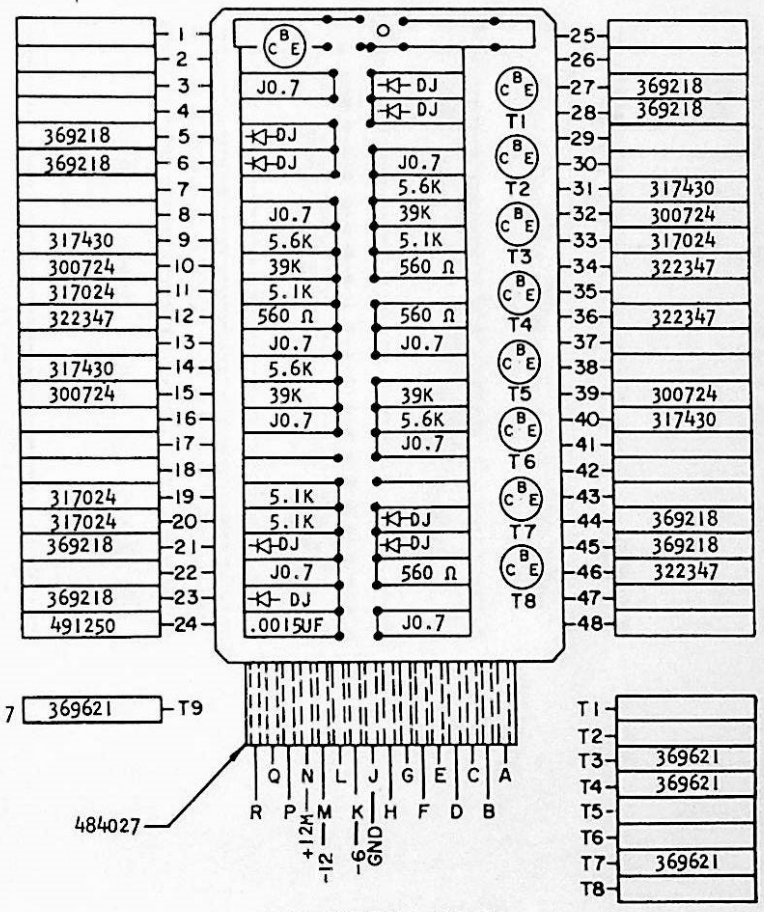
SDTDL-2 WAY LOGIC BLOCK LOW SPEED WITH LOADS





SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,C, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-SDTDL-2-WAY				4 19 62	115599					
LOGIC BLOCK LOW SPEED WITH LOADS										
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW LIG	3-17-62							
APPRO		CHECK								

729913

C

FORM 22-001

STANDARDS CODE

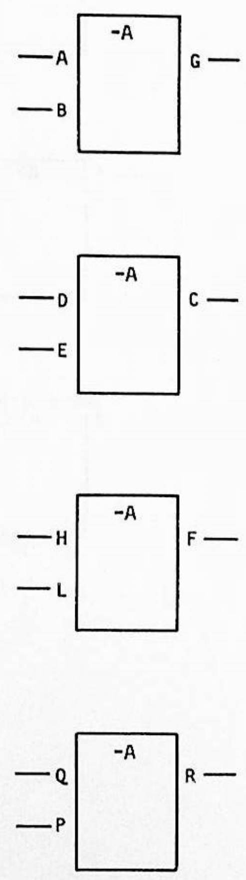
729914

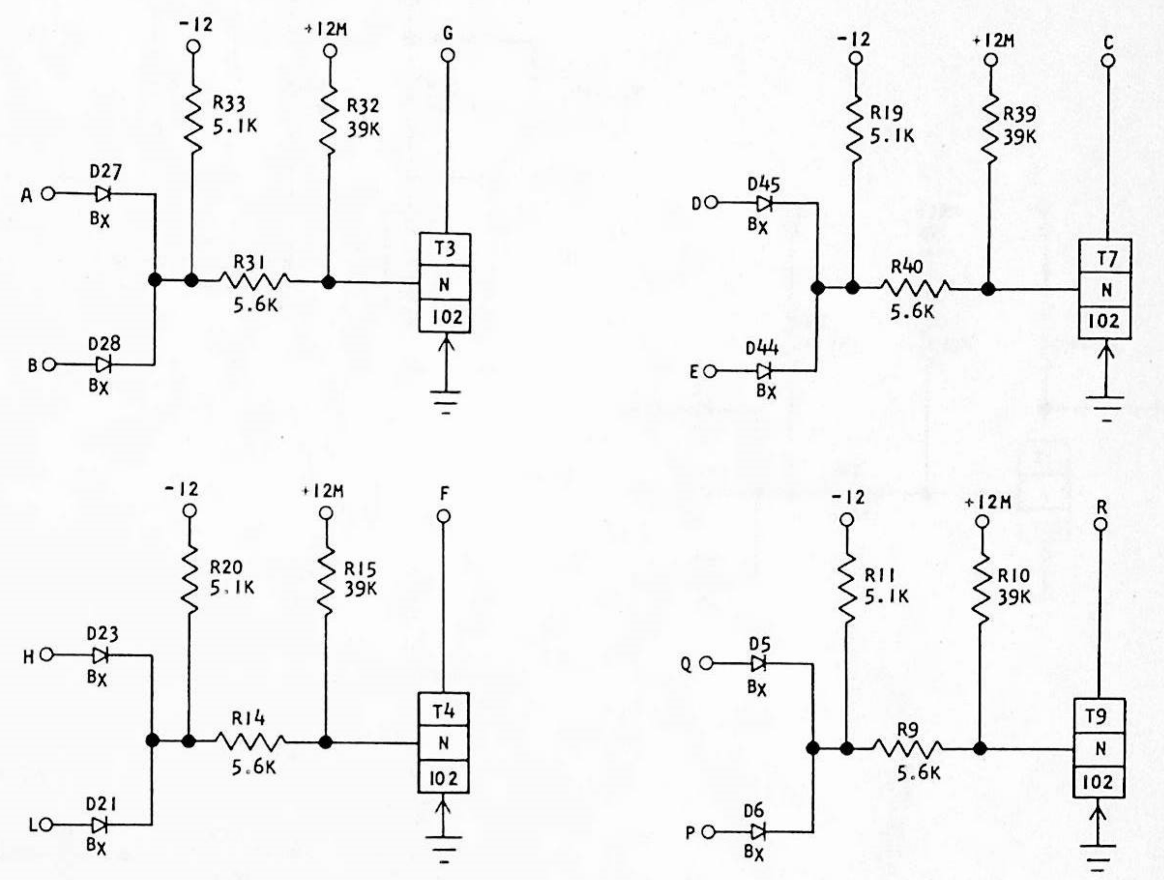
CARD CODE	729914
D G U -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370379

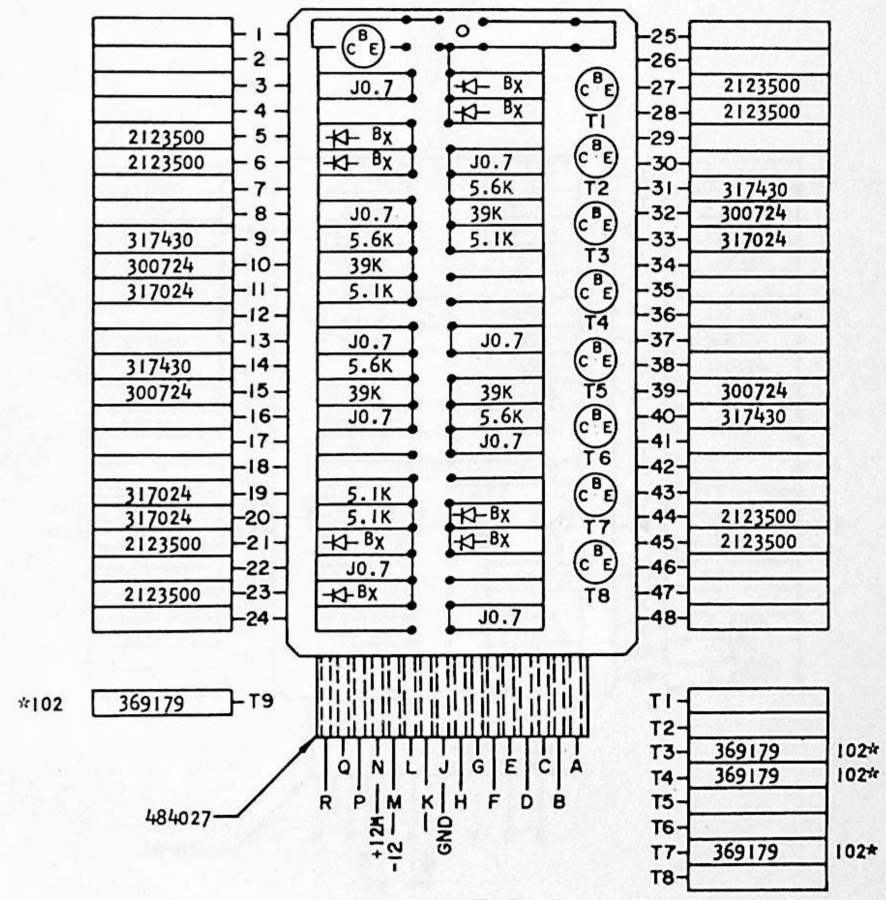
SDTDL 2-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS





SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT DOWN TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,D, H,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,E, L,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,C, F,R	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 2-WAY			6 ?Y -62	115599					
	LOGIC BCK LOW SPEED WITHOUT LOADS									
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729914

FORM 83-001

C

STANDARDS CODE	

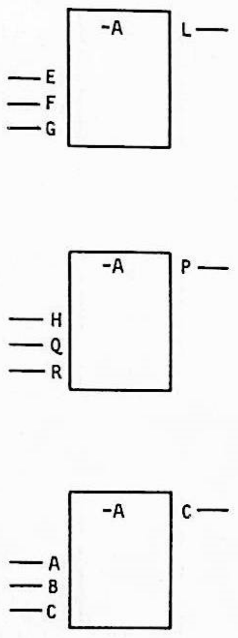
729915

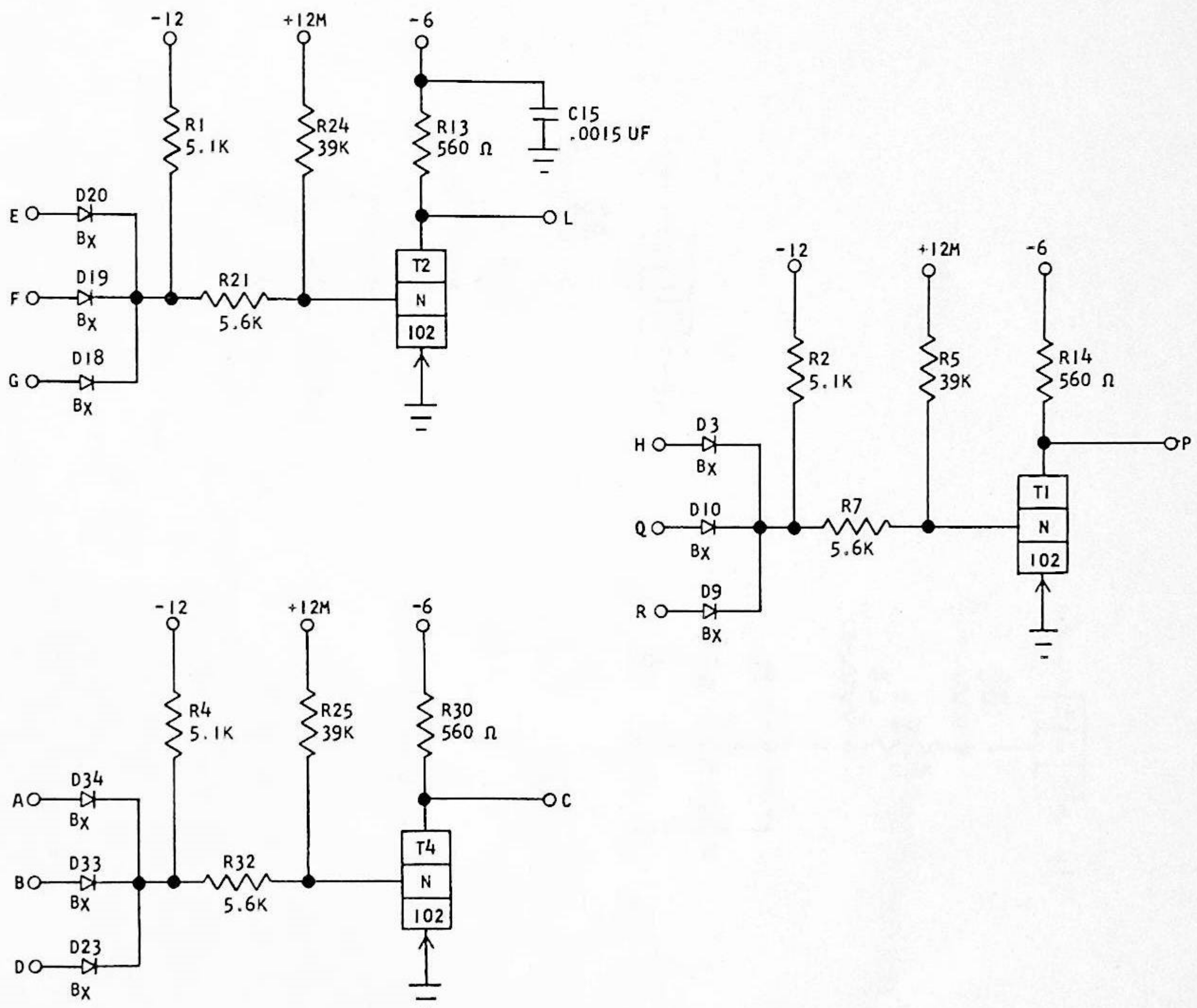
CARD CODE	729915
D G V -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370378

SDTDL - 3-WAY LOGIC BLOCK LOW SPEED WITH LOADS





SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
E,H, A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F,Q, B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,R, D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L,P, C	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

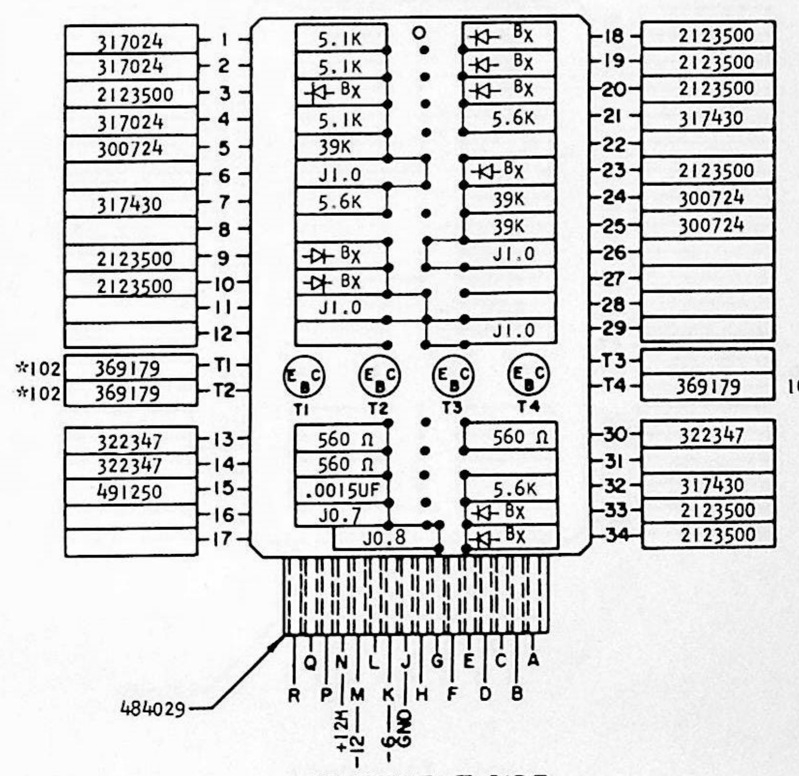
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL-3-WAY				6-29-62	115599					
LOGIC BLOCK LOW SPEED WITH LOADS											
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729915

C

STANDARDS CODE

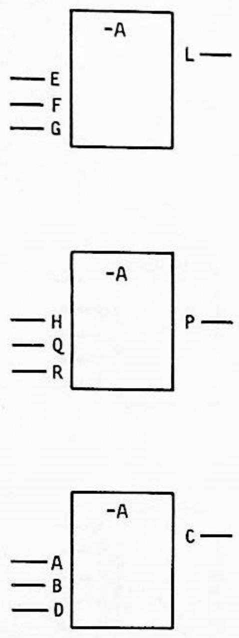
729916

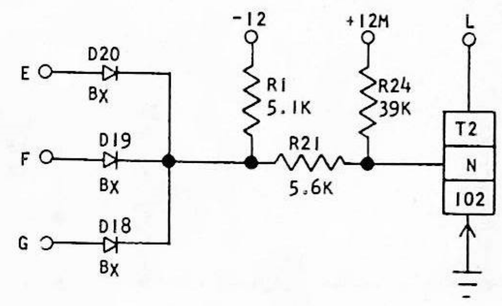
CARD CODE	729916
D G W -	

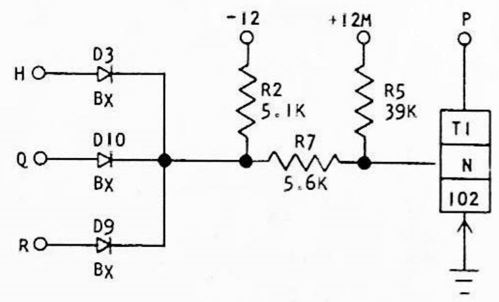
REFERENCE DRAWING

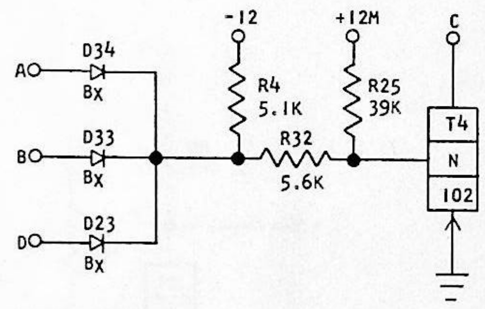
SEE PRODUCTION DRAWING 370377

SDTDL 3-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS



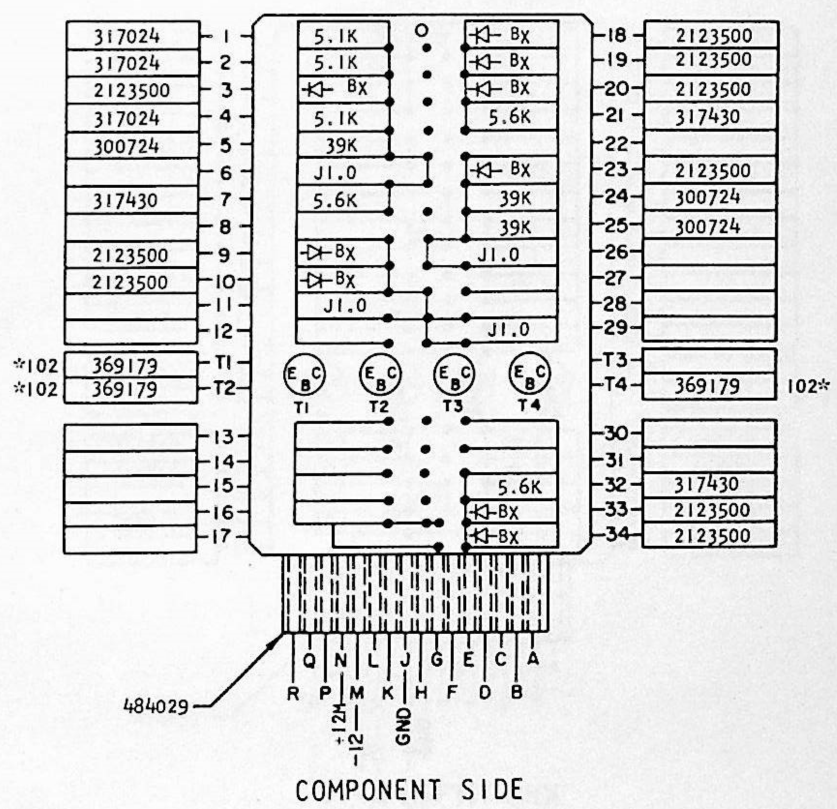






SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	MAX
E,H, A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F,Q, B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,R, D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L,P, C	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-SDTDL 3-WAY				-62	115599					
LOGIC BCK LOW SPEED WITHOUT LOADS										
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729916

FORM 85-001

C

STANDARDS CODE

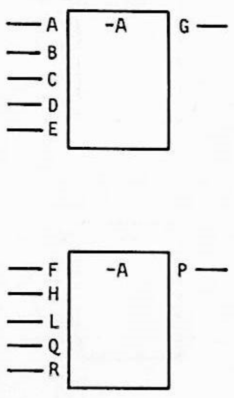
729917

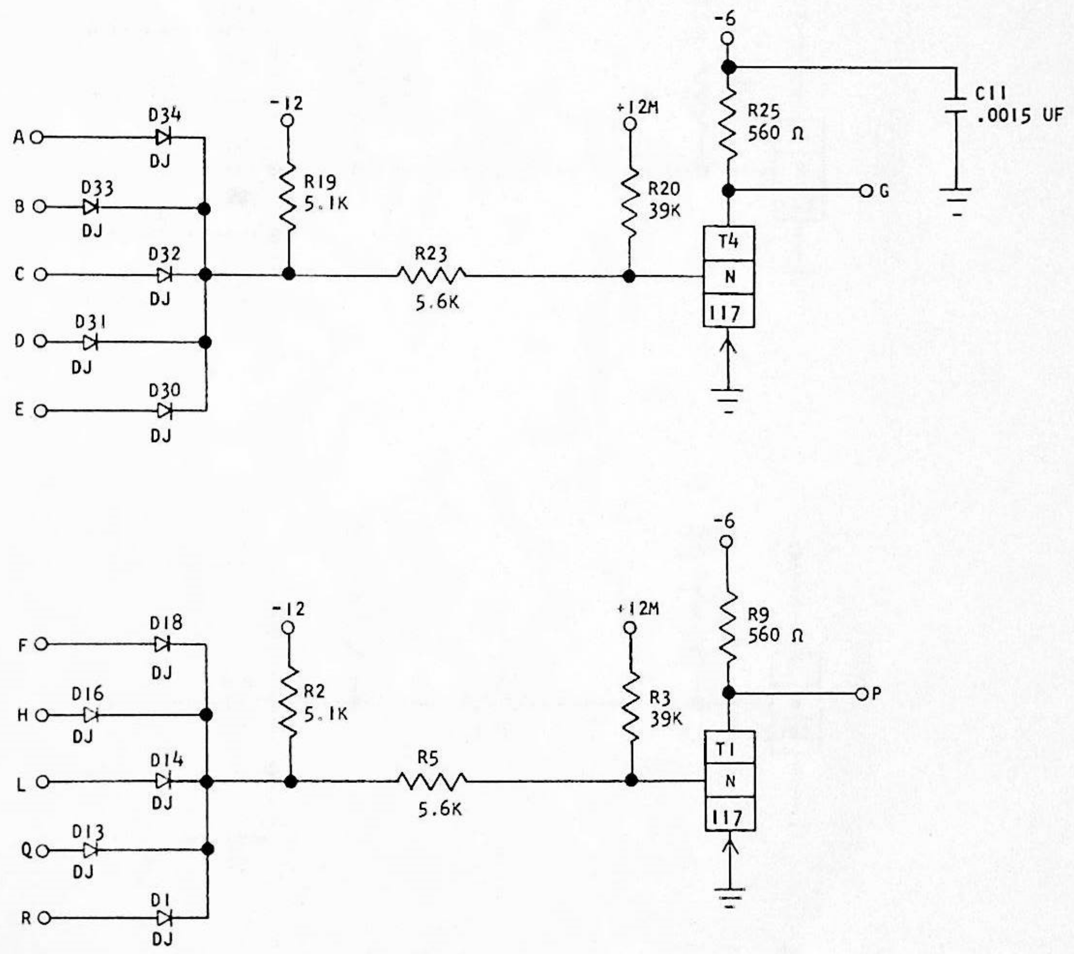
CARD CODE	729917
D G X -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370376

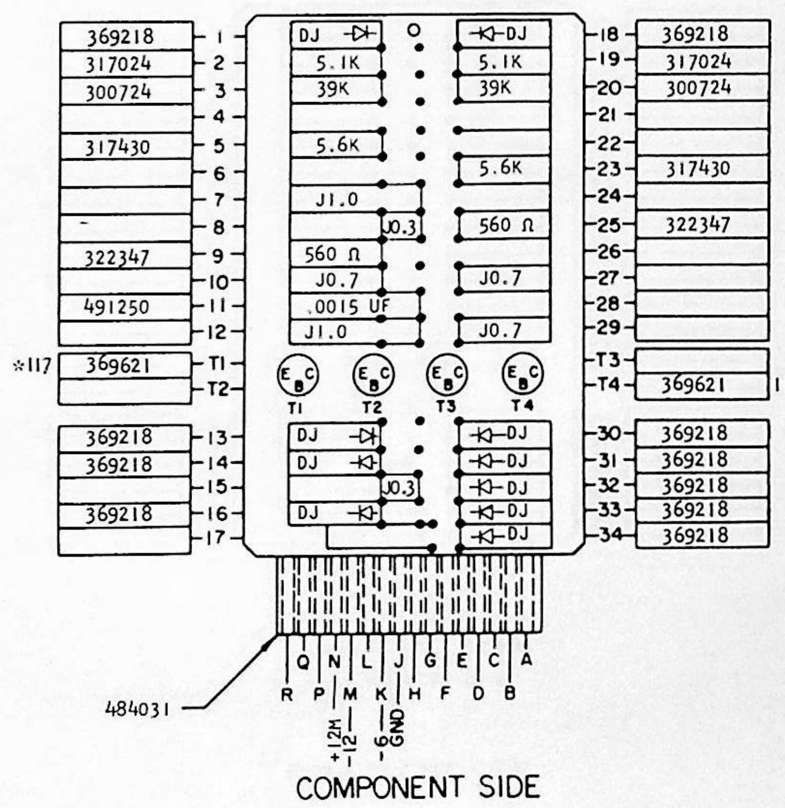
SDTDL-5-WAY LOGIC BLOCK LOW SPEED WITH LOADS





SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
A,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C,L	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E,R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 5-WAY LOGIC BLOCK LOW SPEED WITH LOADS			-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729917

C

STANDARDS CODE

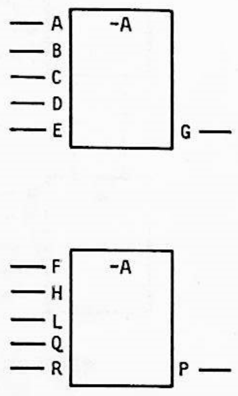
729918

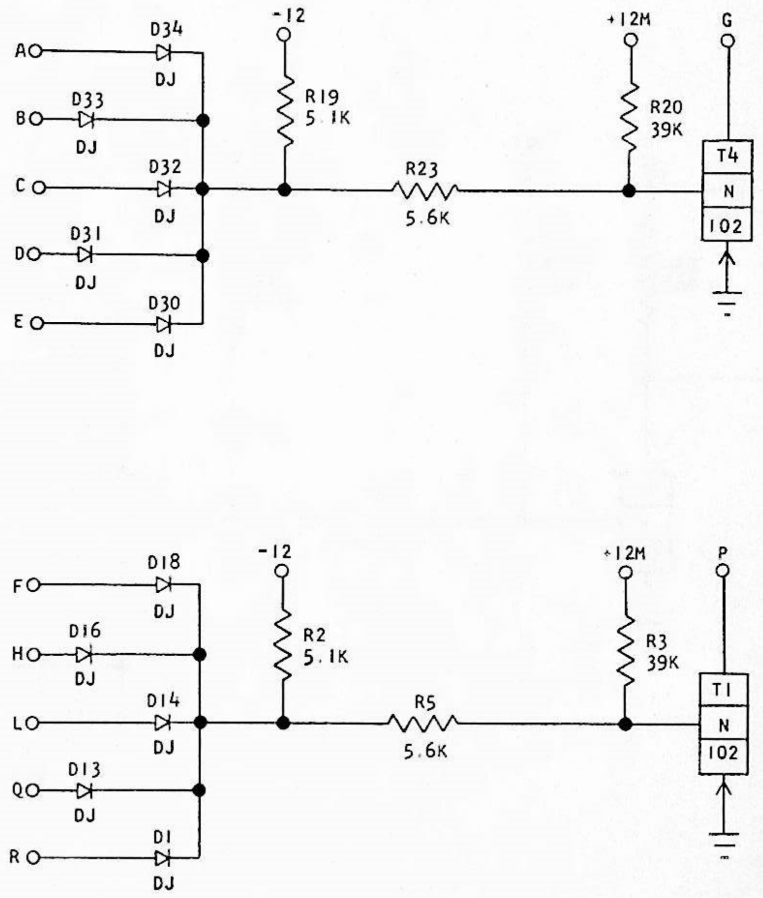
CARD CODE	729918
D G Y -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370375

SDTDL 5 WAY LOGIC BLOCK LOW SPEED WITHOUT LOAD

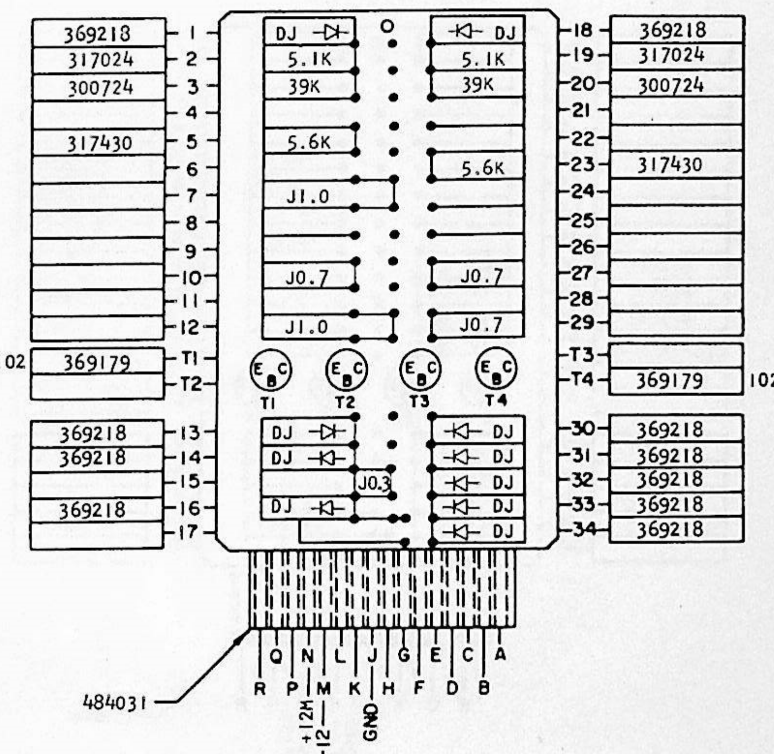




SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
B,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
C,L	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
D,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
E,R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
G,P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



COMPONENT SIDE

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				
NAME	CARD ASM TSTR-SDTDL 5-WAY			
	LOGIC BLOCK LOW SPEED WO/LOAD			
DESIGN			MODEL	SMS
DETAIL	RQ	3-1-62	SCALE	NONE
CHECK	WH	3-1-62	DRAW	LIG 3-17-62
APPRO			CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
-62	115599					

729918

C

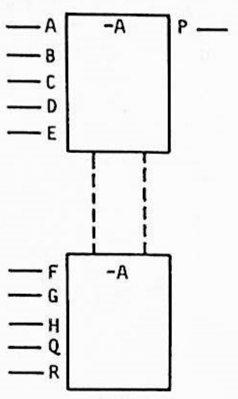
STANDARDS CODE
729919

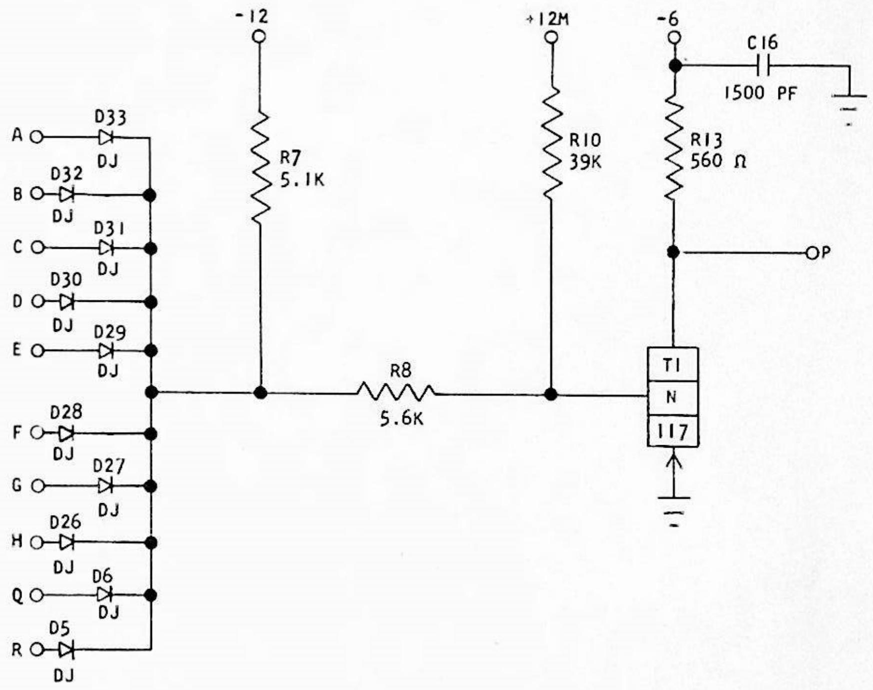
CARD CODE	729919
D G Z -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370373

SDTDL 10 WAY LOGIC BLOCK LOW SPEED WITH LOAD





DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

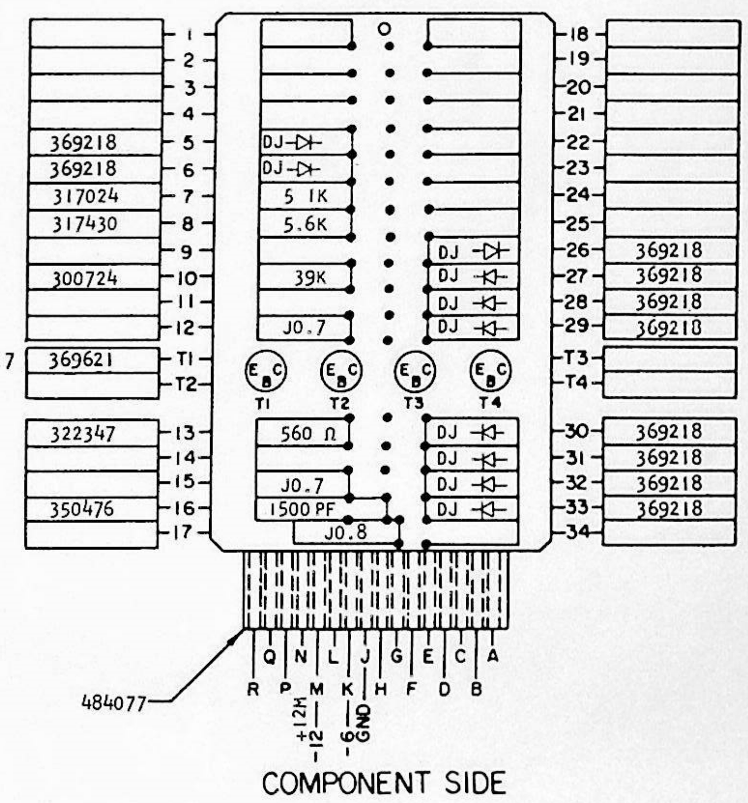
	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL 10 WAY LOGIC BLOCK LOW SPEED WITH LOAD				4 - -62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729919

C

STANDARDS CODE

729920

CARD CODE	729920
D H A -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370374

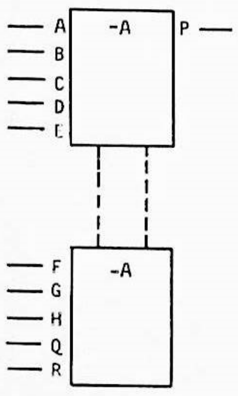
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

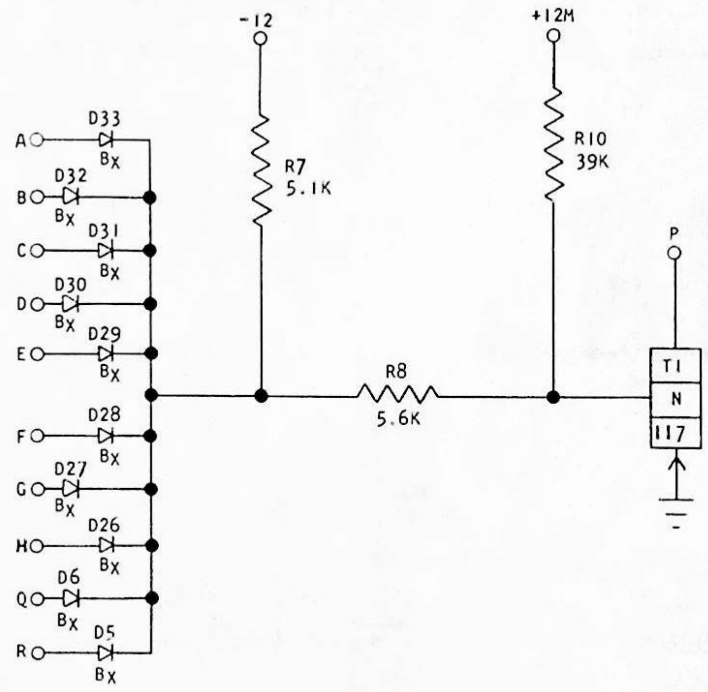
	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

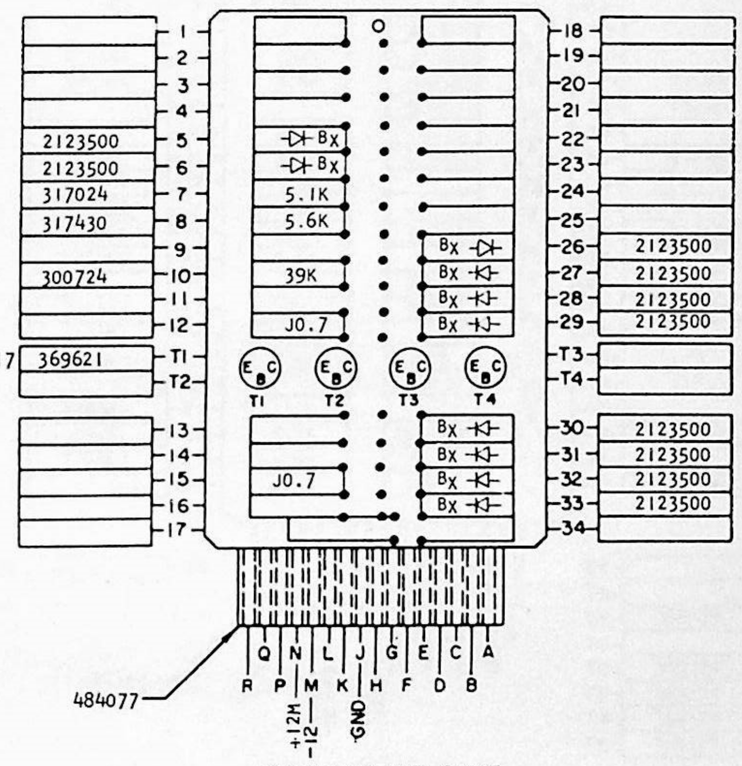


SDTDL 10-WAY LOGIC BLOCK LOW SPEED WITHOUT LOADS



SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP.
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN.
3. COLLECTOR MUST BE LOADED.
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-SDTDL 10-WAY				-62	115599					729920
LOGIC BLOCK LOW SPEED WO/LOADS										
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

C

72992I

STANDARDS CODE

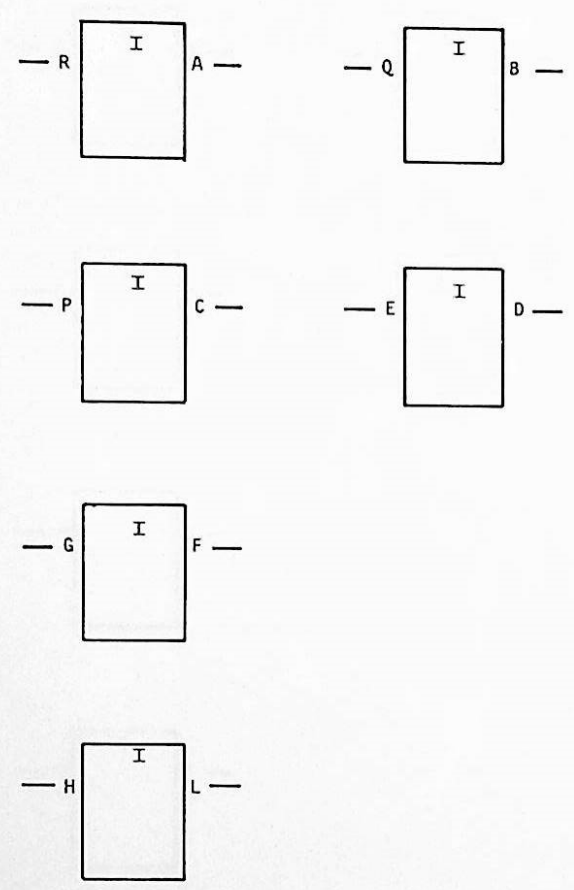
CARD CODE 72992I

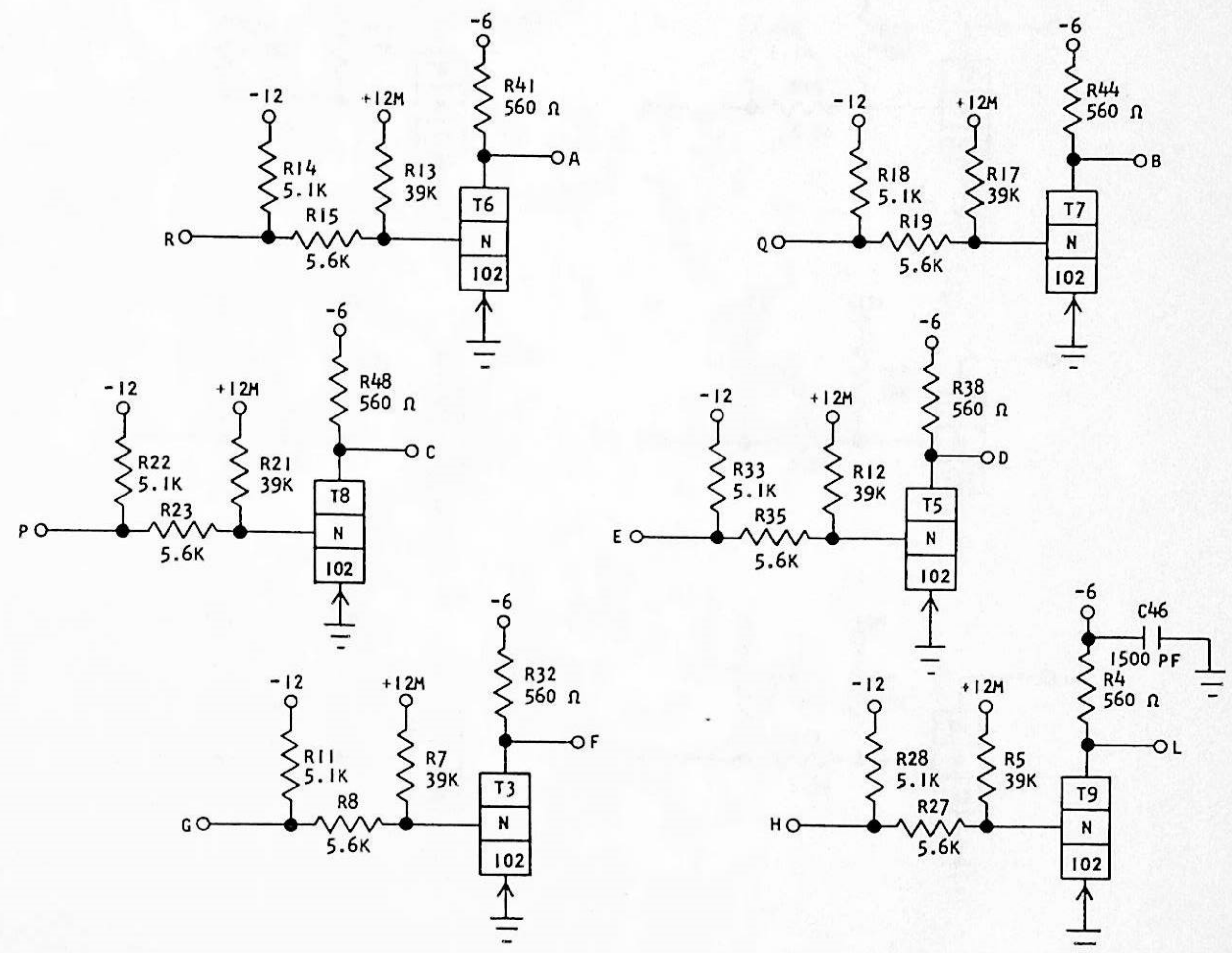
D H B -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370348

SDTDL INVERTER LOW SPEED WITH LOAD





SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
R,Q,P, E,G,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
A,B,C, D,F,H	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

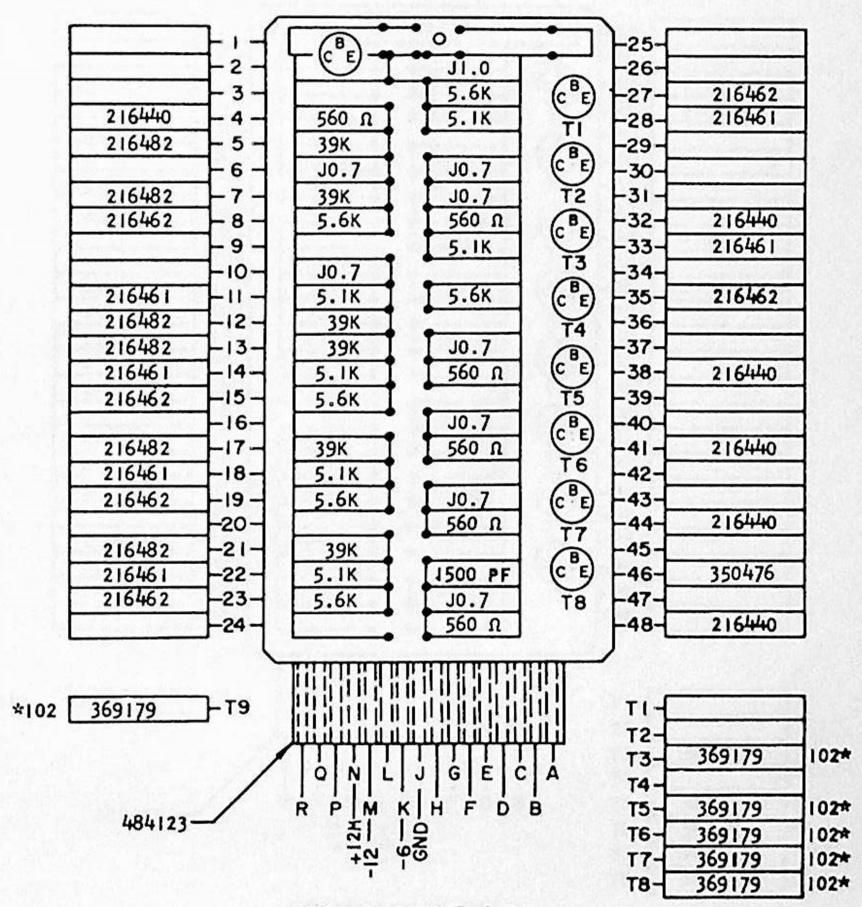
DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESOSTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR- SDTDL				-62	115599					
INVERTER LOW SPEED WITH LOAD										
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

72992I

C

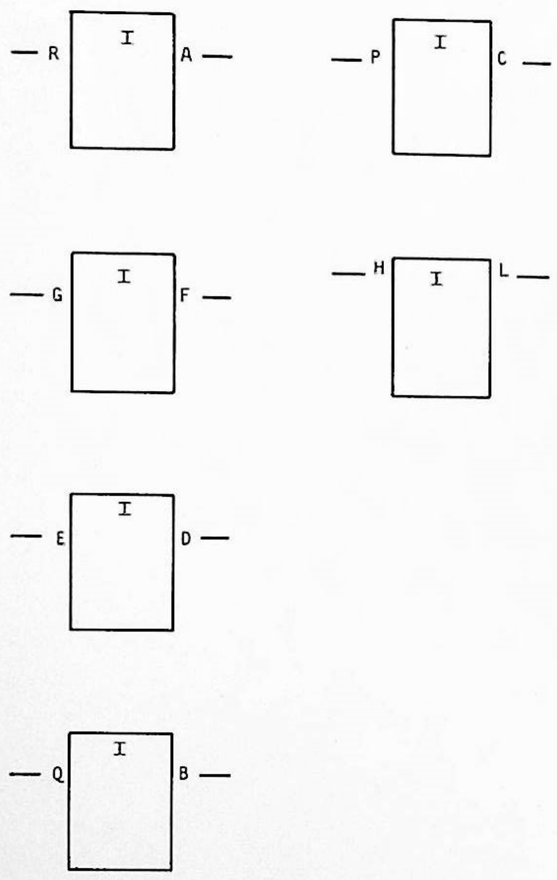
STANDARDS CODE

729922

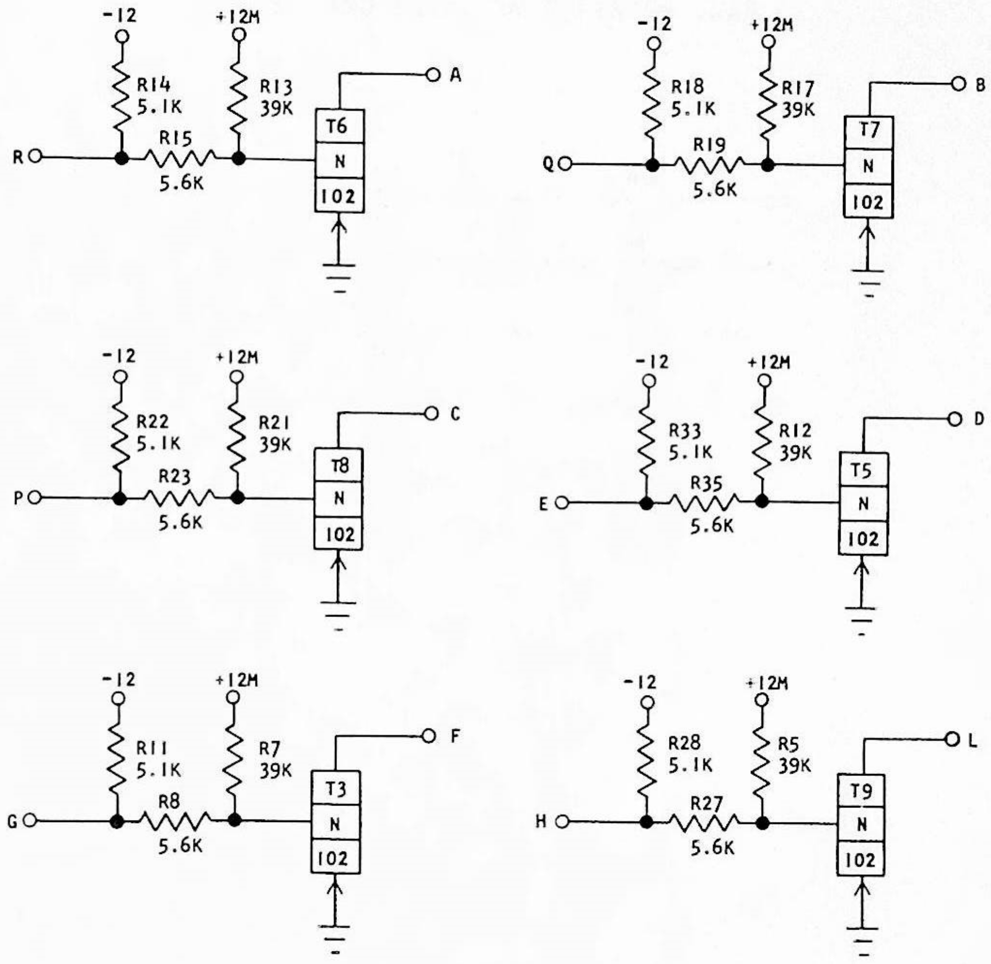
CARD CODE	729922
D H C -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370372

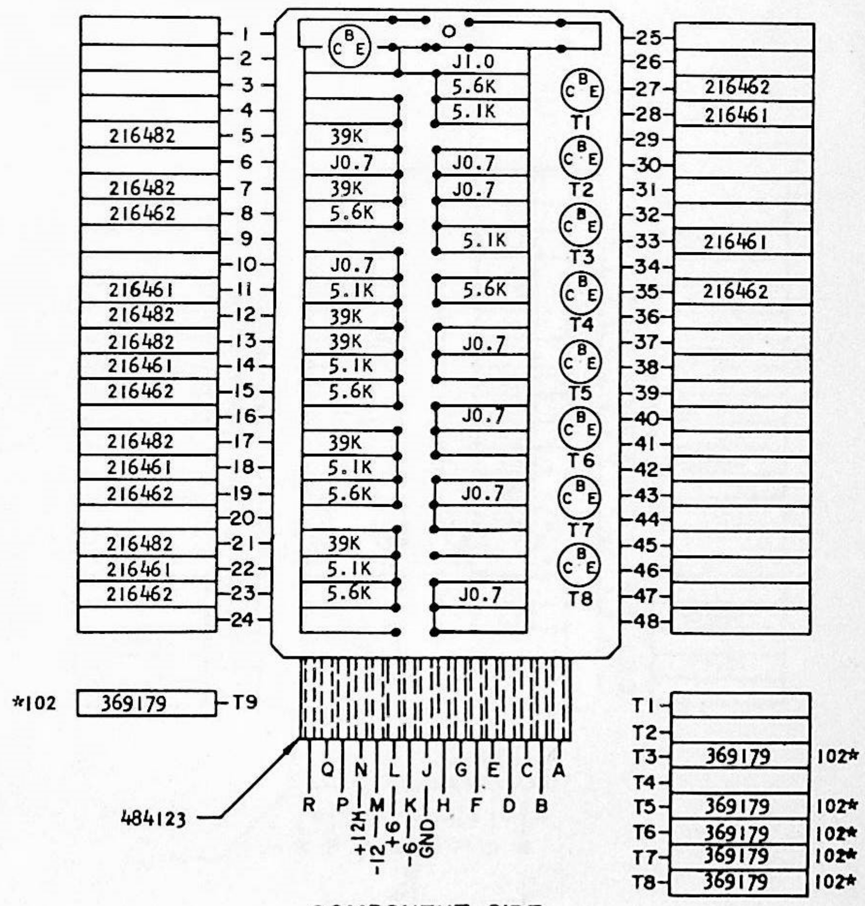


SDTDL INVERTER LOW SPEED W/O LOAD



SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. ALL COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
R,Q,P, E,G,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
A,B,C, D,F,L	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- SDTDL					-62	115599					
INVERTER LOW SPEED W/O LOAD												
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729922

C

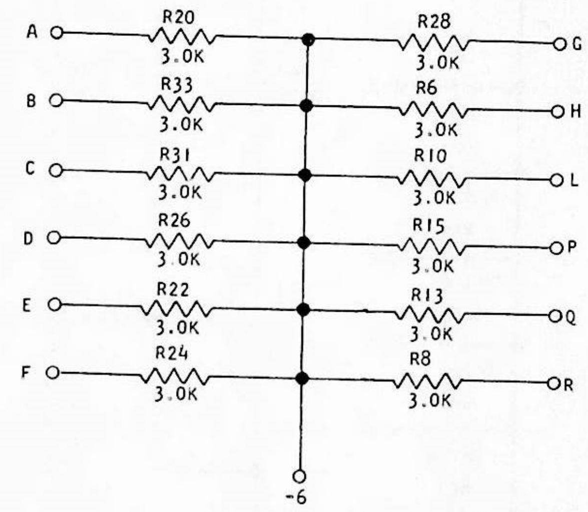
STANDARDS CODE
729923

CARD CODE	729923
DHD -	

REFERENCE DRAWING

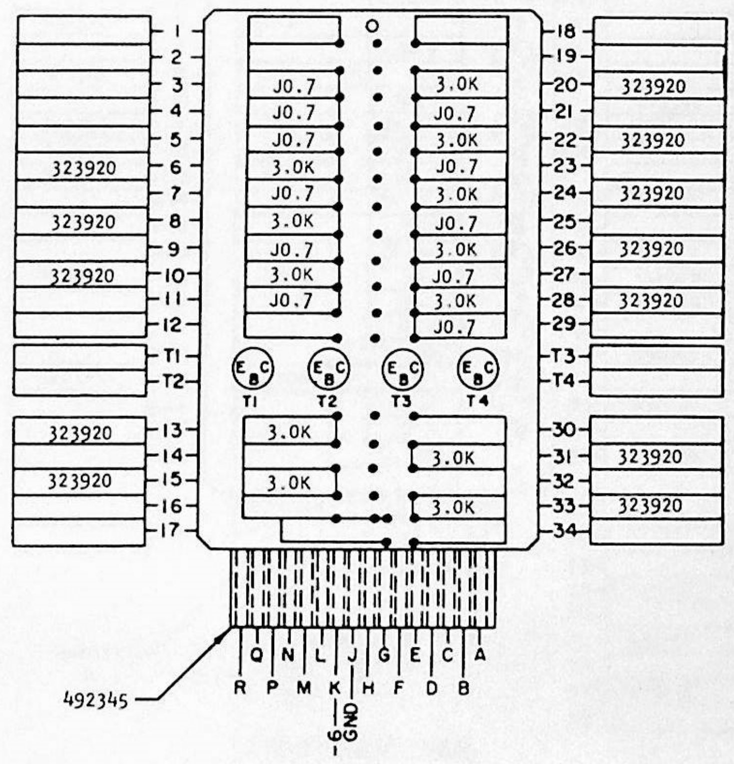
SEE PRODUCTION DRAWING 370371

SDTDL AND SDTRL 3K RESISTOR LOAD



APPLICATION

1. FOR COLLECTOR LOADING OF SDTDL AND SDTRL CARDS



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.

NAME	CARD ASM TSTR-SDTDL AND SDTRL 3K RESISTOR CARD		
DESIGN		MODEL	SMS
DETAIL	RQ 3-1-62	SCALE	NONE
CHECK	WH 3-1-62	DRAW	LIG 3-17-62
APPRO		CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-24-62	115599					

729923

C

STANDARDS CODE

729924

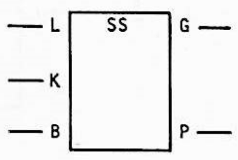
CARD CODE	729924
D H E -	

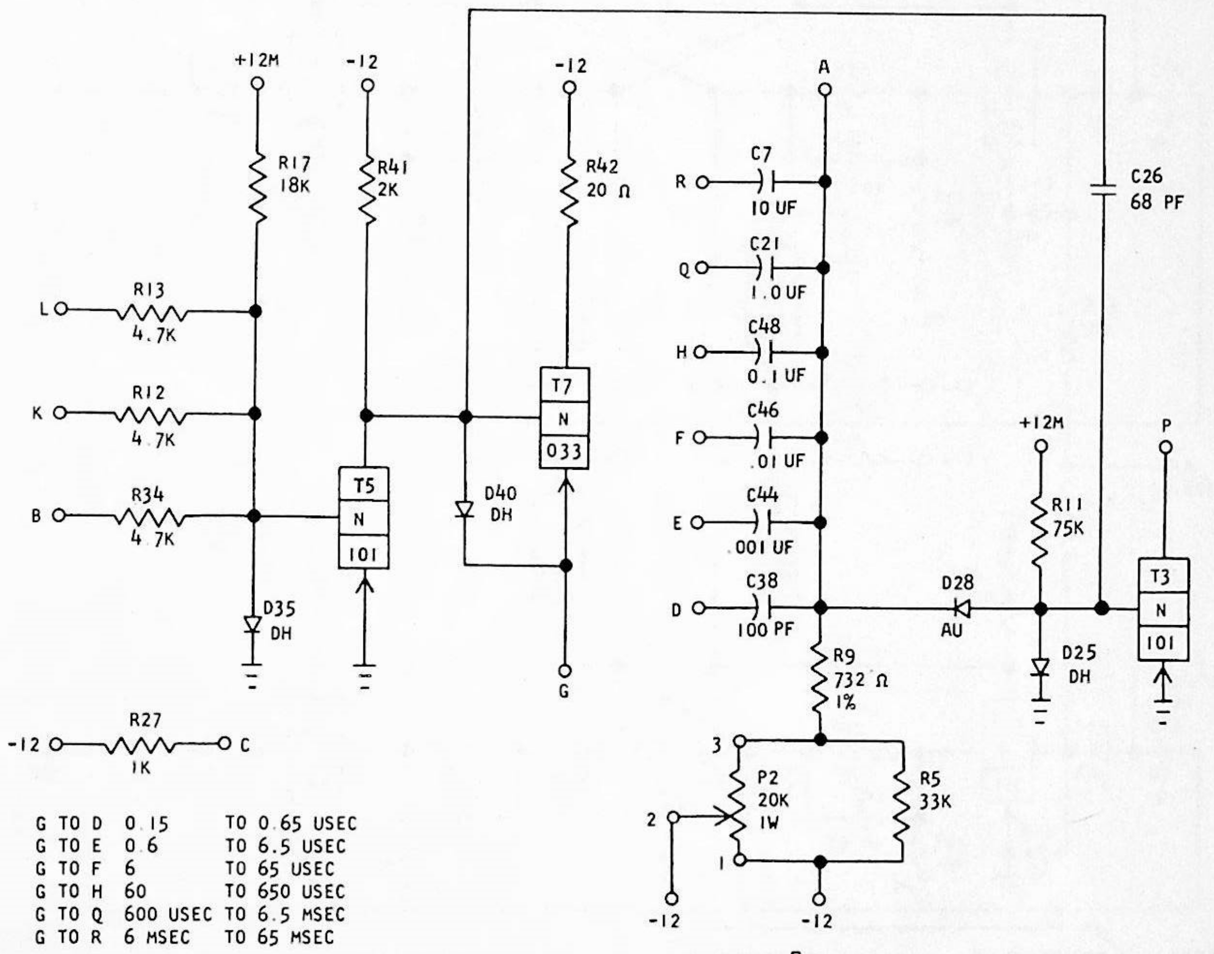
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370262

SDTRL - SINGLE SHOT

0.15 USEC TO 65 MSEC

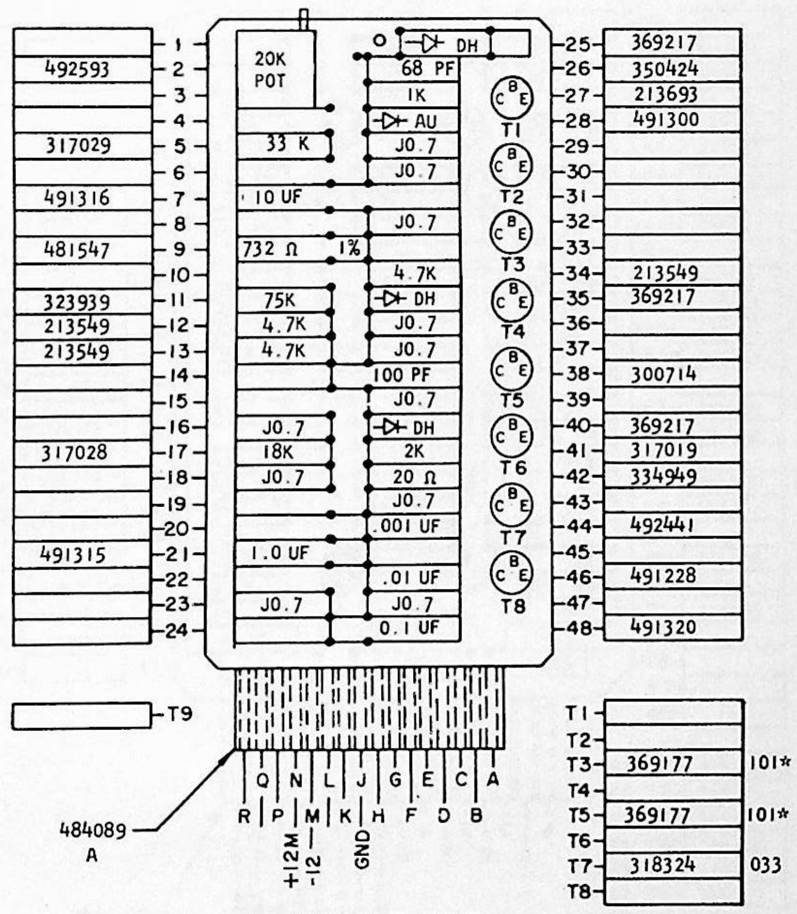




G TO D 0.15 TO 0.65 USEC
G TO E 0.6 TO 6.5 USEC
G TO F 6 TO 65 USEC
G TO H 60 TO 650 USEC
G TO Q 600 USEC TO 6.5 MSEC
G TO R 6 MSEC TO 65 MSEC

SEQUENCE OF OPERATION

1. PIN P TIED TO C FOR COLLECTOR LOAD, AND TO ANY INPUT IF INPUT PULSE IS NARROWER THAN REQUIRED OUTPUT PULSE. G IS TIED TO REQUIRED TIME CONSTANT INPUT
2. ALL INPUTS UP T5 OFF, T3 ON, OUTPUT UP
3. DOWN INPUT T5 ON, T3 OFF, OUTPUT DOWN
4. T3 TURNED BACK ON AT END OF TIME CONSTANT



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
L	Y	INPUT		UP	-0.6	-0.1
				DOWN	-6.87	-12.5
K	Y	INPUT		UP	-0.6	-0.1
				DOWN	-6.87	-12.5
B	Y	INPUT		UP	-0.6	-0.1
				DOWN	-6.87	-12.5
P	Y	OUTPUT		UP	-0.6	-0.1
				DOWN	-6.87	-10.5
T3 BASE		SWITCH LEVEL				

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL- SINGLE SHOT			6-29-62	115599					729924
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

C

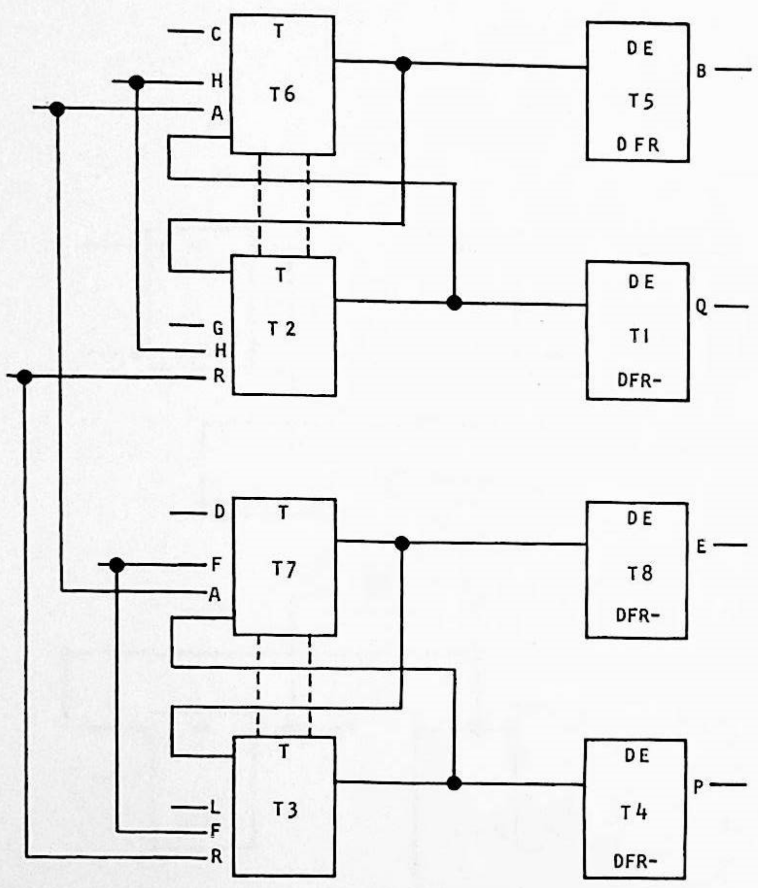
STANDARDS CODE

729925

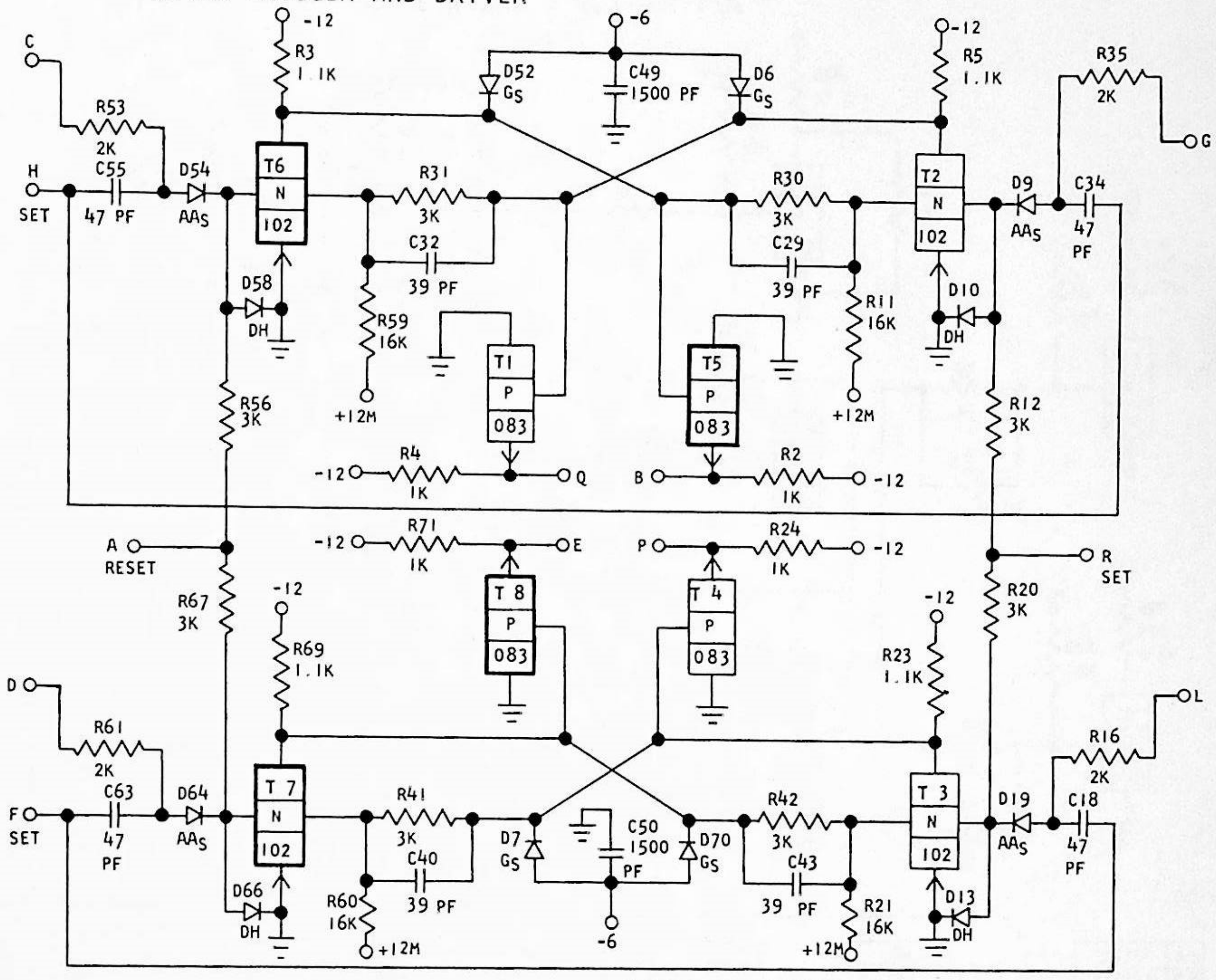
CARD CODE	729925
D H F -	

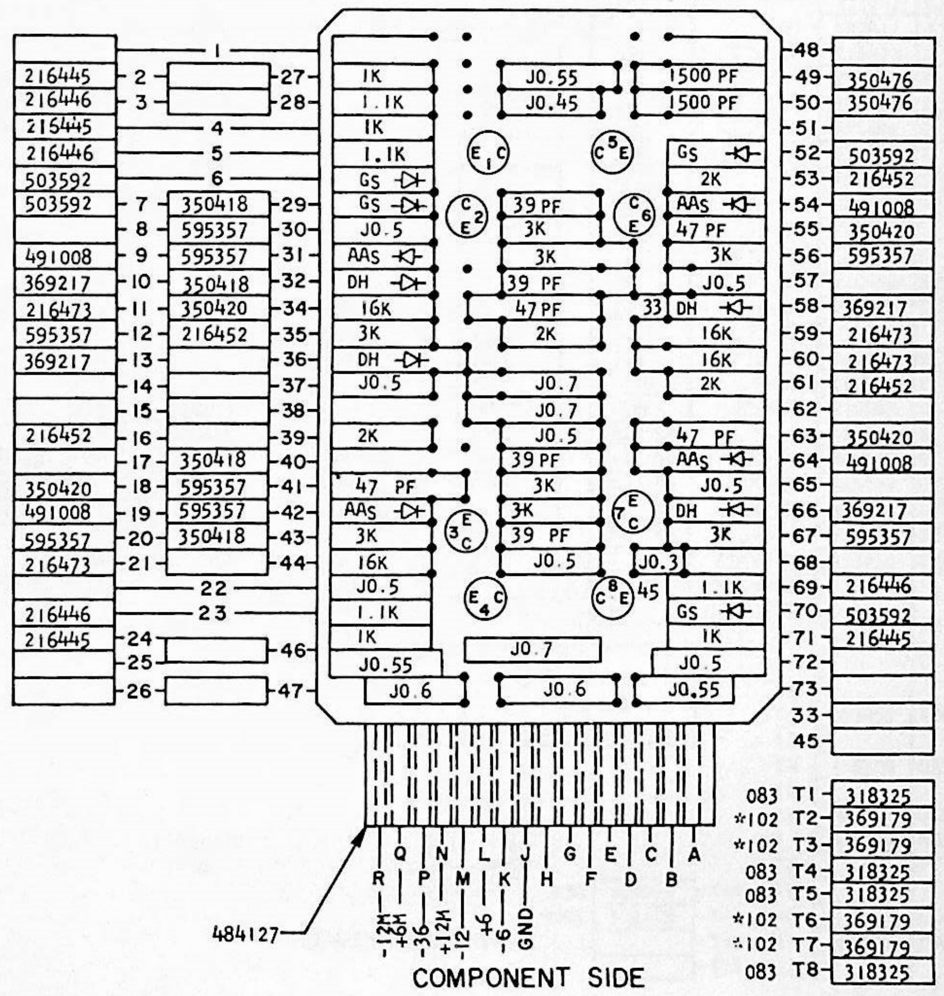
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370350



SDTDL TRIGGER AND DRIVER





SEQUENCE OF OPERATION

THE RESET INPUT RESPONDS TO A NEGATIVE VOLTAGE LEVEL. RESETING TURNS T6, T7, T5 AND T8 ON AND THE OTHER TRANSISTORS WILL BE IN THE OPPOSITE STATE. THE GATES ARE CONDITIONED BY A POSITIVE VOLTAGE LEVEL AND THE AC SET IS RESPONSIVE TO A POSITIVE VOLTAGE LEVEL. THUS, TO SET THE TRIGGER MEANS TO TURN OFF THE TRANSISTOR WHOSE GATE AND SET ARE BOTH POSITIVE. THE DC SET RESPONDS TO A NEGATIVE VOLTAGE LEVEL. THUS WHEN THE TRIGGER IS DC SET, T2, T3, T1 AND T4 WILL BE ON.

DELAY - NSEC

	TON		TRISE		TOFF		TFALL	
	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
BINARY OPERATION:	123	36	63	16	240	115	200	95
GATED:	135	40	48	16	205	82	160	61

NOTE: TON IS DEFINED AS THE DELAY FROM THE TIME AN AC INPUT SIGNAL ARRIVES UNTIL THE "OFF" TRANSISTOR HAS TURNED ON COMPLETELY. THIS IS MEASURED FROM THE TIME THE AC INPUT HAS SHIFTED 10%

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
C,D	Y	GATE		UP	-.65	-.1
				DOWN	-5.81	-7.64
H,F	Y	AC SET		UP	-.65	-.1
				DOWN	-5.81	-7.64
R	Y	DC SET		UP	-.65	-.1
				DOWN	-5.81	-7.64
A	Y	RESET		UP	-.65	-.1
				DOWN	-5.81	-7.64
Q,P	Y	OUTPUT		UP	-1.1	-.22
				DOWN	-5.83	-7.3
B,E	Y	OUTPUT		UP	-1.1	-.22
				DOWN	-5.83	-7.3
G,L	Y	GATE		UP	-.65	-.1
				DOWN	-5.81	-7.64

IN THE POSITIVE DIRECTION UNTIL THE "OFF" TRANSISTOR HAS SHIFTED 90% POSITIVE.

TOFF IS MEASURED FROM THE TIME AN AC INPUT HAS SHIFTED 10% POSITIVE UNTIL THE OUTPUT OF THE "ON" TRANSISTOR HAS SHIFTED 90% NEGATIVE.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					
NAME	CARD ASM TSTR-SDTDL				
	TRIGGER AND DRIVER				
DESIGN			MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE	
CHECK	WH	3-1-62	DRAW	LIG	3-17-62
APPRO			CHECK		

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
4 ?-62	115599					

729925

C

STANDARDS CODE

729926

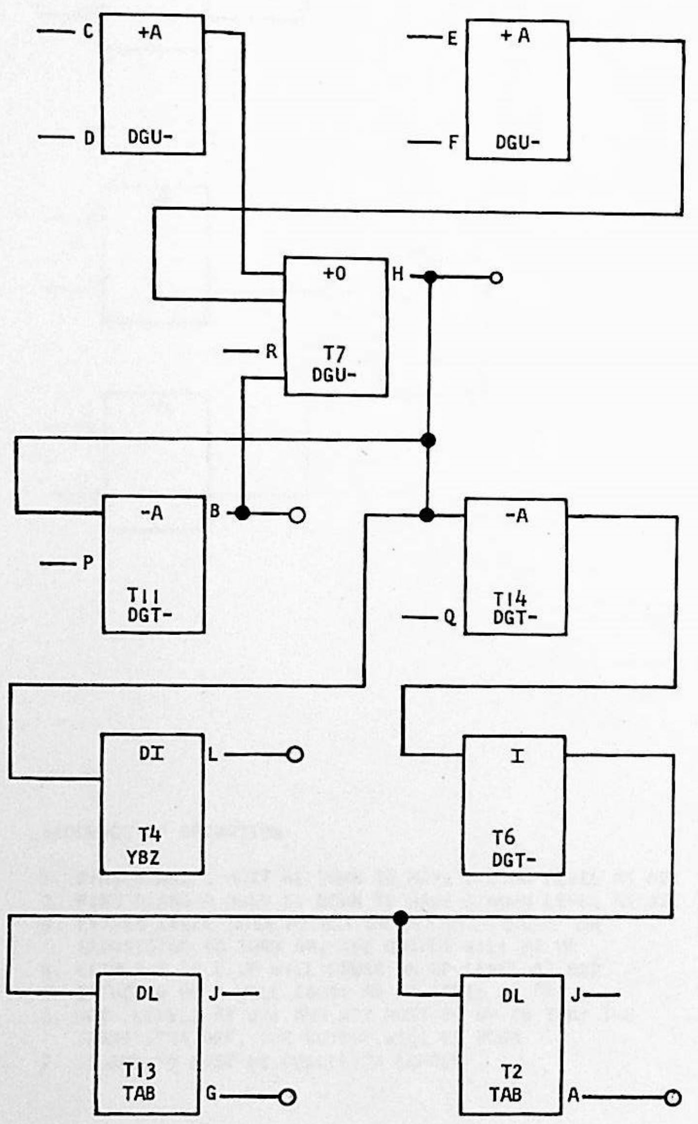
CARD CODE 729926

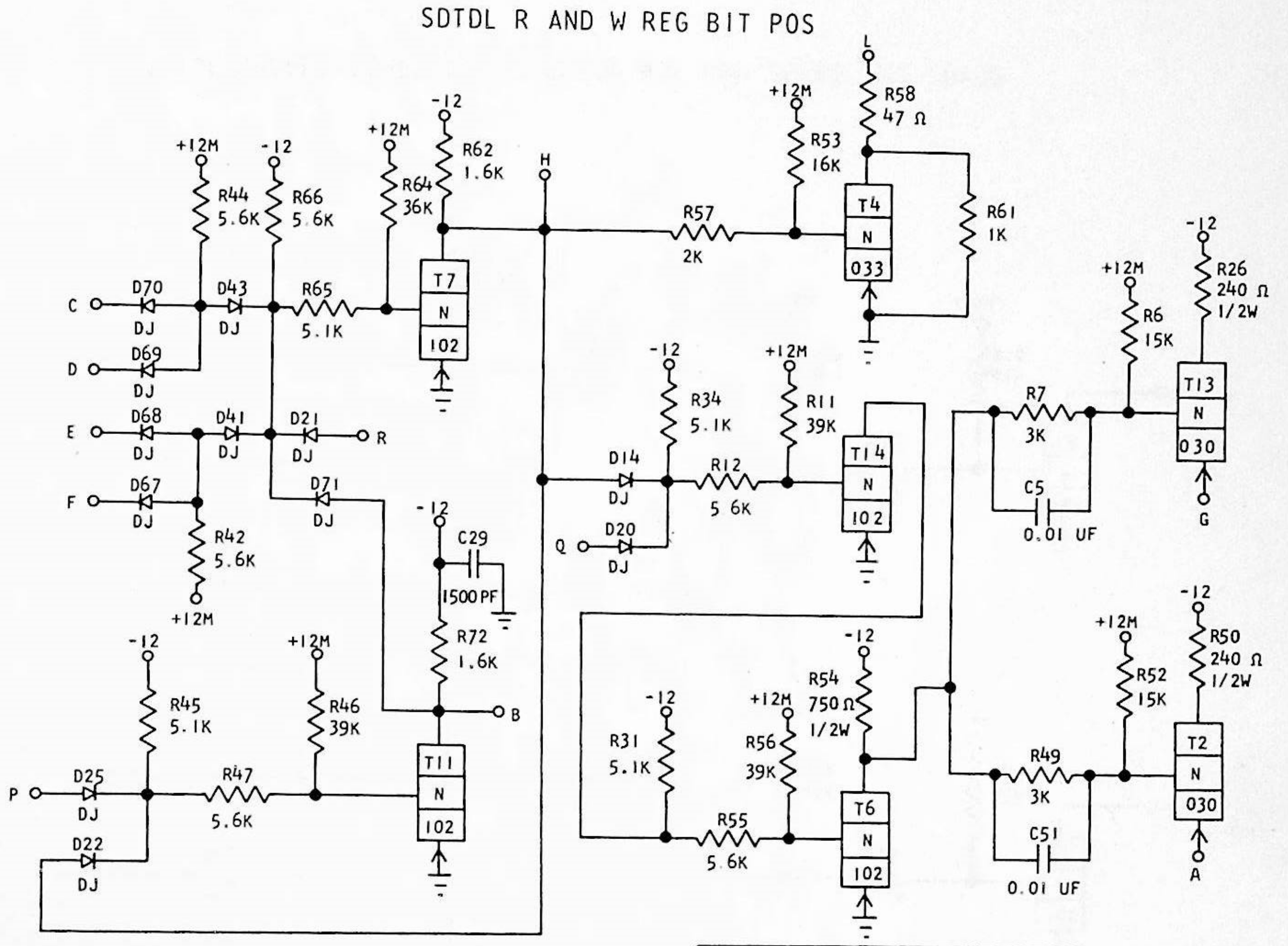
D H G -

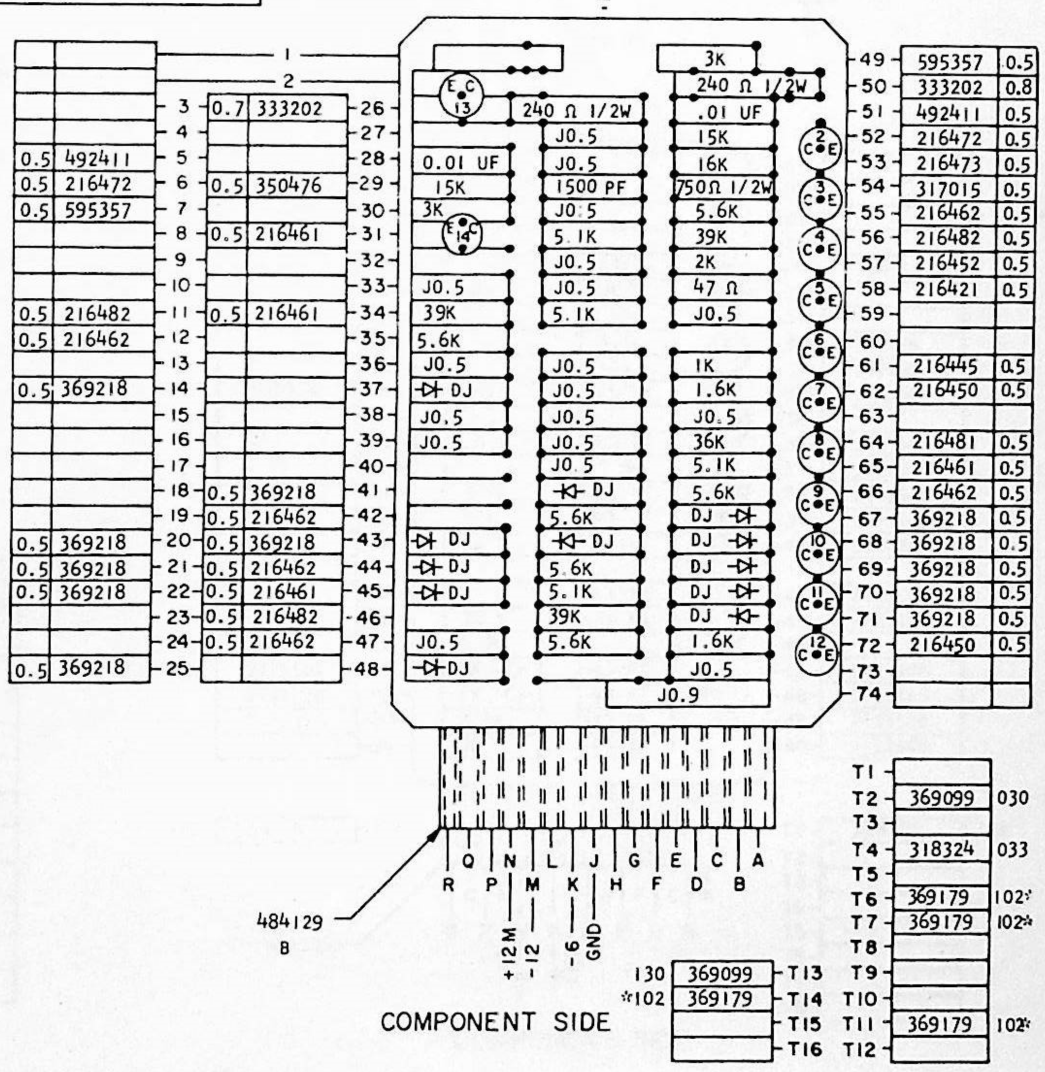
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370351

SDTDL R AND W REG BIT POS







SEQUENCE OF OPERATION

1. PINS CD OR EF OR R OR B IN UP LEVEL GIVES DOWN LEVEL AT PIN H. A DOWN LEVEL AT PIN H TURNS ON T4 GIVING UP LEVEL AT PIN L.
2. DOWN LEVELS ON PIN H AND Q GIVES UP LEVEL AT OUTPUT OF T14 WHICH TURNS T6 OFF AND T2 AND T13 ON GIVING VOLTAGE OUTPUT AT PINS A AND G (N LEVEL).
3. DOWN LEVEL AT PIN H WITH DOWN LEVEL AT PIN P RESULTS IN UP LEVEL AT PIN B
4. T7 AND T11 ACT AS A LATCH WITH GATE IN CONTROLS. THE LATCH BACK IS PERFORMED BY THE OUTPUT OF T11 BEING FED TO T7
5. T2 AND T13 ARE TRANSMISSION LINE DRIVERS CONVERTING S LEVEL INPUT TO A VOLTAGE SIGNAL FOR TRANSMISSION OVER A 93 OHM COAXIAL LINE
6. THE INPUTS ARE Y LINE LEVELS. FOR WAVEFORMS AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS
7. DELAY - NSEC

		MIN.	MAX.
PINS C, D, E, F, R TO PIN H:	TURN ON	80	258
	TURN OFF	100	465
PINS C, D, E, F, R TO PIN B:	TURN ON	120	458
	TURN OFF	175	465
PIN P TO PIN B:	TURN ON	75	100
	TURN OFF	40	200
PIN Q TO PIN G OR A:	TURN ON	125	340
	TURN OFF	115	310
PINS C, D, E, F, R TO PIN G OR A:	TURN ON	195	568
	TURN OFF	225	705

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR SDTDL R AND W REG BIT POS			4-2-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729926

C

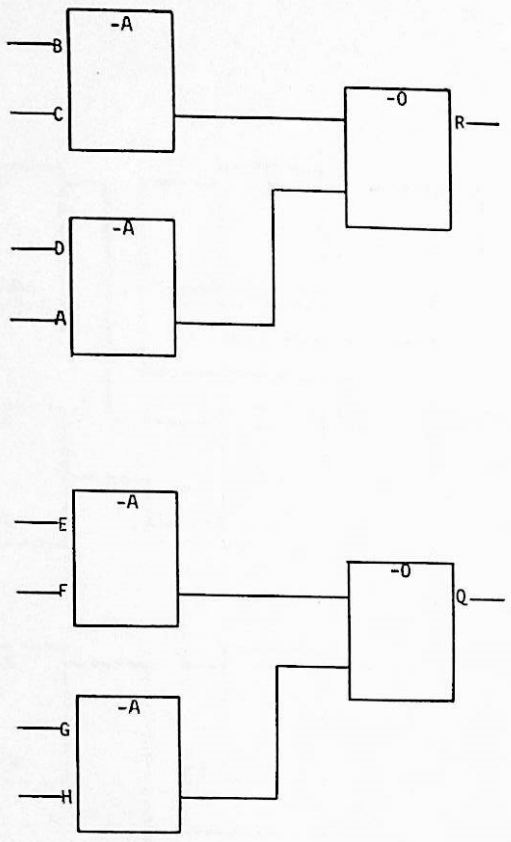
STANDARDS CODE

729927

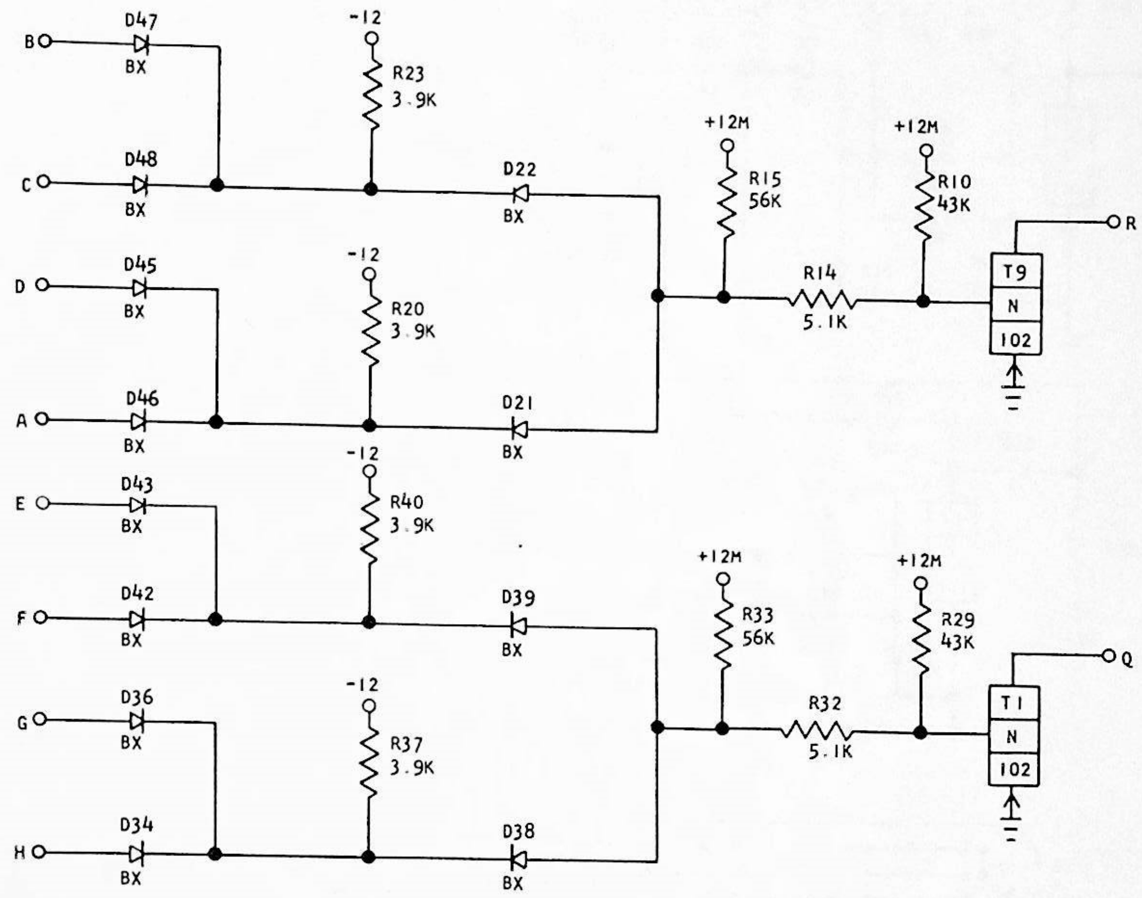
CARD CODE	729927
D H H -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370358

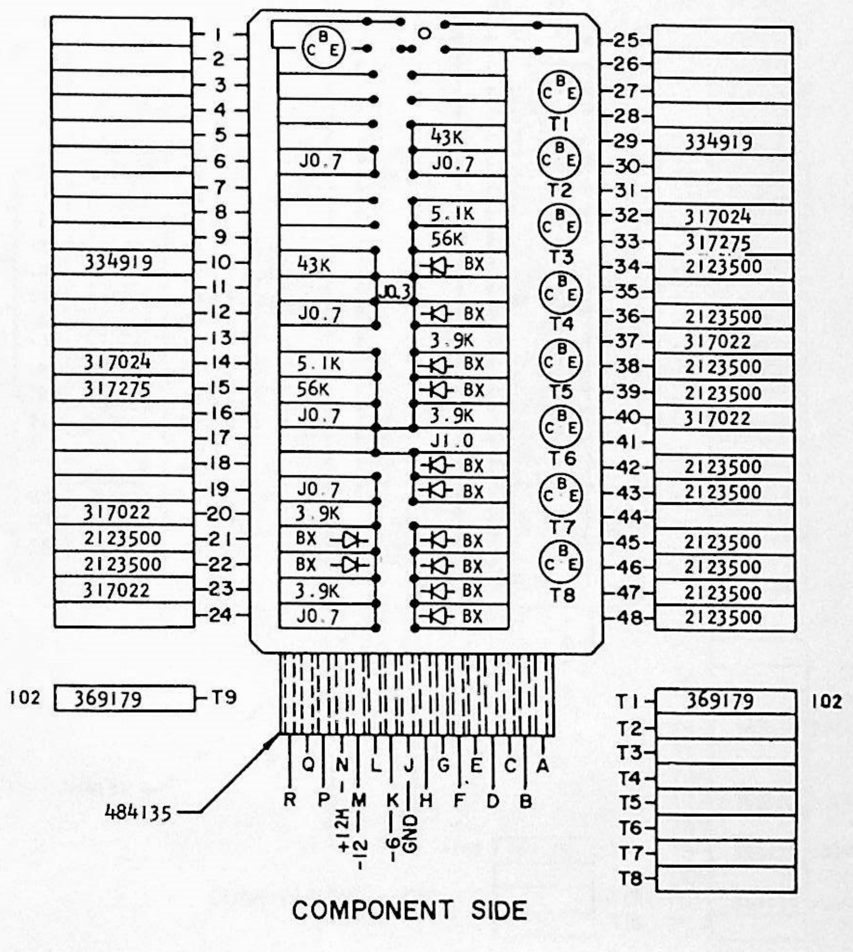


SDTDL DOUBLE LEVEL LOGIC BLOCK #2A LOW SPEED, WO LOADS



SEQUENCE OF OPERATION

1. PINS B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D22
2. PINS D AND A MUST BE DOWN TO HAVE A DOWN LEVEL AT D21
3. EITHER LEVEL DOWN AT D21 OR D22 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP
4. EITHER B OR C UP WILL CAUSE AN UP LEVEL AT D22
5. EITHER D OR A WILL CAUSE AN UP LEVEL AT D21
6. BOTH LEVELS AT D21 AND D22 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN
7. T1 AND T9 MUST BE COLLECTOR LOADED



PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B,C D,A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
R	Y	OUTPUTS		UP	-.65	.1
				DOWN	-5.81	-8.8
E,F G,H	Y	INPUTS		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	Y	OUTPUTS		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY - NSEC

	MIN.	MAX
TURN ON	70	240
TURN OFF	110	515

NOTE: MAXIMUM DELAY MAY INCREASE FOR A 6.2K COLLECTOR RESISTOR.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.			
NAME	CARD ASM TSTR-SDTDL-DOUBLE LEVEL LE #2A LOW SPEED, WO LOADS		
DESIGN		MODEL	SMS
DETAIL	RQ 3-1-62	SCALE	NONE
CHECK	WH 3-1-62	DRAW	LIG 3-17-62
APPRO		CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
-62	115599					

729927

C

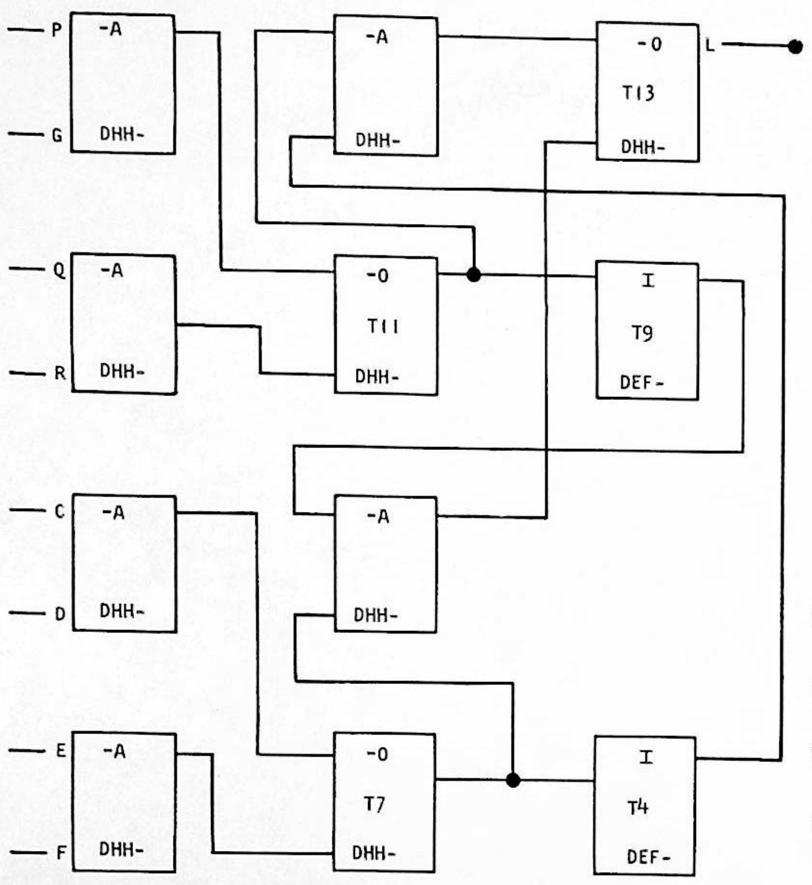
STANDARDS CODE

729928

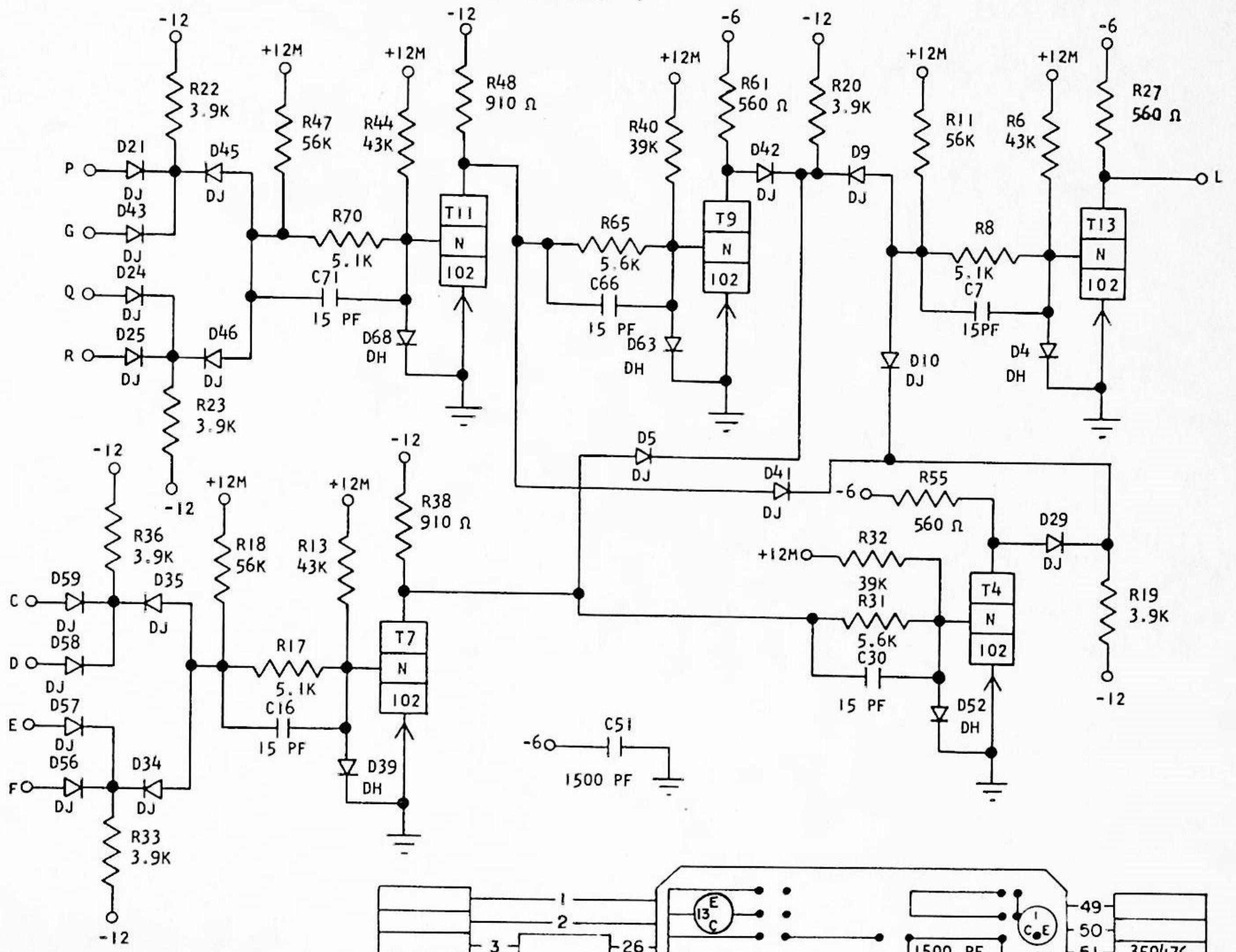
CARD CODE	729928
D H J -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370352



SDTDL MUP NUMBER 4



SEQUENCE OF OPERATION

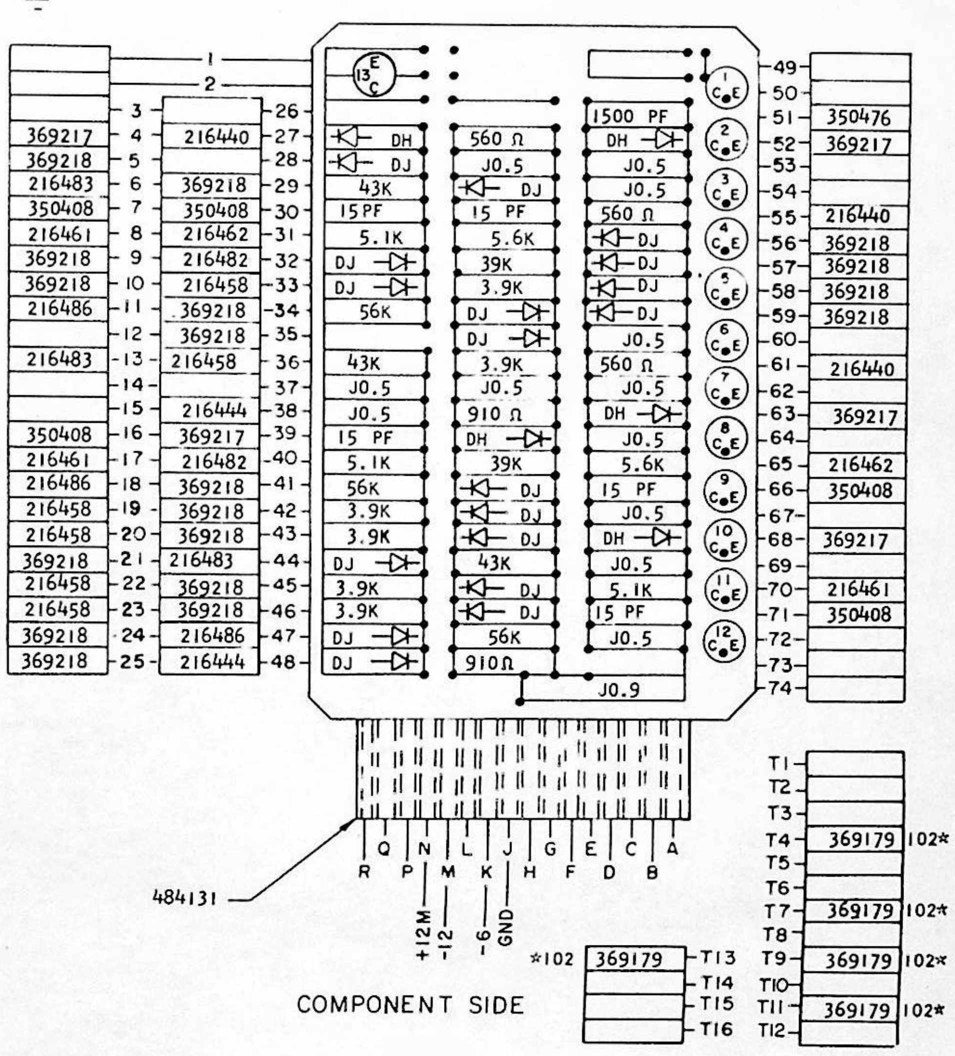
1. THE FIRST LEVEL OF DIODES OF BOTH T11 AND T7 PERFORM A NEGATIVE AND AND THE SECOND LEVEL OF DIODES A NEGATIVE OR FUNCTION. T9 AND T4 ARE HIGH SPEED INVERTERS THAT ACCEPT NEGATIVE INPUTS TO PERFORM A NEGATIVE AND INVERT FUNCTION. THESE TRANSISTORS ARE DRIVEN BY T11 AND T7 RESPECTIVELY. THE OUTPUTS OF T11, T7, T9 AND T4 ARE FED INTO T13 WHOSE FIRST LEVEL OF DIODES PERFORM A NEGATIVE AND AND WHOSE SECOND LEVEL PERFORM A NEGATIVE OR FUNCTION. THIS CIRCUIT IS USED TO CHECK FOR ODD PARITY OF A TAPE CHARACTER. T11 AND T7 ARE EXCLUSIVE OR'S THAT EACH DETERMINE IF TWO BITS ARE ODD OR EVEN PARITY AND THEN T13, ANOTHER EXCLUSIVE OR COMPARES THE OUTPUTS OF T11 AND T7 TO DETERMINE IF ALL FOUR BITS ARE ODD OR EVEN PARITY.

2. THE CARD CODES SHOWN IN THE BLOCKS REFER TO INDIVIDUAL CARDS SIMILAR TO THAT PORTION OF CIRCUITRY.

3. DELAY - NSEC

INPUTS TO OUTPUT:	MIN.	MAX.
TURN ON	32	263
TURN OFF	27	213

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
P,R, C,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,Q, D,E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
L	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.			
NAME	CARD ASM TSTR - SDTDL MUP NUMBER 4		
DESIGN		MODEL	SMS
DETAIL	RQ 3-1-62	SCALE	NONE
CHECK	WH 3-1-62	DRAW	LIG 3-17-62
APPRO		CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
4-?-62	115599					

729928

C

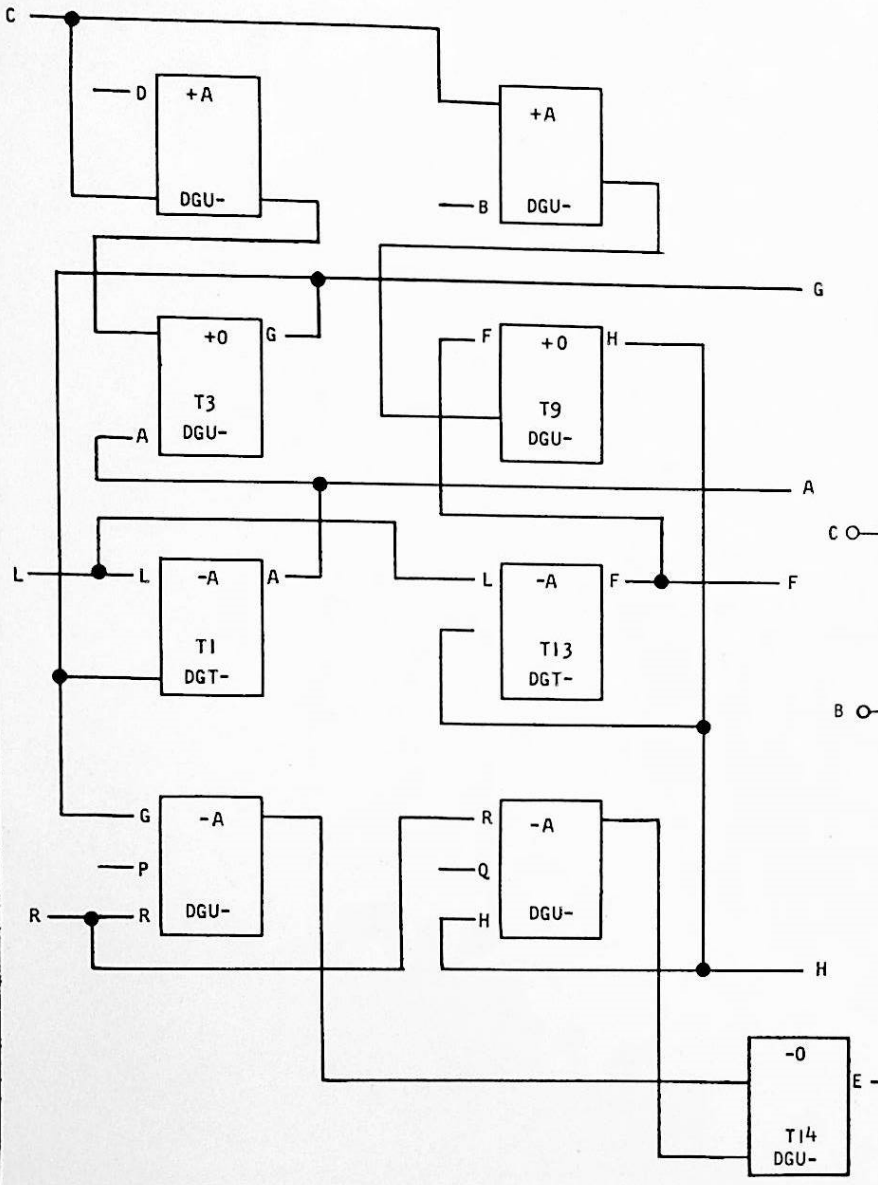
STANDARDS CODE

729929

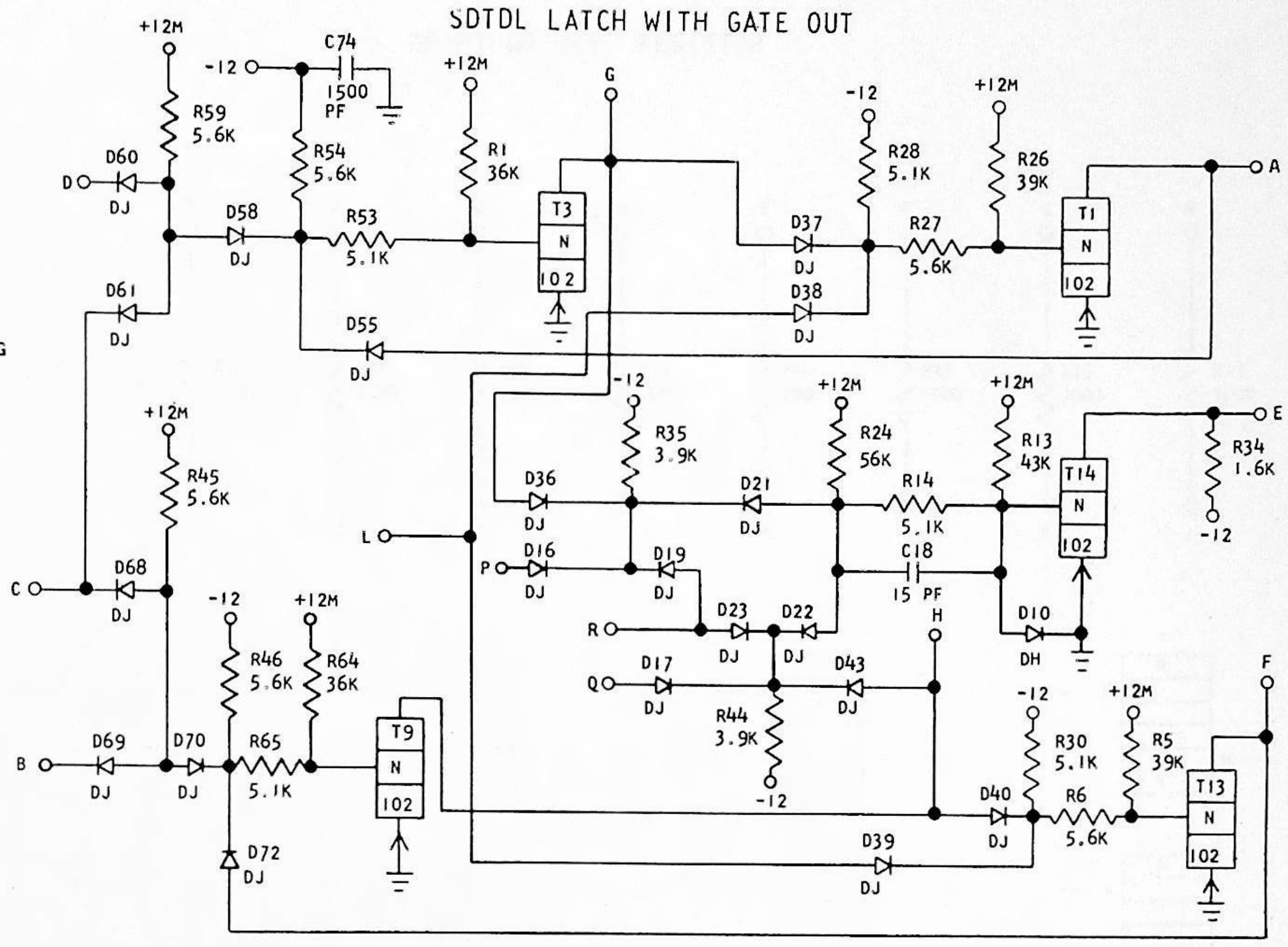
CARD CODE	729929
D H K -	

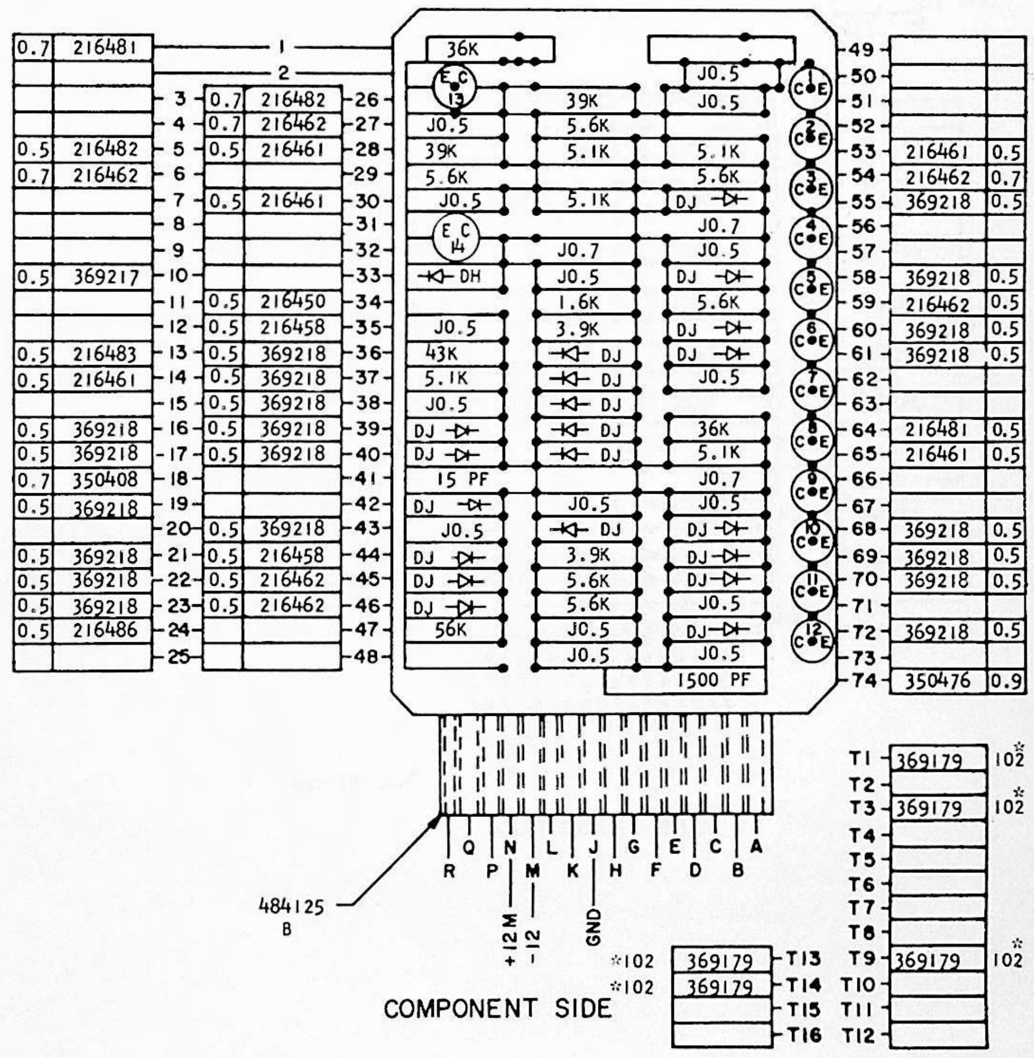
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370349



SDTDL LATCH WITH GATE OUT





SEQUENCE OF OPERATION

1. FIRST SET OF DIODES TO T3 AND T9 PERFORM A POSITIVE AND FUNCTION AND THE SECOND SET A NEGATIVE AND.
2. LATCH CONFIGURATION IS PERFORMED BY COUPLING THE OUTPUT OF T1 BACK TO THE NEGATIVE AND OF T3 AND BY T13 TO T9.
3. THE INPUTS TO T14 PERFORM TWO LOGICAL FUNCTIONS. FIRST SET PERFORM A NEGATIVE AND AND THE SECOND A NEGATIVE OR.
4. THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.
5. T3, T9, T1 AND T13 COLLECTORS MUST BE LOADED.
6. INPUTS AND OUTPUTS ARE ALL Y LINE LEVELS. FOR WAVE FORMS AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS.
7. THIS CIRCUIT PERFORMS A LATCH OPERATION WITH A GATE OUT.
8. DELAY - NSEC

		MIN	MAX
PIN C, D OR B TO PINS A & F:	TURN ON	120	458
	TURN OFF	175	565
PIN C, D OR B TO PINS G & H:	TURN ON	80	258
	TURN OFF	100	465
PIN C, D OR B TO PIN E:	TURN ON	95	383
	TURN OFF	107	523
PIN L TO PINS A & F:	TURN ON	75	100
	TURN OFF	40	200
PINS P, R AND Q TO PIN E:	TURN ON	7	58
	TURN OFF	15	125

NOTE: THESE DELAYS BASED ON A .68K LOAD RESISTOR AT PINS G AND H AND A .56K LOAD RESISTOR AT PINS A AND F. THEY CAN BE EXCEEDED WITH A LARGER COLLECTOR RESISTOR.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL LATCH				?-?-62	115599					729929
	WITH GATE OUT										
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

STANDARDS CODE

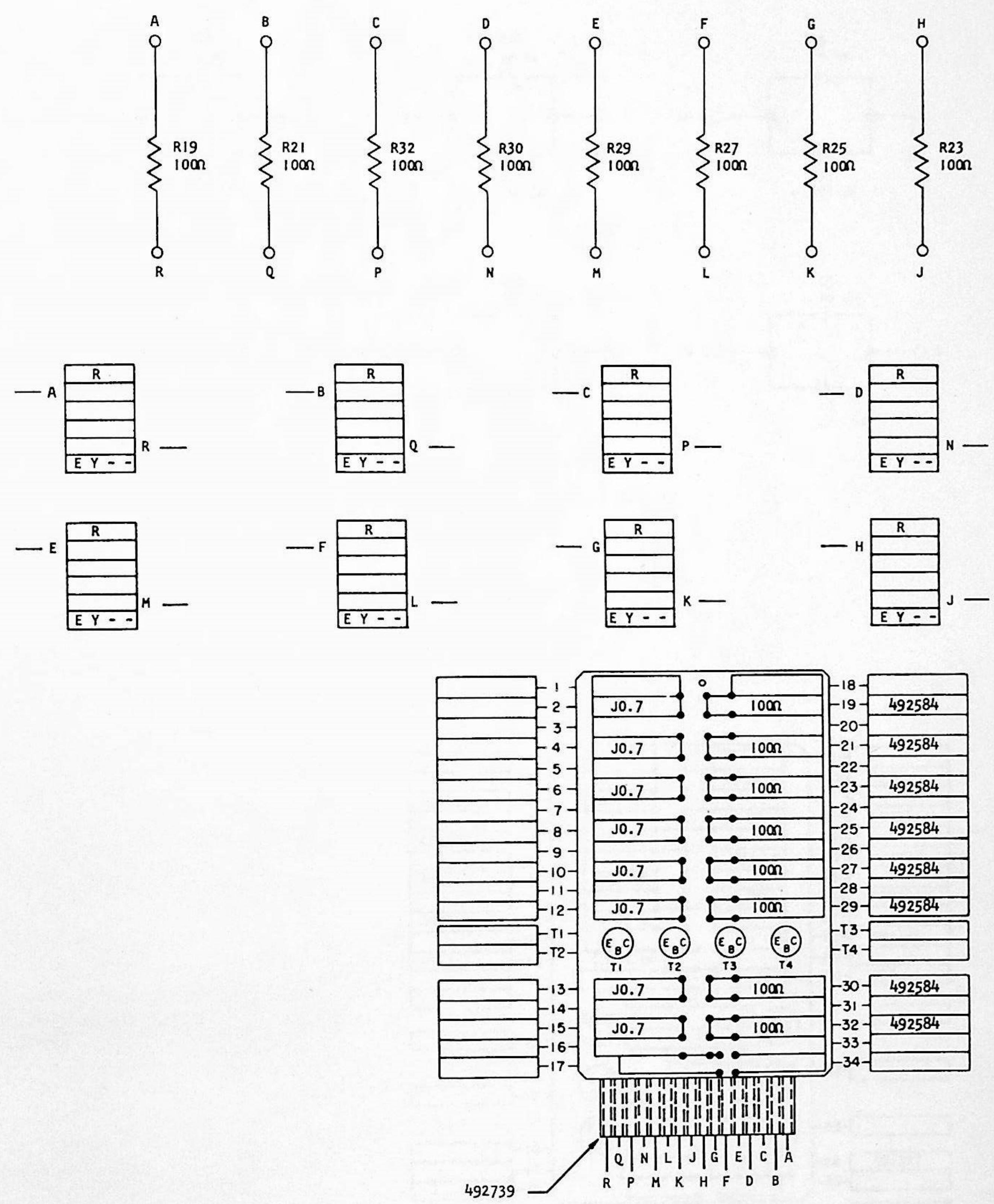
729930

CARD CODE	729930
EY --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371199

DRIFT-DRIVER, RESISTOR



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - DRIFT-DRIVER, RESISTOR				6-27-62	115599					
DESIGN		MODEL	SMS								
DETAIL	RQ 3-1-62	SCALE	NONE								
CHECK	WH 3-1-62	DRAW	LIG 3-17-62								
APPRO		CHECK									

729930

C

STANDARDS CODE

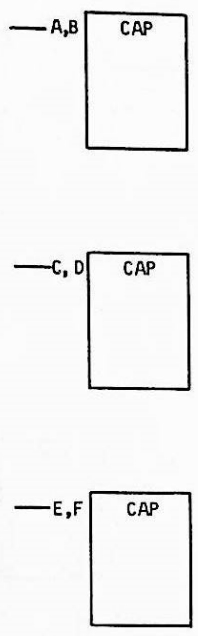
729931

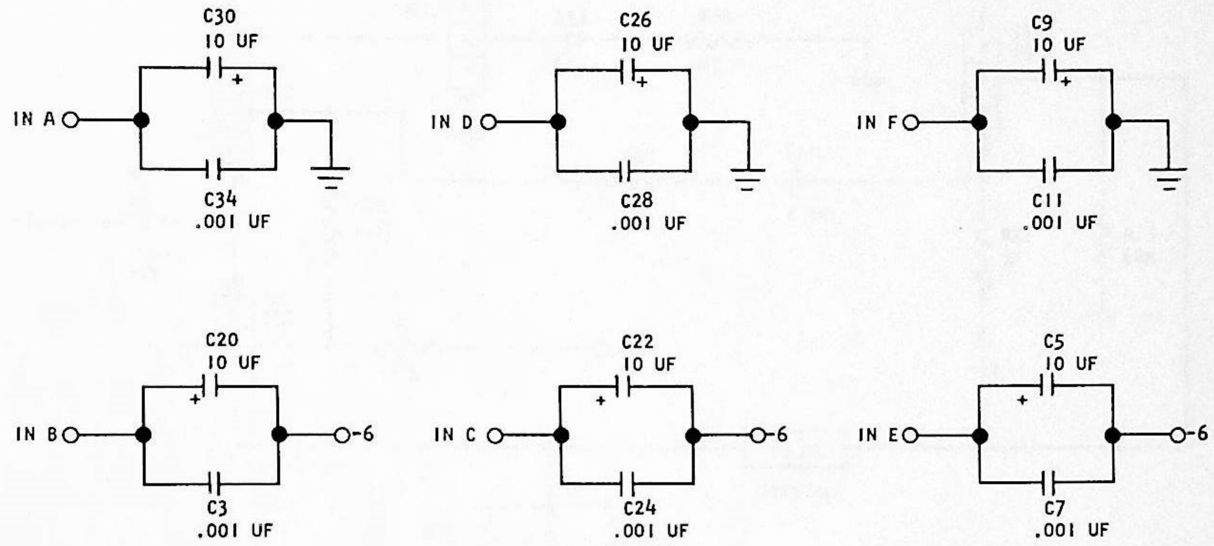
CARD CODE	729931
GK --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371533

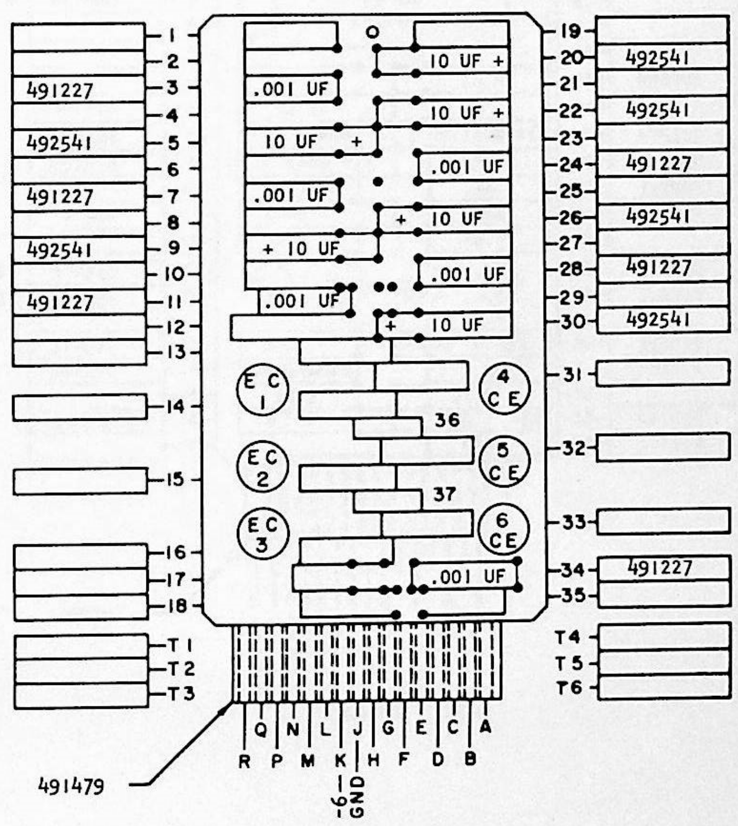
CABLE DE COUPLE CARD





SEQUENCE OF OPERATION

1. CARD DECOUPLES THE NEUTRAL WIRE OF A TWISTED PAIR OR THE SHIELD OF A COAXIAL CABLE



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CABLE					6-2?-62	115599					
	DE COUPLE CARD											
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729931

C

FORM 82-001

STANDARDS CODE

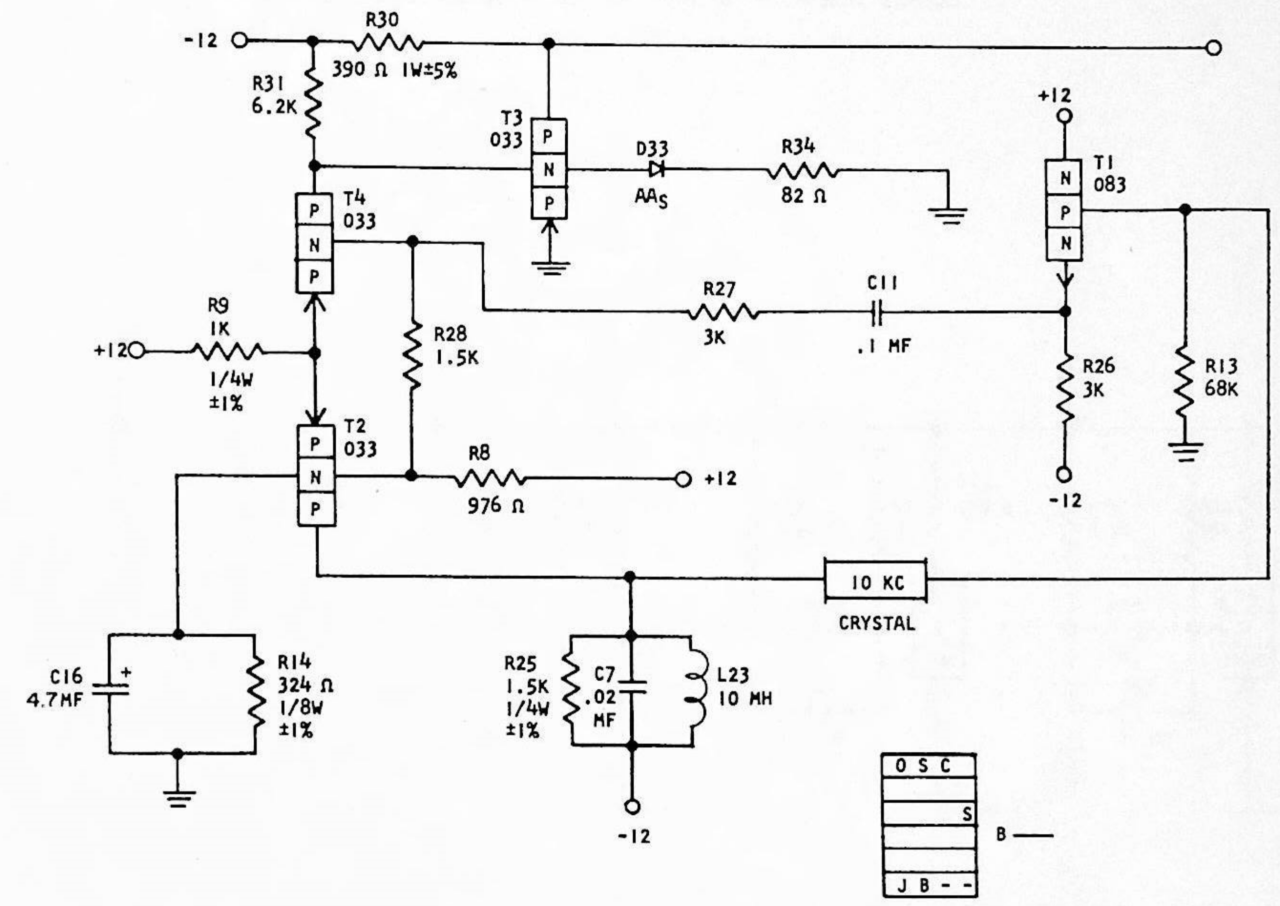
729932

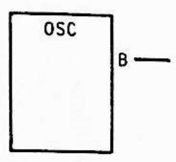
CARD CODE	729932
JB --	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371245

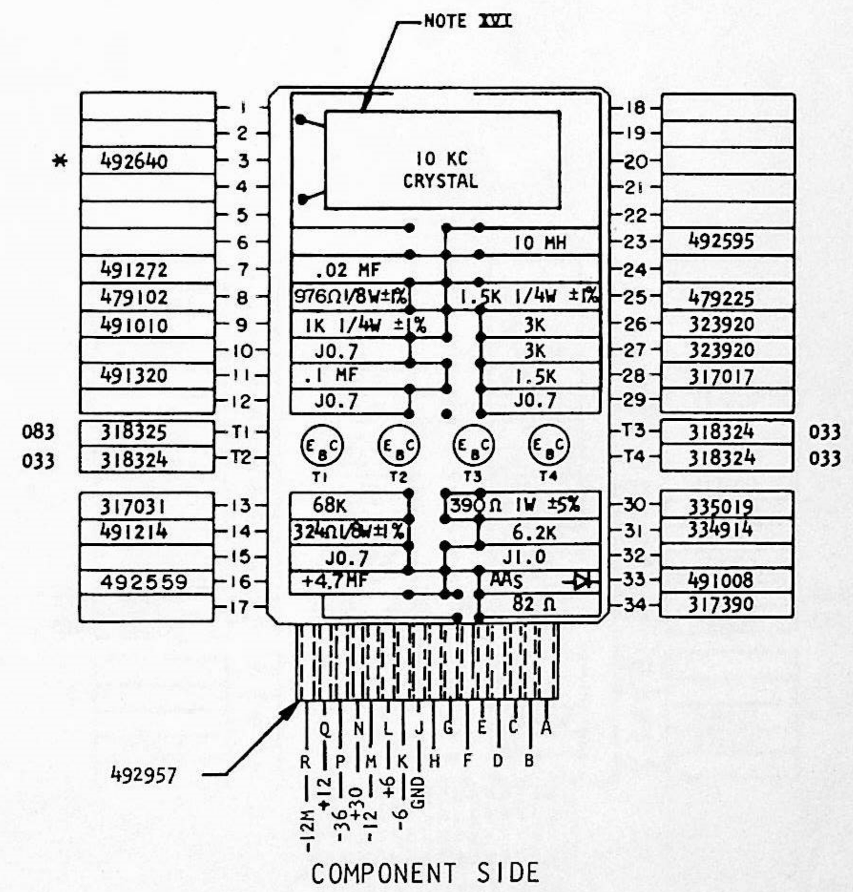
CTRL-OSCILLATOR, 10 KC FREE RUNNING (CRYSTAL)





SEQUENCE OF OPERATION

1. WHEN POWER IS UP, OSCILLATOR TURNS ON



PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
B	S	OUTPUT	10 KC	UP	0	-.2
				DOWN	-11.8	-12.12

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.			
NAME	CARD ASM TSTR - CTRL OSC, 10KC FREE RUNNING CRYSTAL		
DESIGN		MODEL	SMS
DETAIL	RQ 3-1-62	SCALE	NONE
CHECK	WH 3-1-62	DRAW	LIG 3-17-62
APPRO		CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
4-24-62	115599					

729932

C

STANDARDS CODE

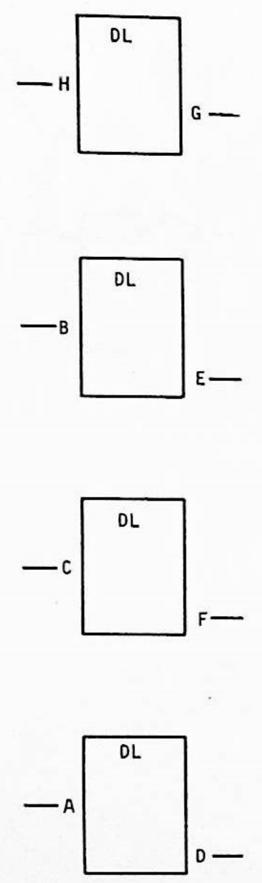
729933

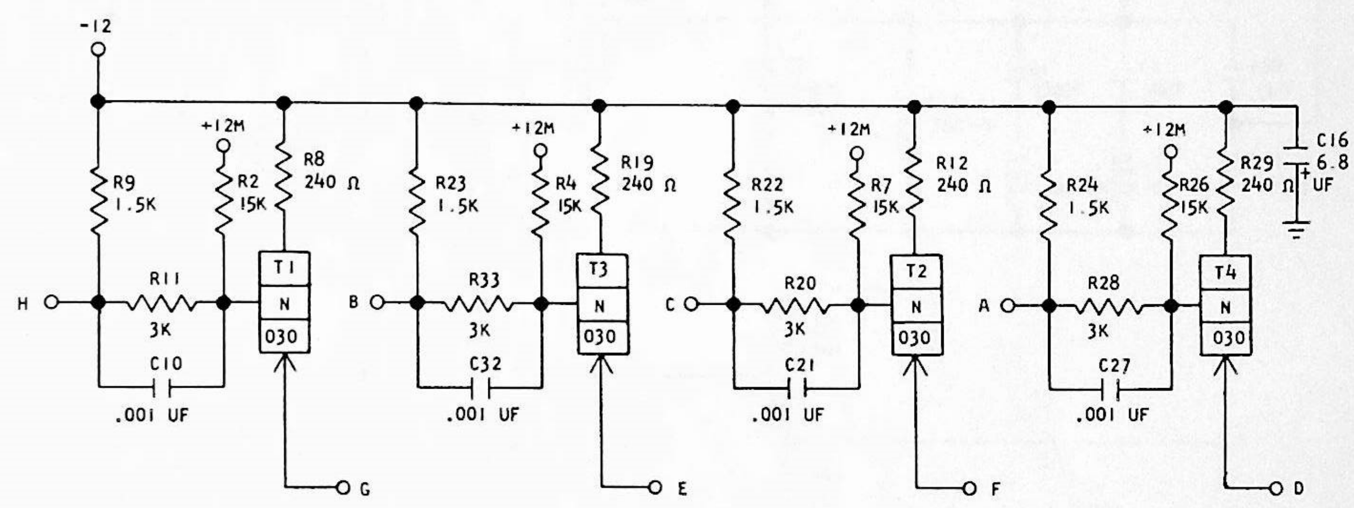
CARD CODE	729933
T A B -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370066

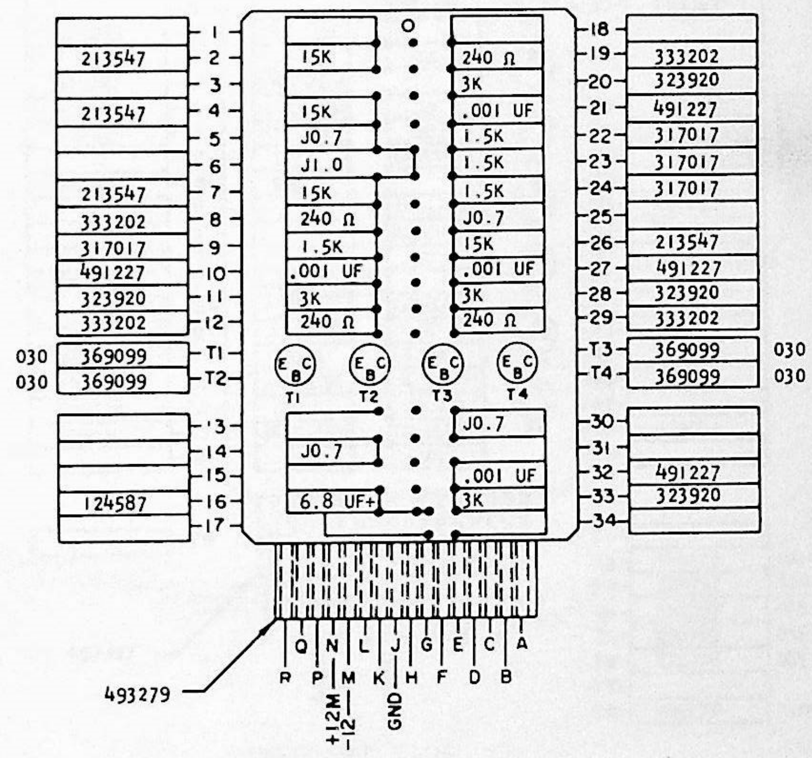
SDTRL 93Ω COAX LINE DRIVER-DISPERSED LOADS





SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT DOWN
2. INPUT UP TRANSISTOR OFF OUTPUT UP



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	MAX
H,B, C,A	S	INPUT		UP	-.6	0
				DOWN	-1.14	-8.15
G,E, F,D	N	OUTPUT		UP	+0.8	
				DOWN	-0.8	
G,E, F,D	R	OUTPUT		UP	12.	
				DOWN	0.0	

DELAY - NSEC - DISPERSED LOADS:

	MINIMUM	MAXIMUM
TURN ON	10	40
TURN OFF	0	10

DELAY - NSEC - "DOT-ORING"

	MINIMUM	MAXIMUM
TURN ON	16	52
TURN OFF	0	10

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL 93 Ω				6 -, -62	115599					
COAX LINE DRIVER-DISPERSED LOADS											
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729933

C

729934

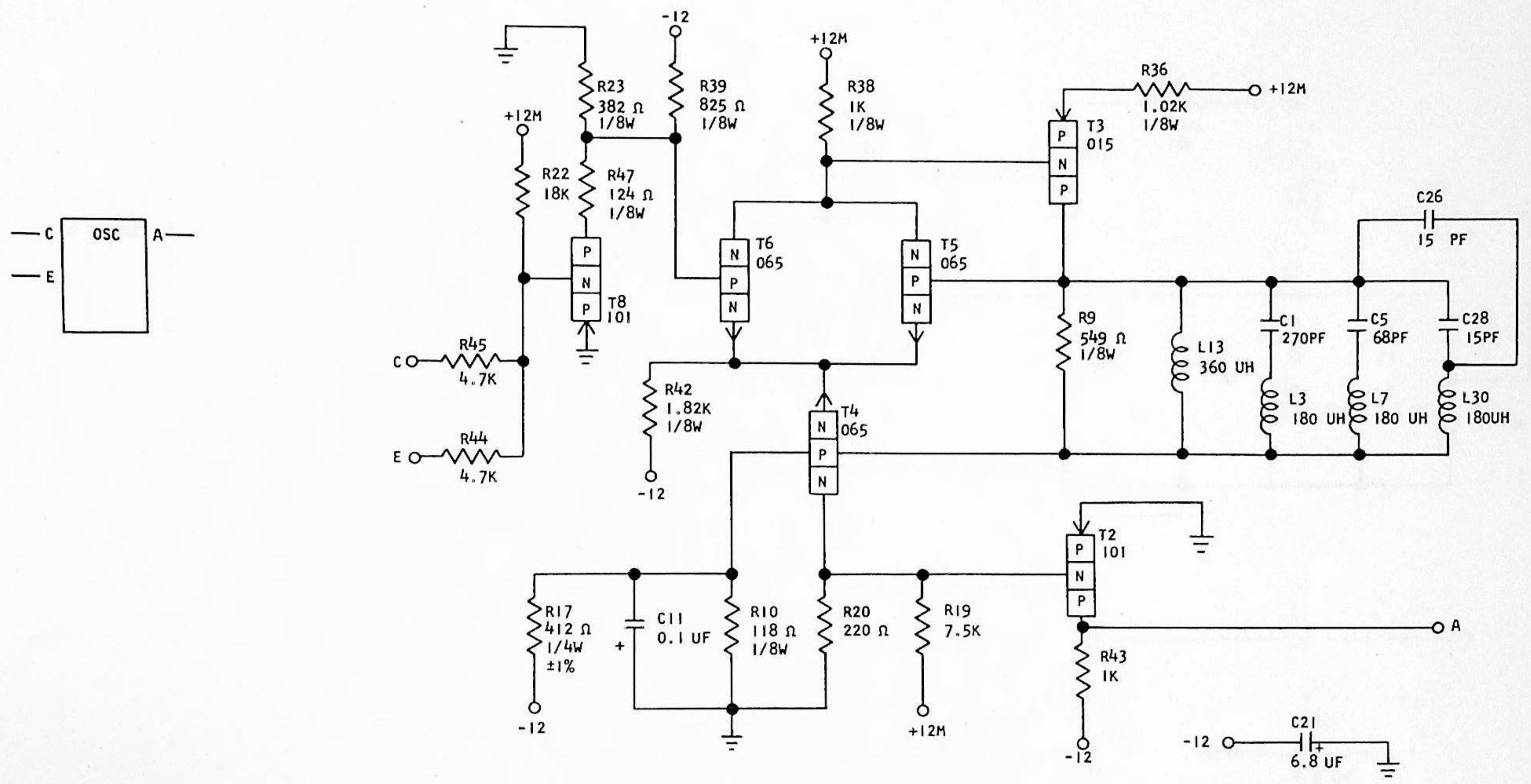
STANDARDS CODE

CARD CODE	729934
T B G -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370296

SDTRL - OSCILLATOR, 320 KC S LINE GATED



SEQUENCE OF OPERATION

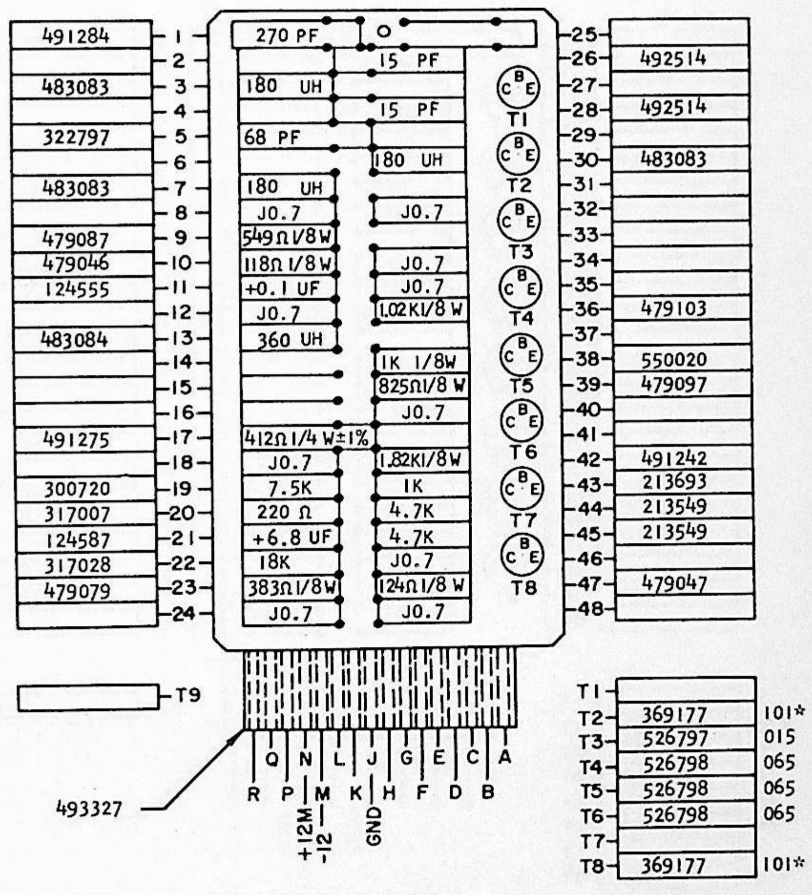
1. WHEN C AND E ARE UP, T8 TURNS OFF, OSCILLATOR TURNS ON
2. WHEN C OR E ARE DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS	
					MIN	MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	70	100
TURN OFF*	160	200
RISE TIME	52	66
FALL TIME	42	60

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL OSC			6 / -62	115599					
	320 KC S LINE GATED									
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729934

C

STANDARDS CODE

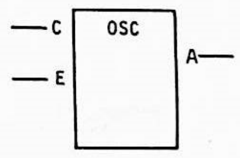
729935

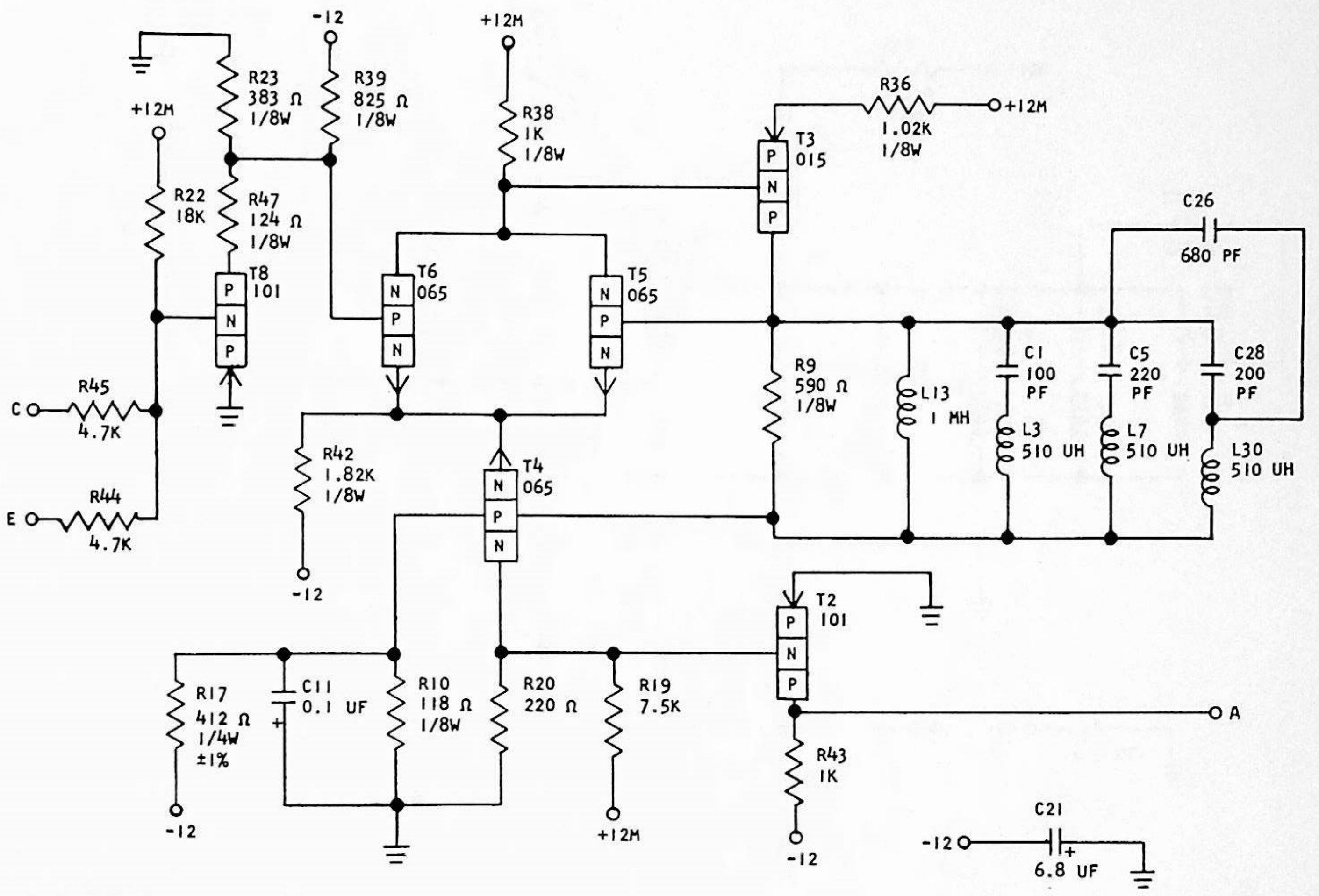
CARD CODE	729935
T B Q -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370295

SDTRL - OSCILLATOR, 115 KC S LINE GATED





SEQUENCE OF OPERATION

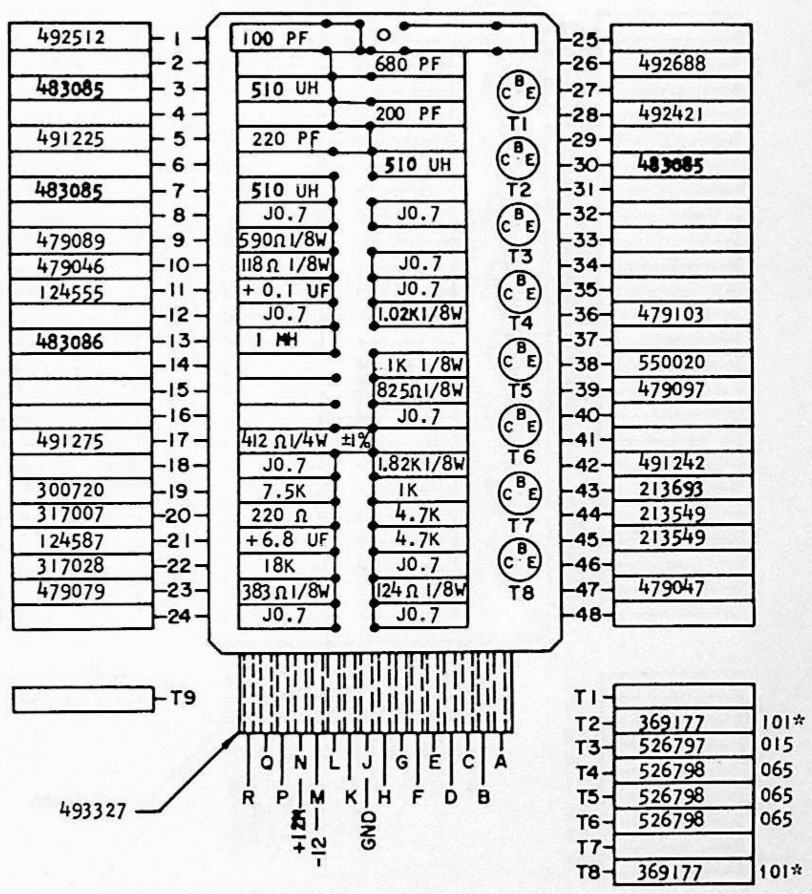
1. WHEN C AND E ARE UP, T8 TURNS OFF, OSCILLATOR TURNS ON
2. WHEN C OR E IS DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT	115 KC	UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	60	130
TURN OFF*	110	190
RISE TIME	28	82
FALL TIME	21	58

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL-OSC, 115 KC S LINE GATED			4-20-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729935

C

STANDARDS CODE

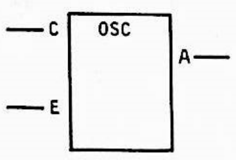
729936

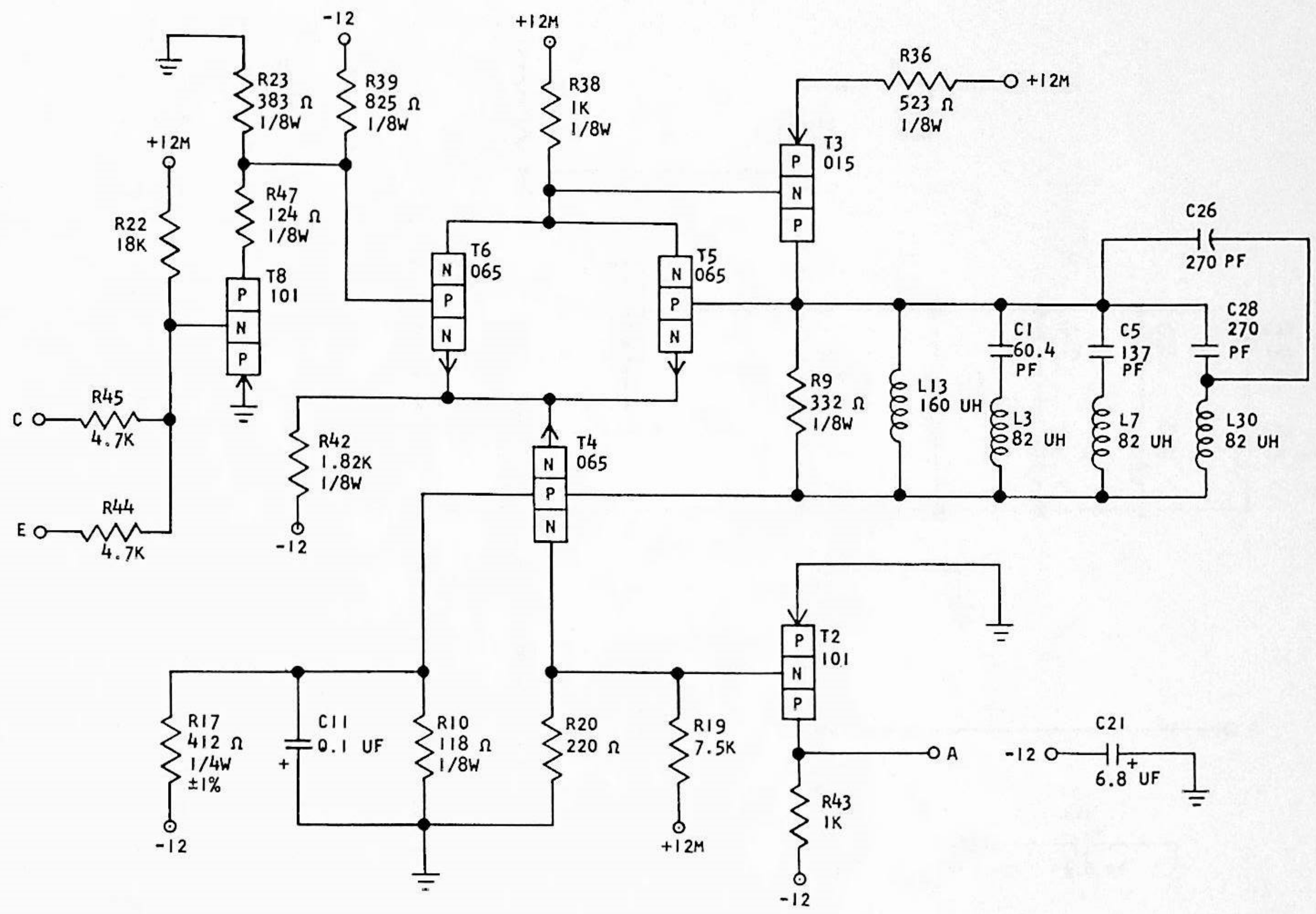
CARD CODE	729936
T B R -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370297

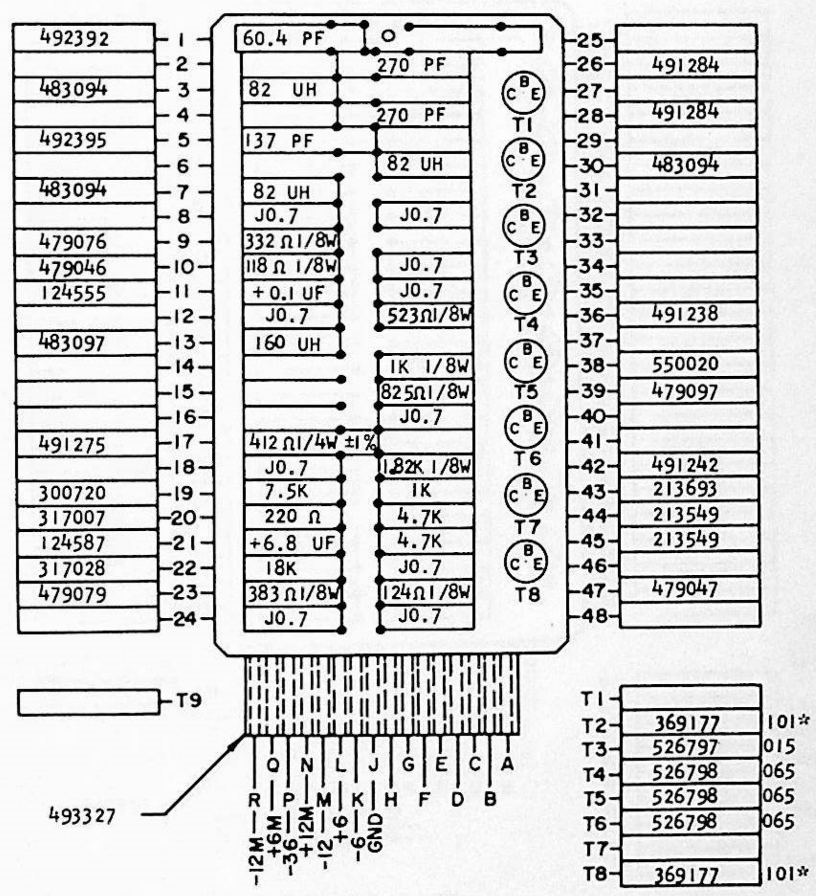
SDTRL - OSCILLATOR, 360 KC S LINE GATED





SEQUENCE OF OPERATION

1. WHEN C AND E ARE UP, T8 TURNS OFF, OSCILLATOR TURNS ON
2. WHEN C OR E IS DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT	360 KC	UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	70	110
TURN OFF*	160	200
RISE TIME	28	52
FALL TIME	46	54

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.

NAME	CARD ASM TSTR-SDTRL-OSC, 360 KC S LINE GATED		
DESIGN		MODEL	SMS
DETAIL	RQ 3-1-62	SCALE	NONE
CHECK	WH 3-1-62	DRAW	LIG 3-17-62
APPRO		CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-17-62	115599					

729936

C

STANDARDS CODE

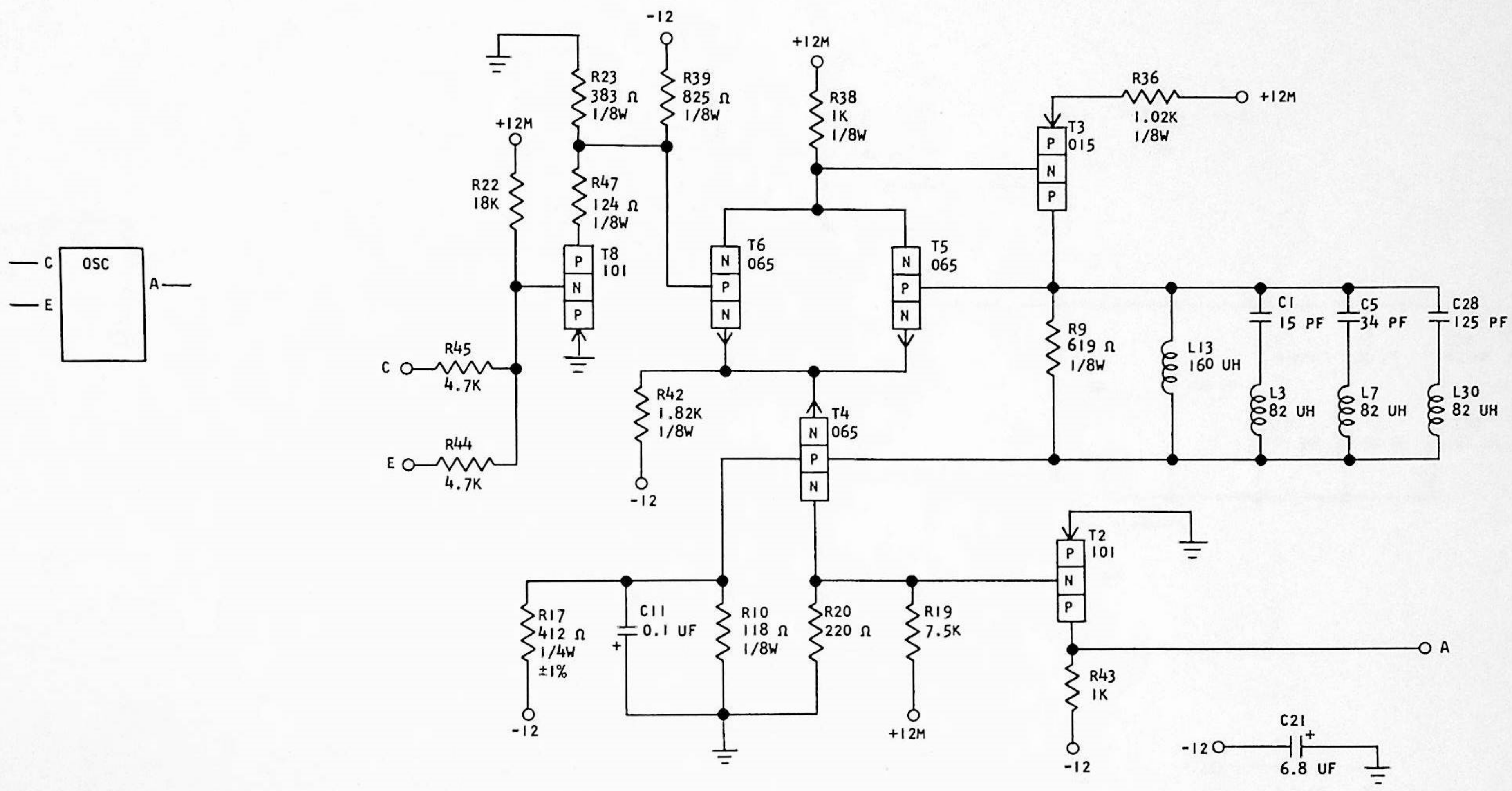
729937

CARD CODE	729937
T B S -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370298

SDTRL - OSCILLATOR, 667 KC S LINE GATED



SEQUENCE OF OPERATION

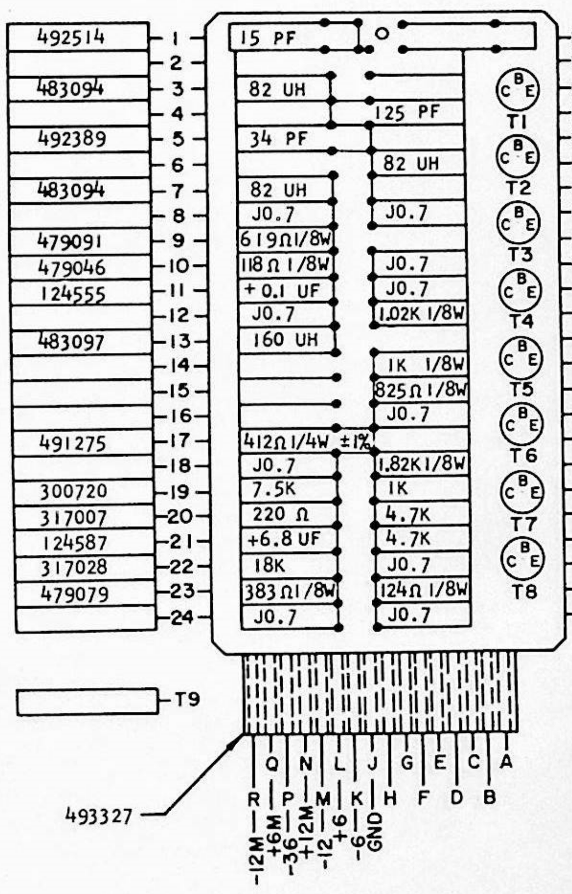
1. WHEN C AND E ARE UP, T8 TURNS OFF, OSCILLATOR TURNS ON
2. WHEN C OR E IS DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT	667 KC	UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	70	110
TURN OFF*	160	200
RISE TIME	36	52
FALL TIME	48	62

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.



T1		
T2	369177	101*
T3	526797	015
T4	526798	065
T5	526798	065
T6	526798	065
T7		
T8	369177	101*

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTRL-OSC, 667 KC S LINE GATED			-62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729937

C

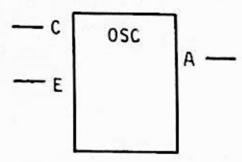
STANDARDS CODE
729938

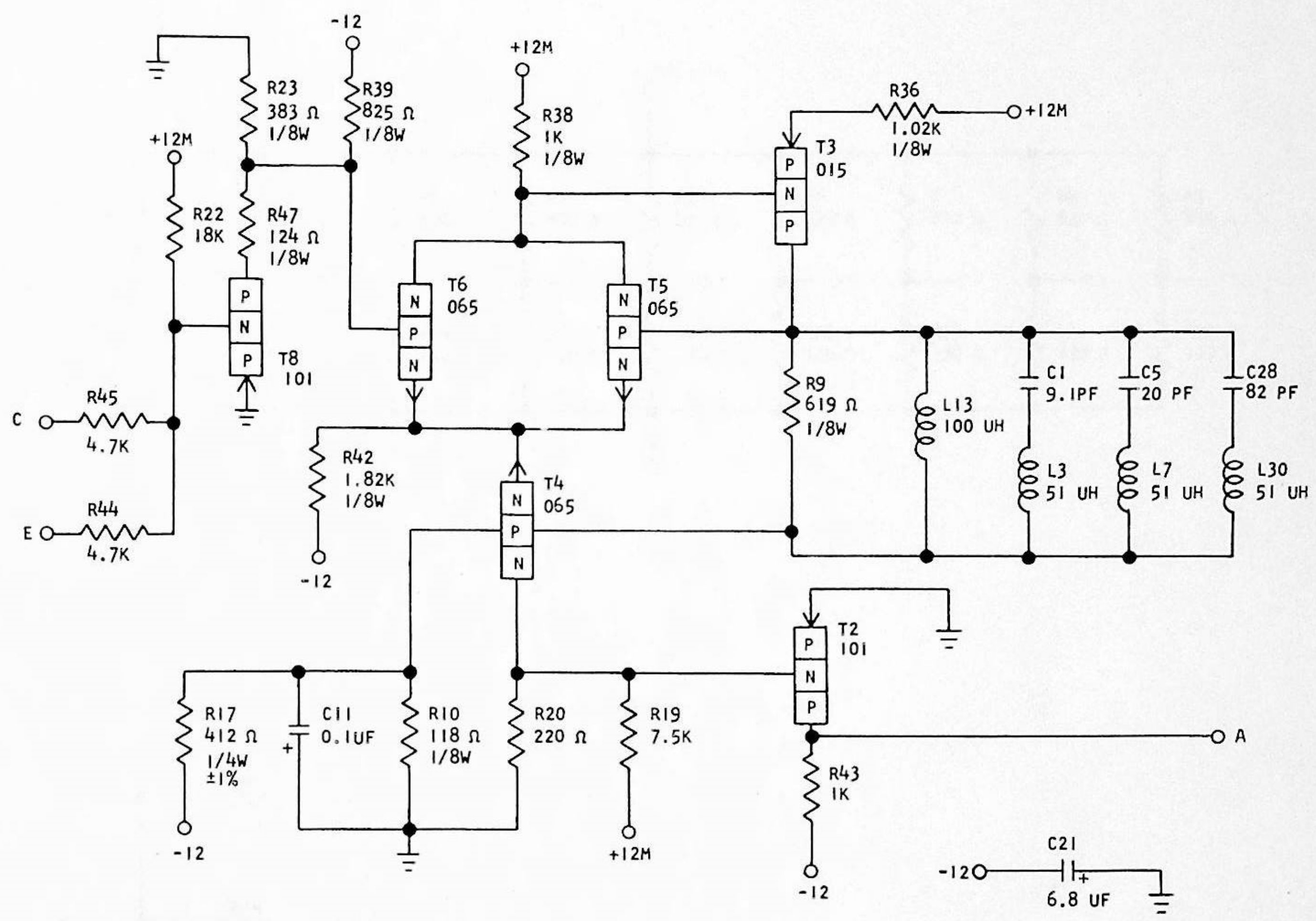
CARD CODE	729938
T B V -	

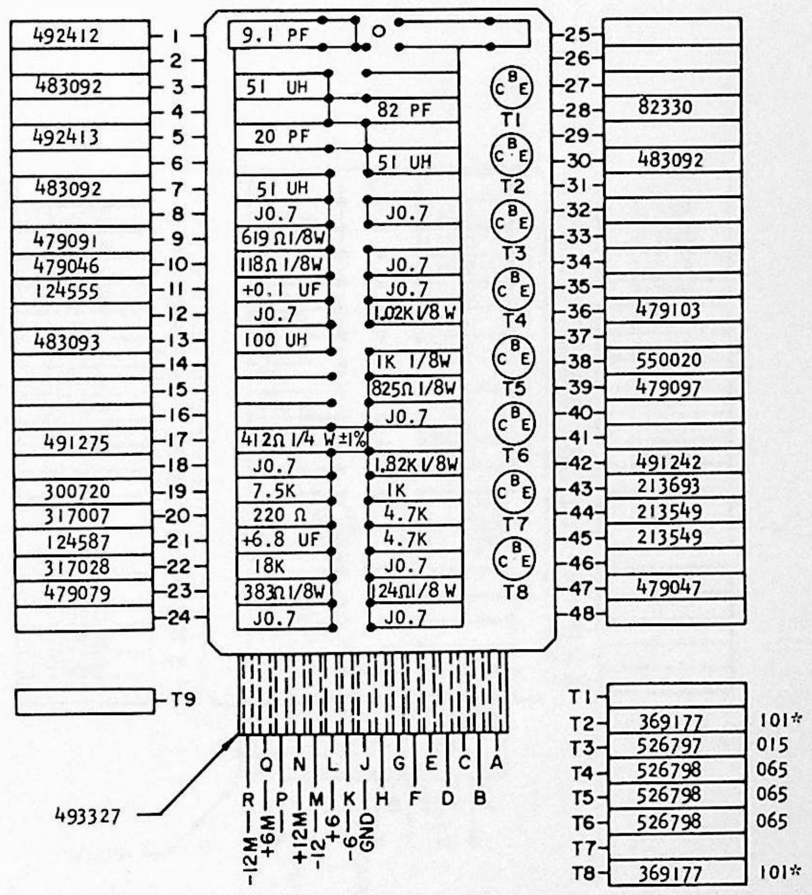
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370299

SDTRL - OSCILLATOR, 1 MC S LINE GATED







COMPONENT SIDE

SEQUENCE OF ODERATION

1. WHEN C & E ARE UP, T8 TURNS OFF, OSCILLATOR TURNS ON
2. WHEN C OR E IS DOWN, T8 TURNS ON, OSCILLATOR TURNS OFF

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
C,E	S	INPUT		UP	-.45	-.05
				DOWN	-6.87	-12.5
A	S	OUTPUT	1MC	UP	-.45	-.05
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	70	120
TURN OFF*	80	200
RISE TIME	52	110
FALL TIME	42	220

*APPLIES ONLY WHEN GATING, WHEN OUTPUT IS AT A + S LEVEL.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- SDTRL-OSC,				-62	115599					
	1 MC S LINE GATED										
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729938

C

STANDARDS CODE

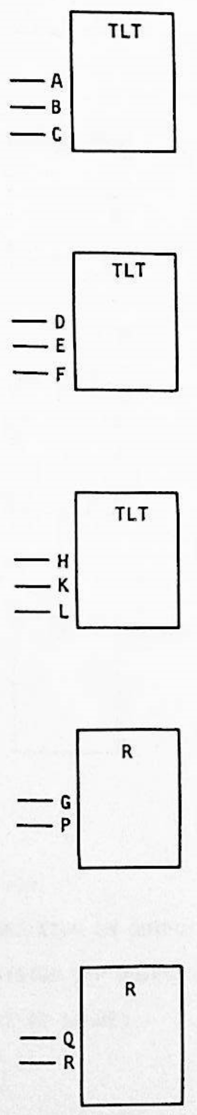
729939

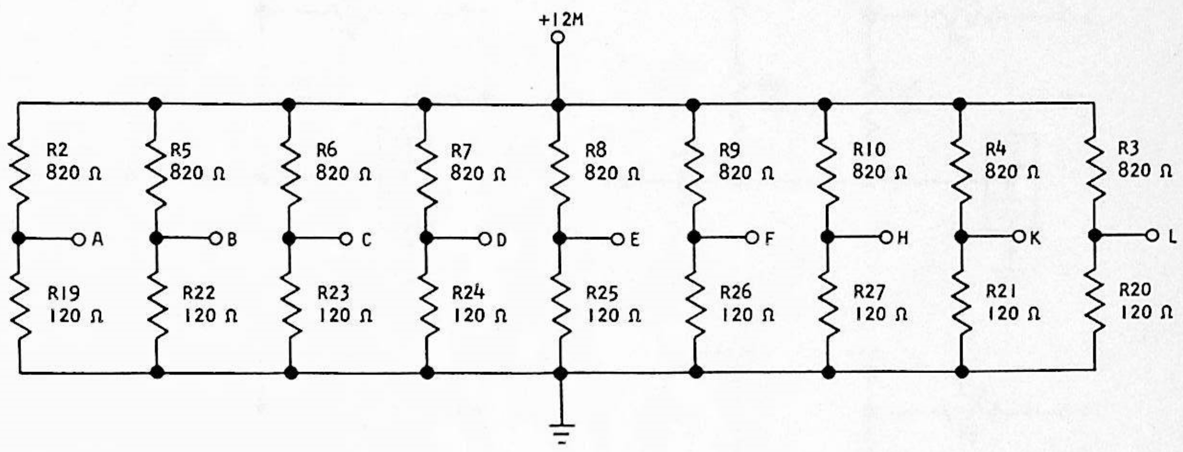
CARD CODE	729939
T C K -	

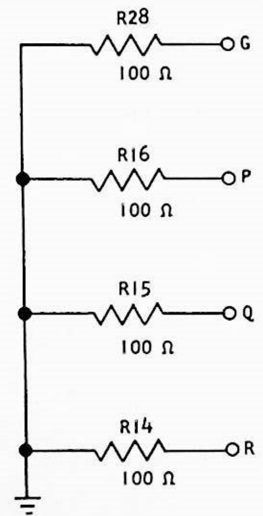
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370334

SDTRL - END OF LINE TERMINATORS

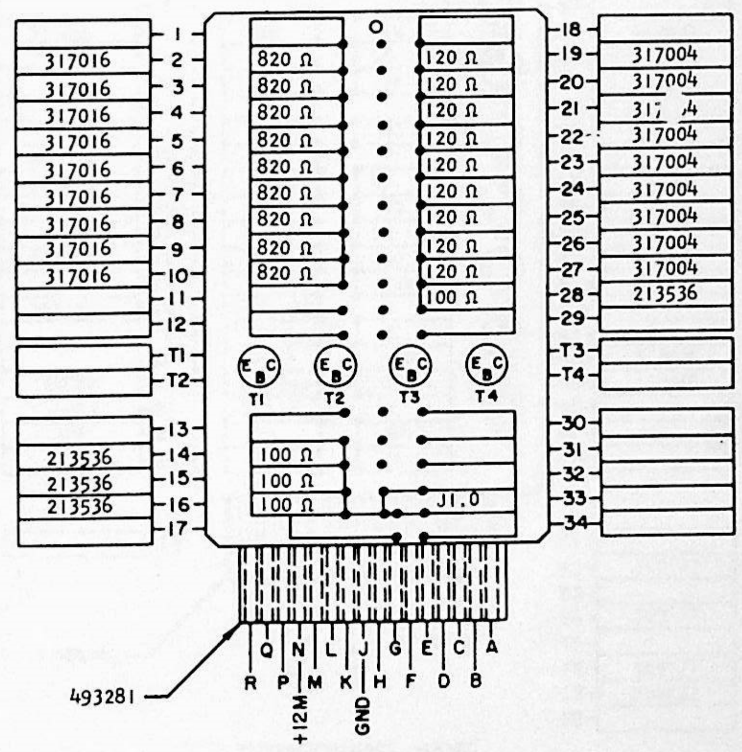






APPLICATION

1. 100Ω RESISTOR USED TO TERMINATE A SDTRL TRANSMISSION LINE
2. 820Ω AND 120Ω RESISTOR FORM COUPLING NETWORK WHICH ACTS AS A SPECIAL END OF LINE TERMINATOR FOR SDTRL COAXIAL LINE AND WITH ITS' INPUT PIN FORMS A SEPARATE CIRCUIT
3. EACH PIN REPRESENTS A SEPARATE NETWORK OR RESISTOR



COMPONENT SIDE

141

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - SDTRL - END OF LINE TERMINATORS			[illegible]-62	115599					729939
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

C

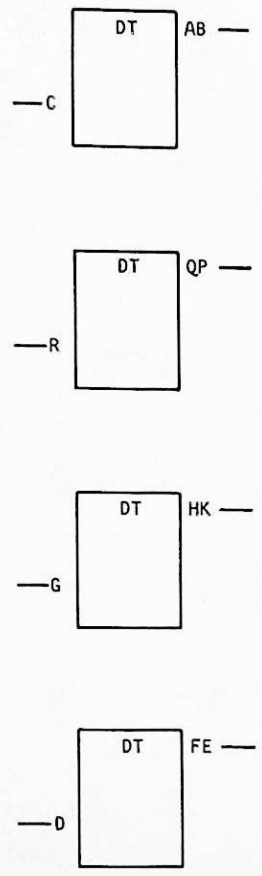
729940

STANDARDS CODE

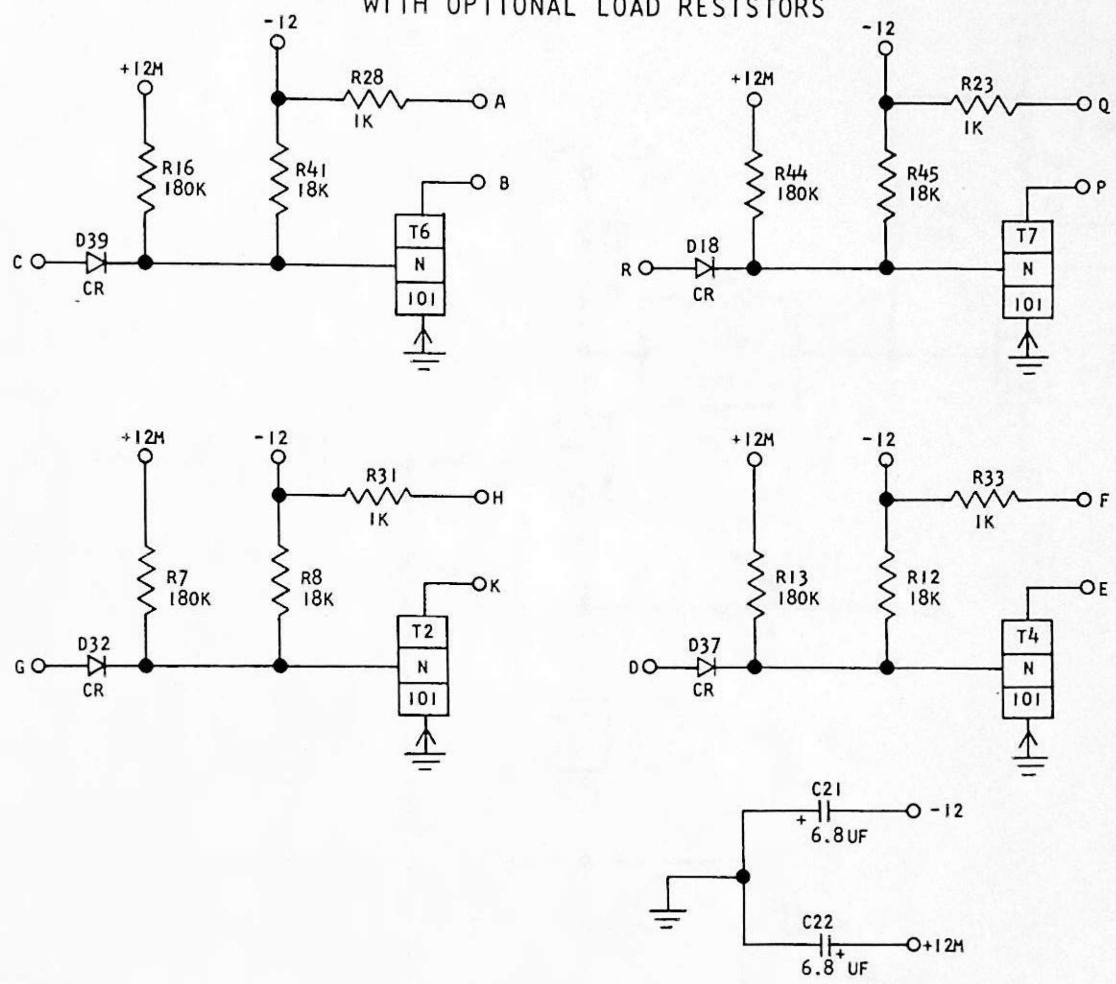
CARD CODE	729940
T D B -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370389

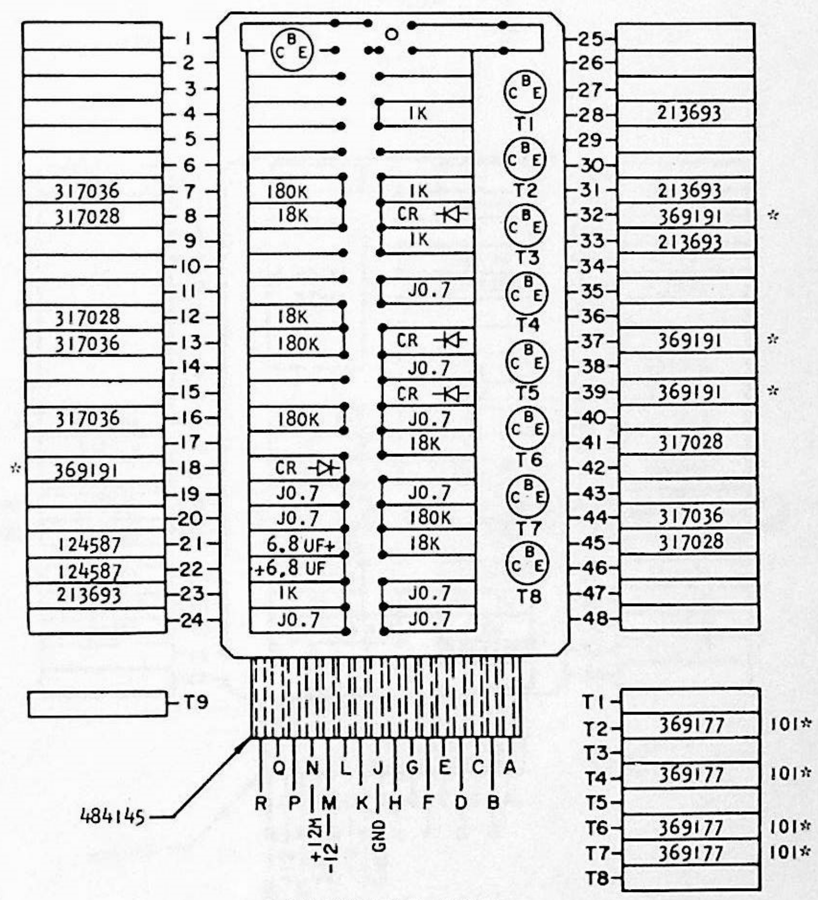


SDTRL-DISTRIBUTED LINE TERMINATOR
WITH OPTIONAL LOAD RESISTORS



SEQUENCE OF OPERATION

1. DOWN INPUT TRANSISTOR ON OUTPUT UP
2. UP INPUT TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS	
					MIN	MAX
C,R, G,D	N	INPUT		UP	+.65	
				DOWN	-.7	
B,P, K,E	Y	OUTPUT		UP	-.1	-.5
				DOWN	-6.87	-12.5

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	106	120☆
TURN OFF	108	126☆

☆FOR 100 FT OF CABLE.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - SDTRL- DISTRIBUTED LINE TERMINATOR					6 2 -62	115599					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WR	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729940

C

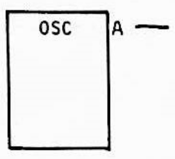
STANDARDS CODE
729941

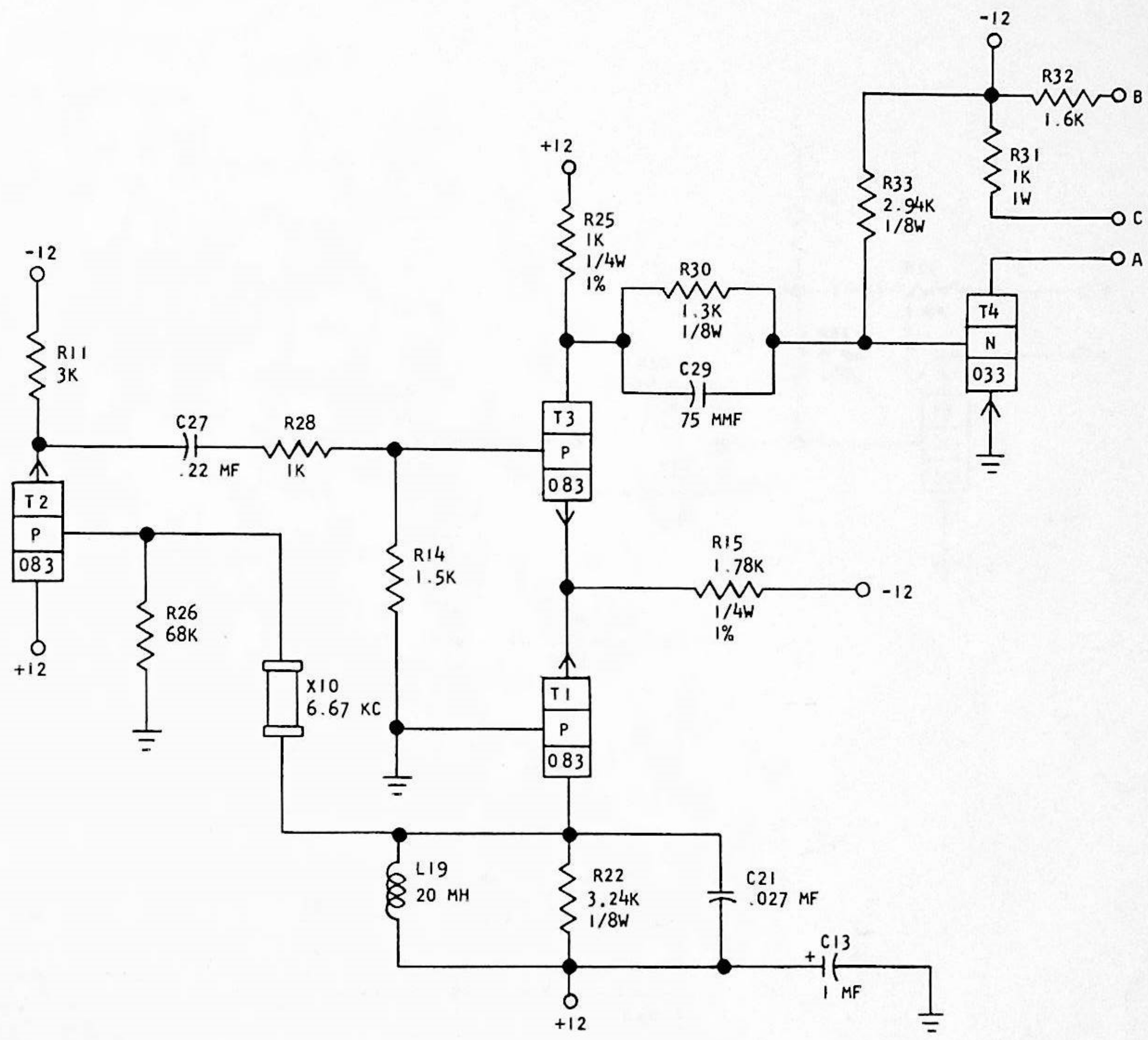
CARD CODE	729941
T D C -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370401

SDTDL-SDTRL - 6.67 KC OSCILLATOR

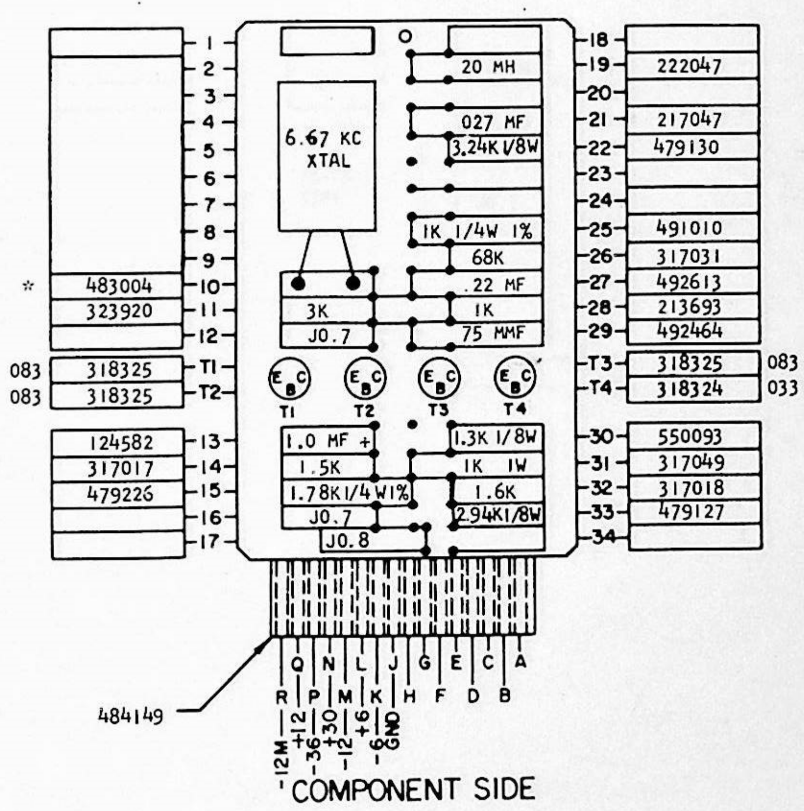




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON THE CURRENT REQUIREMENTS.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
A	S	OUTPUT	6.67KC	UP	-.5	-.1
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTL SDTRL-6.67 KC OSCILLATOR			-62	115599					729941
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

C

STANDARDS CODE

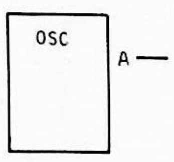
729942

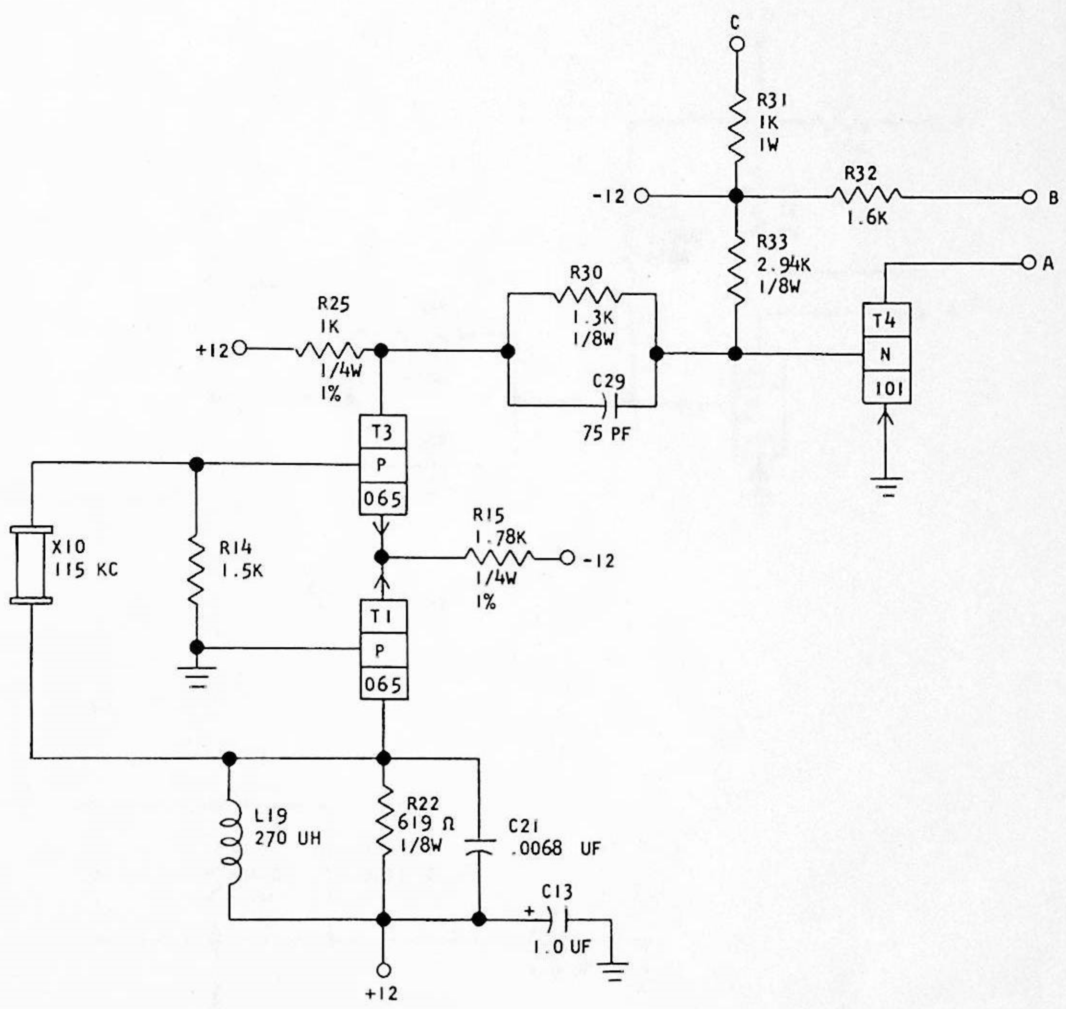
CARD CODE	729942
T D D -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370400

SDTDL-SDTRL - 115 KC OSCILLATOR

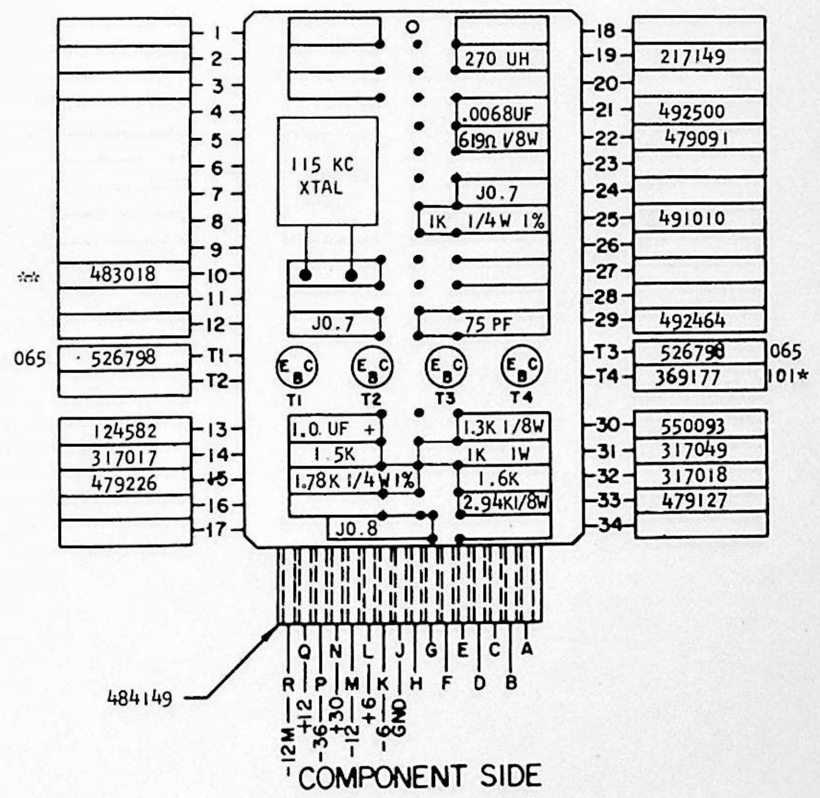




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	MAX
A	S	OUTPUT	115KC	UP	-.45	-.05
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR- SDTDL					62	115599					
SDTRL-115 KC OSCILLATOR											
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729942

C

729943

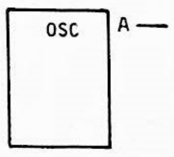
STANDARDS CODE

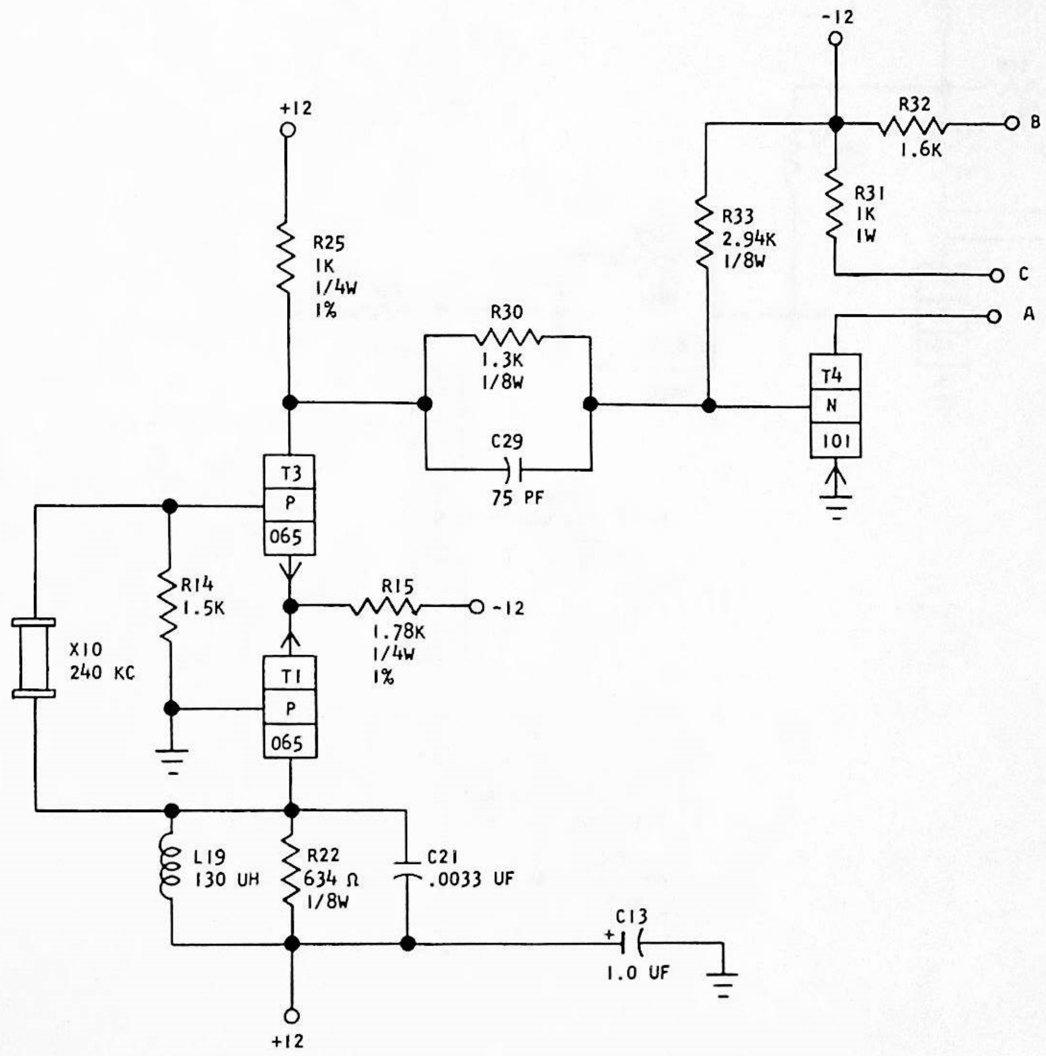
CARD CODE	729943
T D E -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370399

SDTDL-SDTRL-240 KC OSCILLATOR

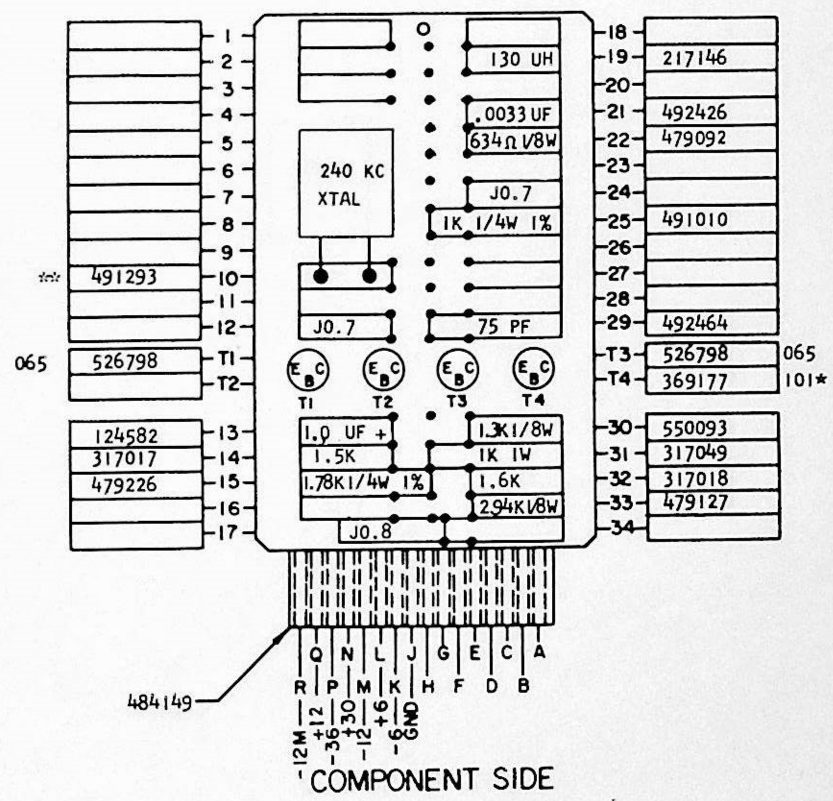




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CIRCUIT REQUIREMENTS

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MAX	MIN
				UP	-.45	-.05
A	S	OUTPUT	240 KC	DOWN	-.05	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL SDTRL-240 KC OSCILLATOR				-62	115599					
DESIGN		MODEL	SMS								
DETAIL	RQ 3-1-62	SCALE	NONE								
CHECK	WH 3-1-62	DRAW	LIG 3-17-62								
APPRO		CHECK									

729943

FORM 82-001

C

STANDARDS CODE

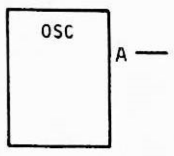
729944

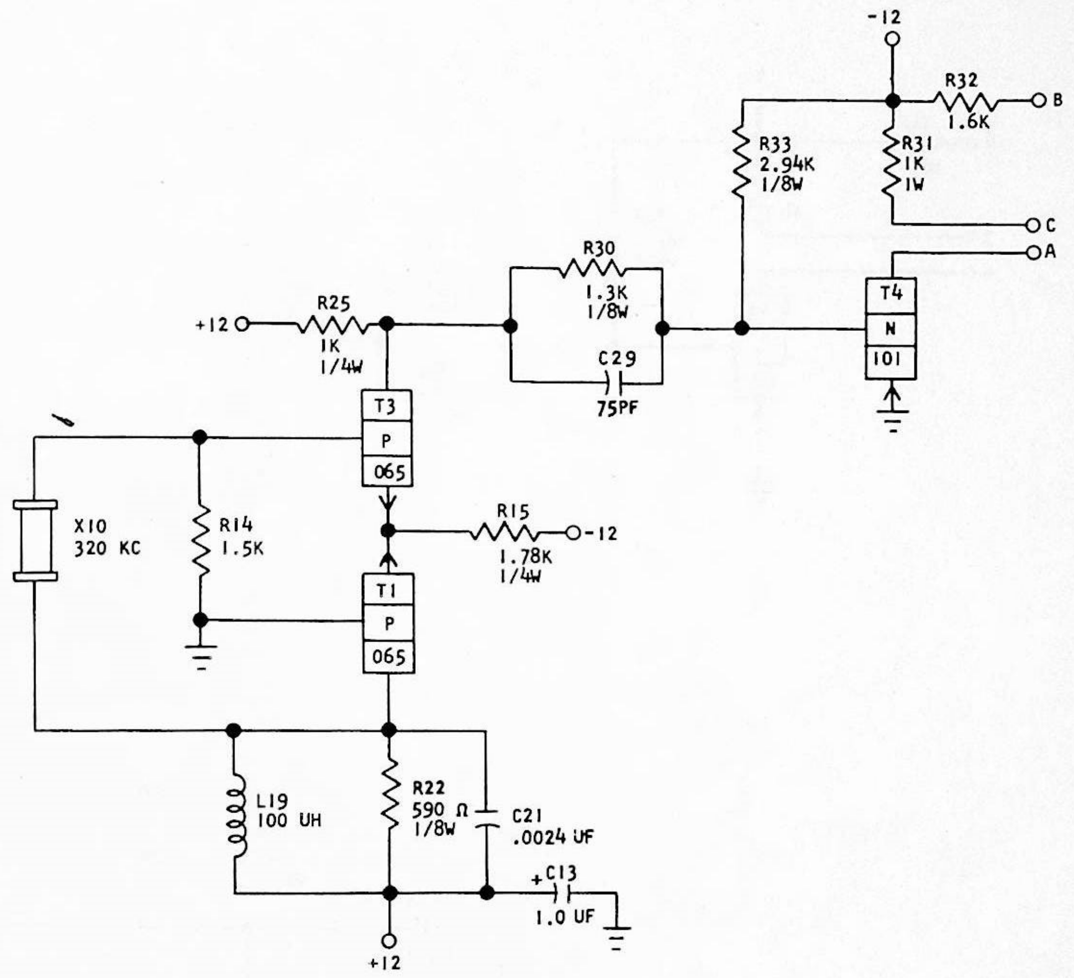
CARD CODE	729944
T D F -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370398

SDTDL-SDTRL-320 KC OSCILLATOR

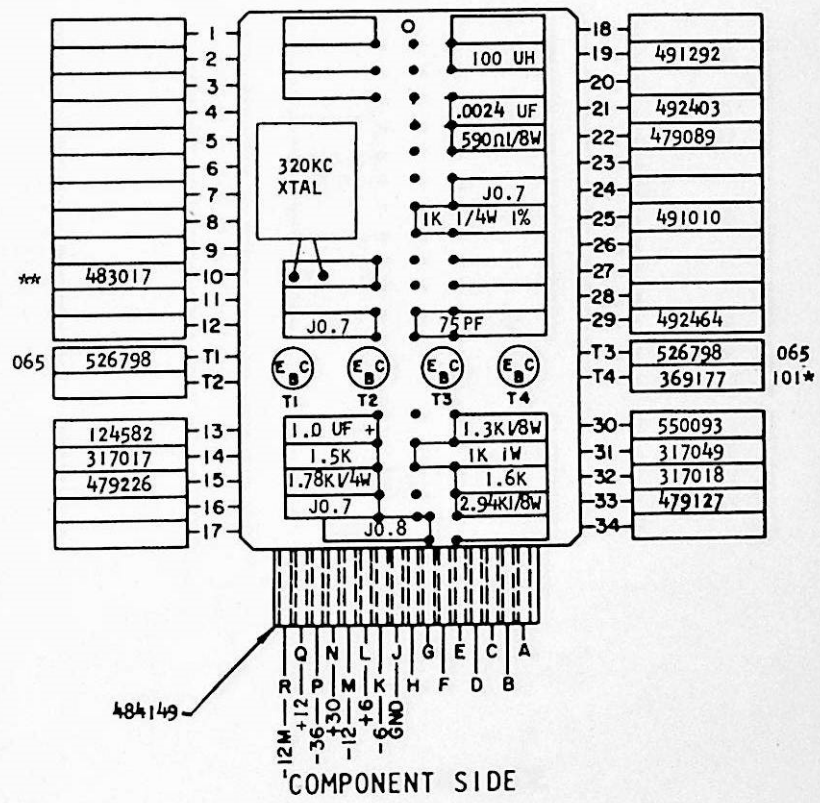




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
A	S	OUTPUT	320KC	UP	-.45	-.05
				DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL			[illegible] -62	115599					
	SDTRL-320 KC OSCILLATOR									
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729944

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STANDARDS CODE

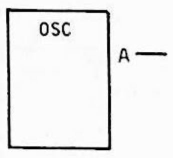
729945

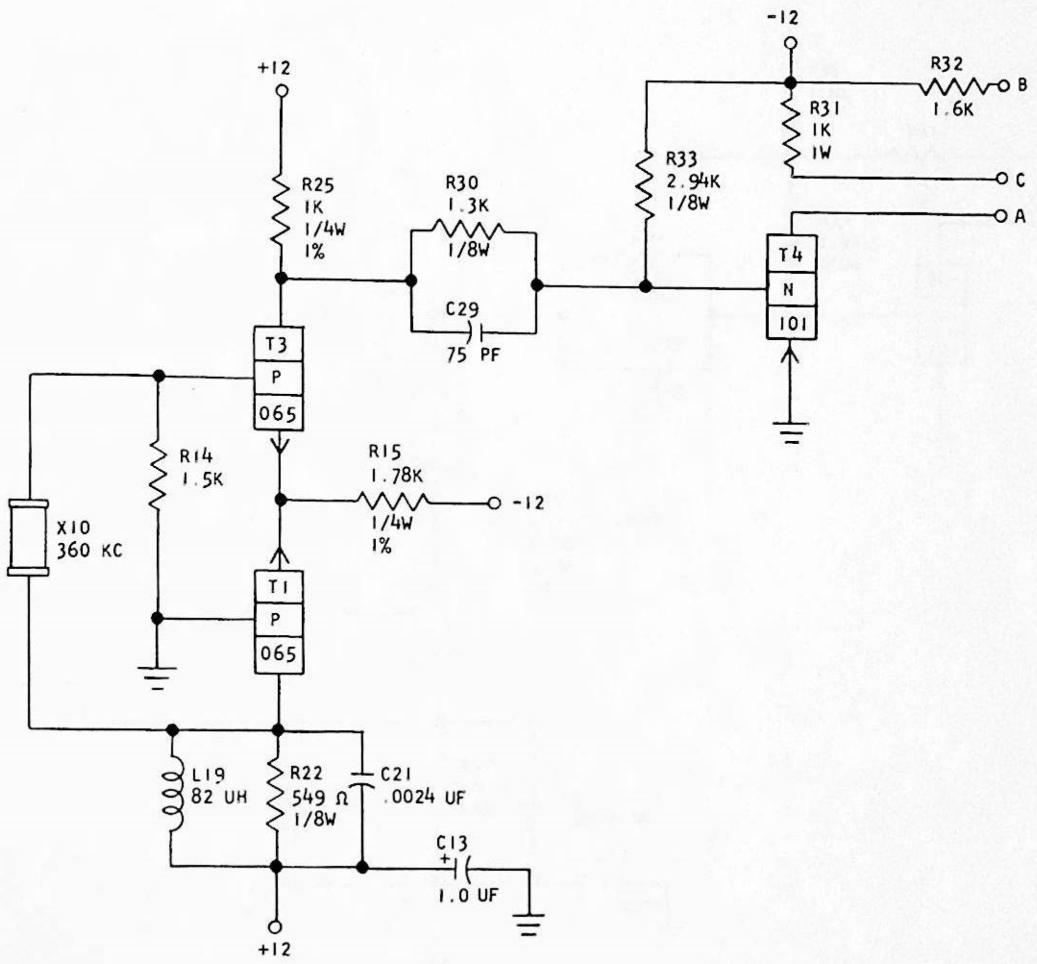
CARD CODE	729945
T D G -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370397

SDTDL- SDTRL - 360 KC OSCILLATOR

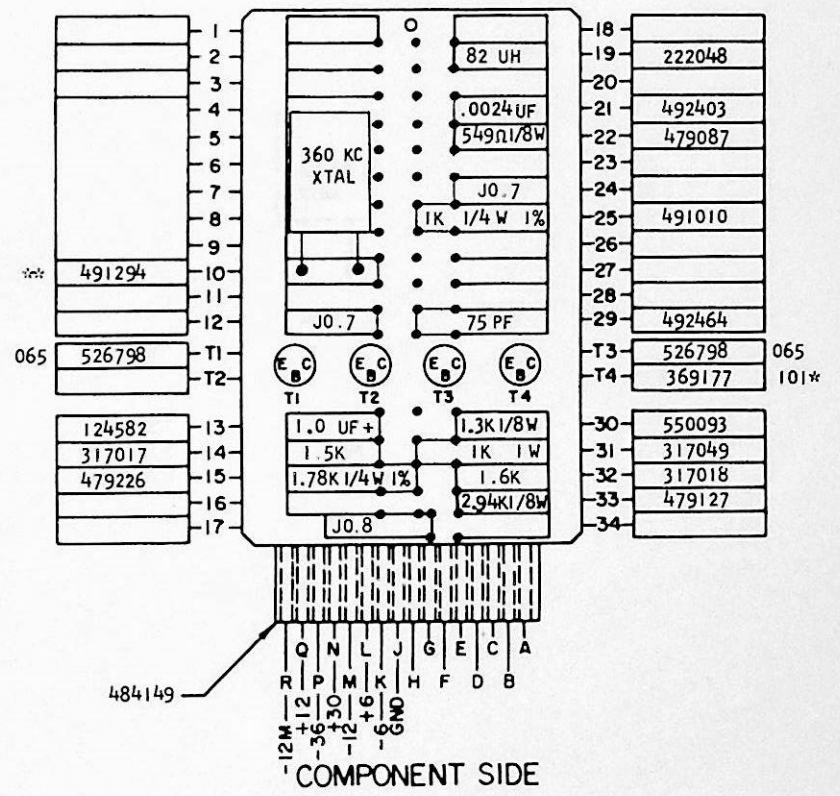




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS	
					MIN	MAX
				UP	-.45	-.05
A	S	OUTPUT	360 KC	DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL				[illegible] 62	115599					729945
	SDTRL - 360 KC OSCILLATOR										
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

C

STANDARDS CODE

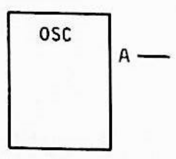
729946

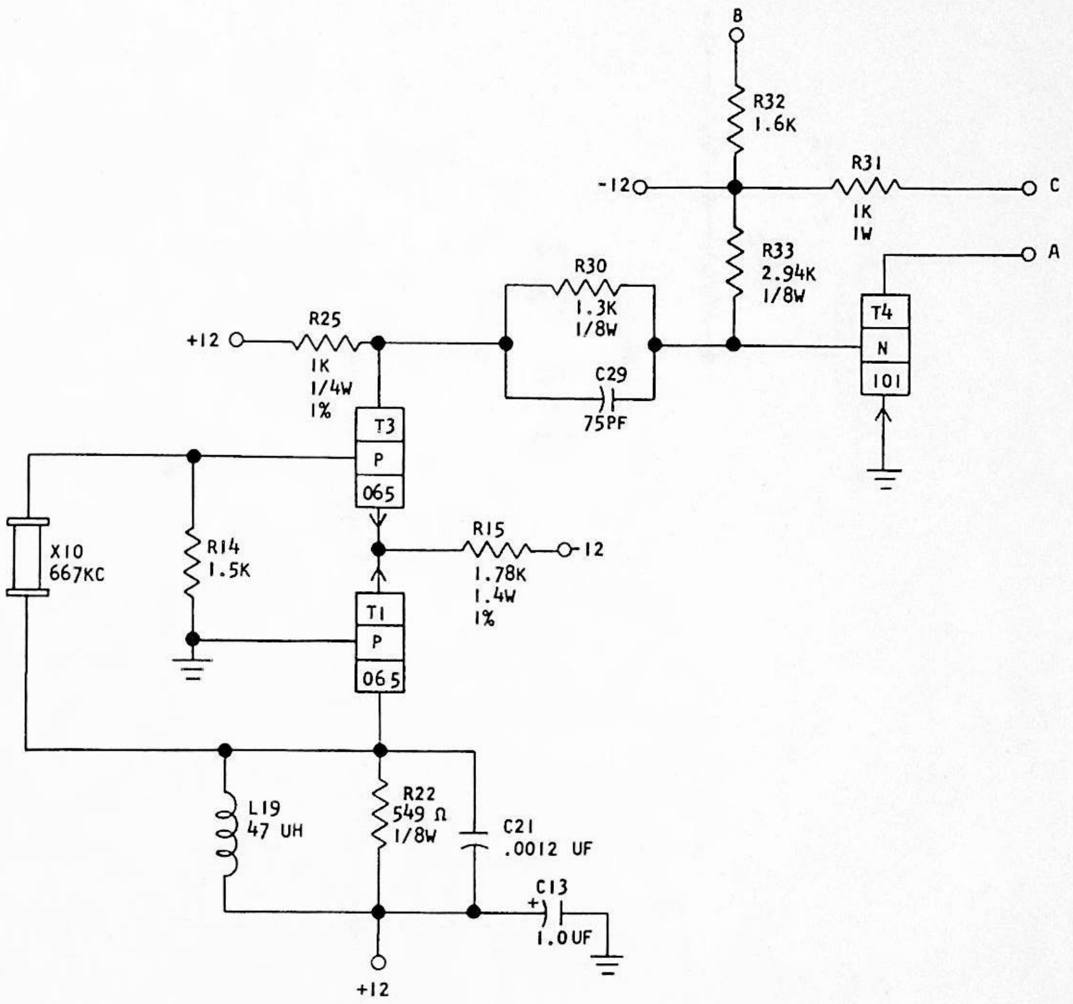
CARD CODE	729946
T D H -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370396

SDTDL-SDTRL-667 KC OSCILLATOR

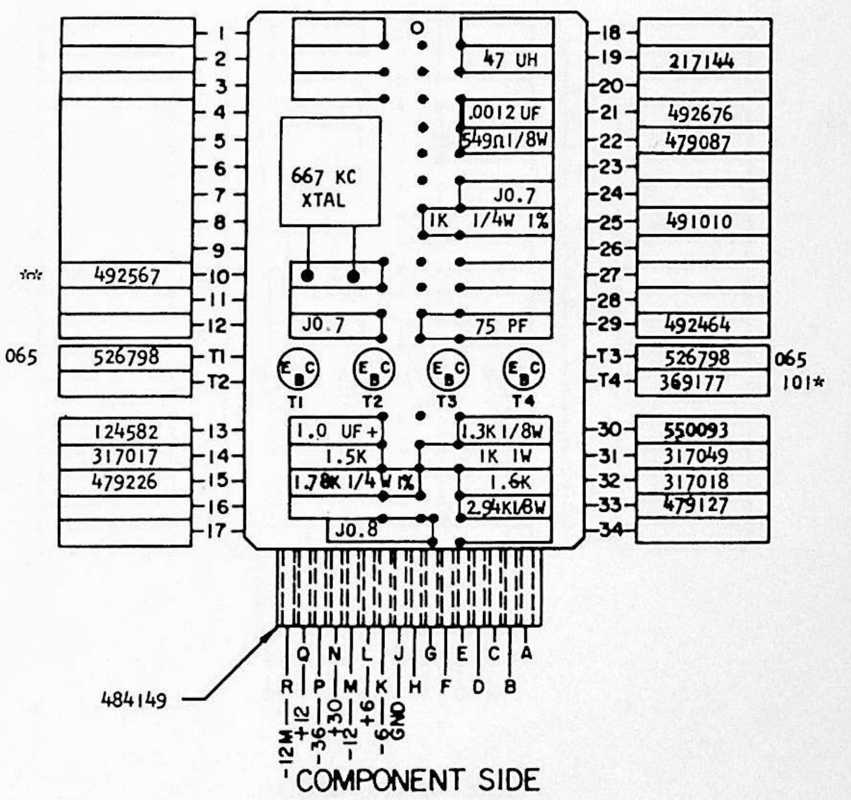




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS, DEPENDING ON CURRENT REQUIREMENTS

PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
				UP	-.45	-.05
A	S	OUTPUT	667KC	DOWN	-5.8	-12.48



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-SDTDL				-62	115599					
SDTRL-667 KC OSCILLATOR										
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729946

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STANDARDS CODE

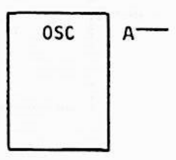
729947

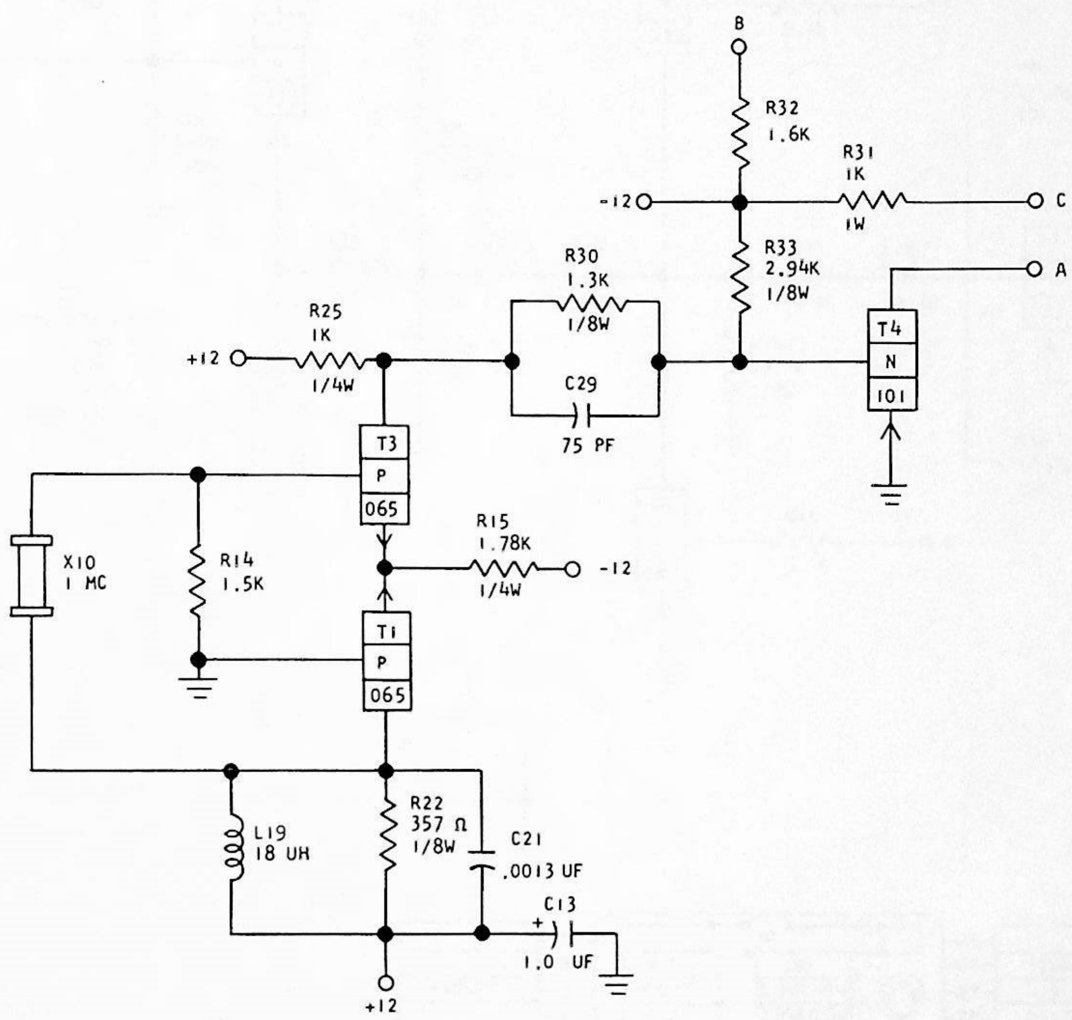
CARD CODE	729947
TDK-	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370551

SDTDL-SDTRL - 1 MC OSCILLATOR

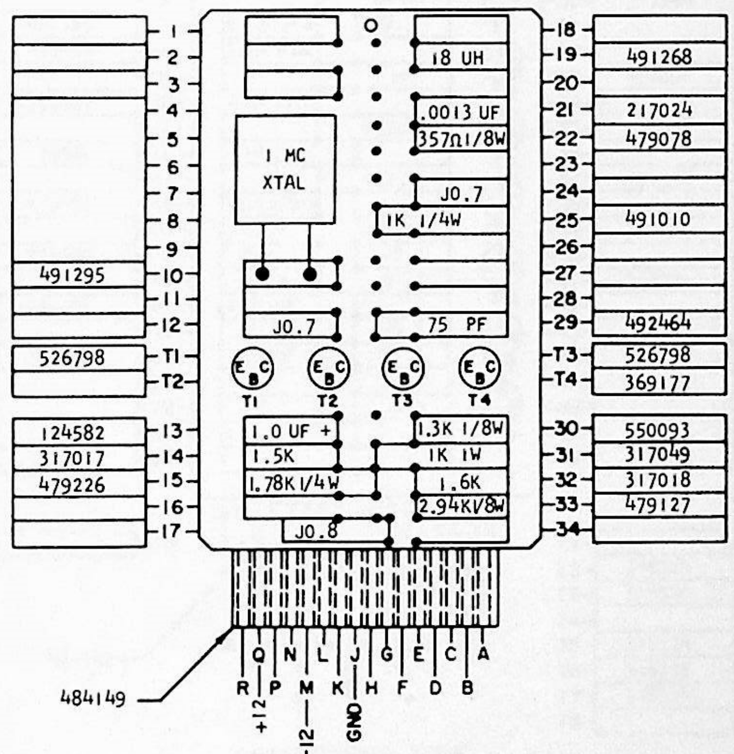




SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS DEPENDING ON CURRENT REQUIREMENTS.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS		
					MIN	MAX
A	S	OUTPUT	1MC	UP	-.3	0
				DOWN	-5.8	-12.48



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL-SDTRL-1 MC OSCILLATOR					62	115599					
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729947

C

STANDARDS CODE

729948

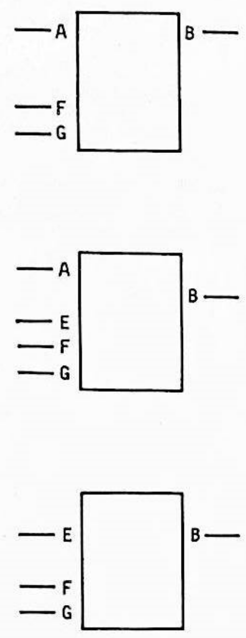
CARD CODE	729948
Y B Y -	

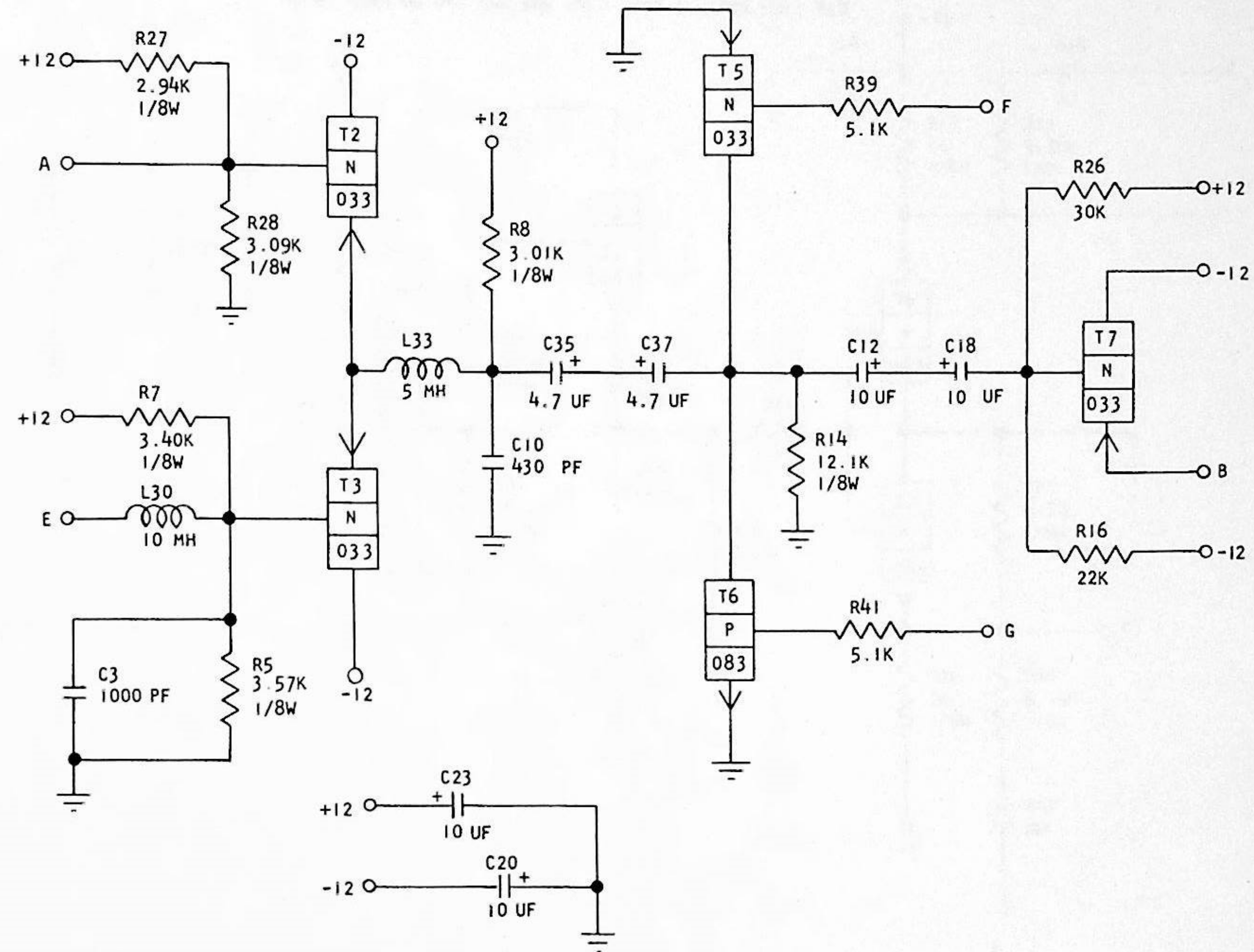
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370417

SENSE AMPLIFIER - INPUT FILTER AND SELECT GATE

MOUNT CARD ON ONE INCH CENTERS NOTE XVI

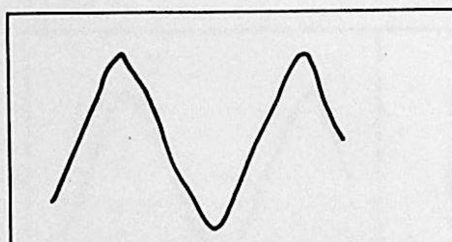




SEQUENCE OF OPERATION

1. PIN F AT +12V AND PIN G AT -12V FROM GATE ON FINAL AMPS. CARD
2. PIN B WAVE FORM WILL BE SAME AS INPUT WAVE FORM
3. TRANSISTOR THAT DOES NOT HAVE INPUT IS CUT OFF

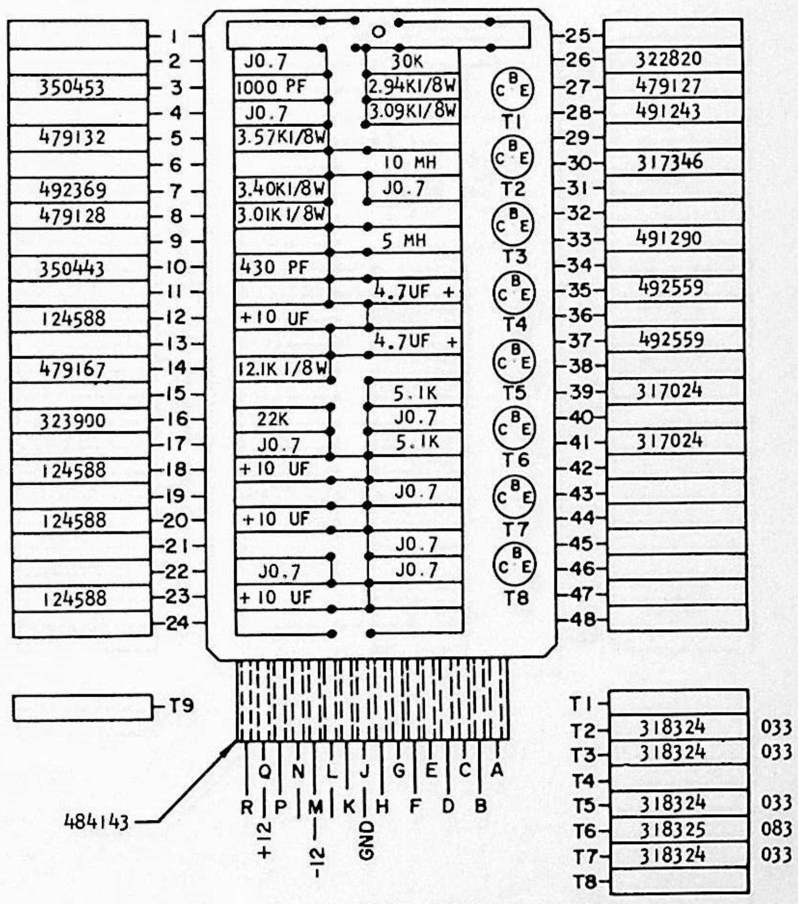
WAVE FORMS



INPUT WAVE 8V P-P — PIN A FOR 729, PIN E FOR 7330

MAX 8.8 P-P

REFERENCE LEVEL 0V +1.2 -.8



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SENSE AMPL			6 62	115599					
	INPUT FILTER AND SELECT GATE									
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729948

C

STANDARDS CODE
729949

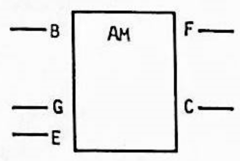
CARD CODE	729949
Y B Z -	

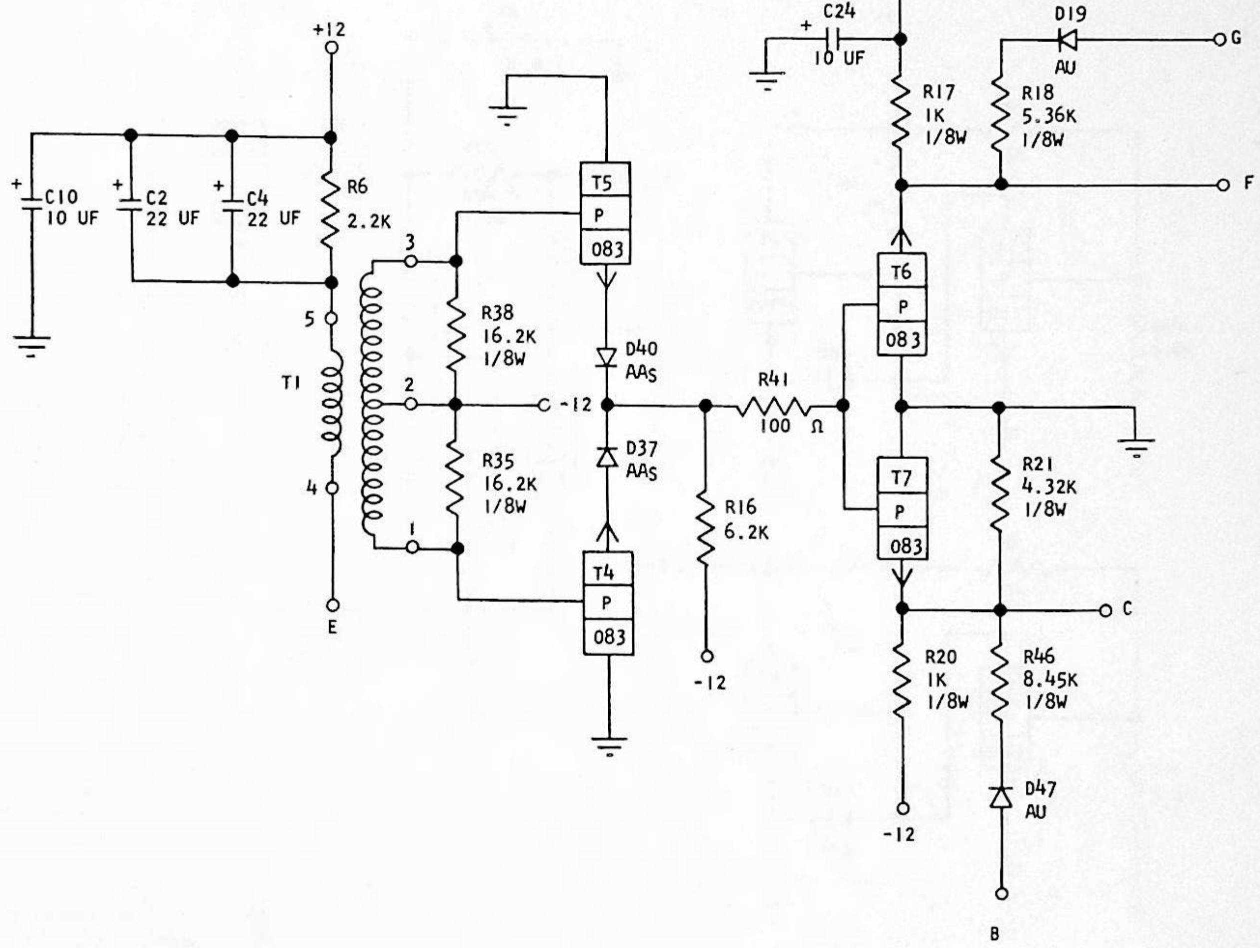
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370418

SENSE AMPLIFIER-RECTIFIER AND CLIPPER

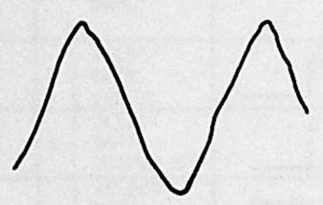
MOUNT CARD ON ONE AND ONE HALF INCH CENTERS NOTE XIV





APPLICATION NOTES

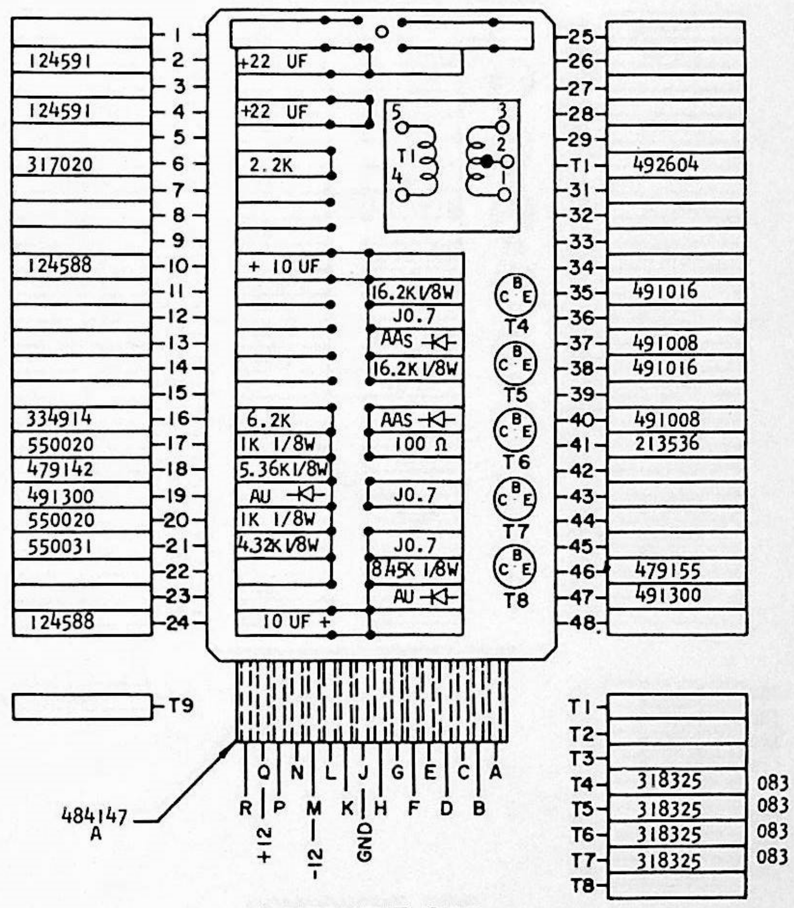
VOLTAGES AT PIN G AND B FROM CLIPPING CARD



INPUT WAVE FORM AT PIN E
7.6VP-P NOMINAL FOR HIGH FREQUENCY
7.2VP-P NOMINAL FOR LOW FREQUENCY
8.4VP-P MAXIMUM
REFERENCE LEVEL +1.59V TO -3.88V

OUTPUT WAVE FORM AT PIN C

1. LOW ACCEPTANCE CHANNEL
   OV TO 9V P-P READ CONDITIONS
   OV TO 7.5 P-P READ WHILE WRITE CONDITIONS
2. HIGH ACCEPTANCE CHANNEL
   OV TO 6.85V P-P READ CONDITIONS
   OV TO 6.18V P-P READ WHILE WRITE CONDITION



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - SENSE AMPLIFIER-RECTIFIER AND CLIPPER			6-14-62	115599					729949
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

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729950

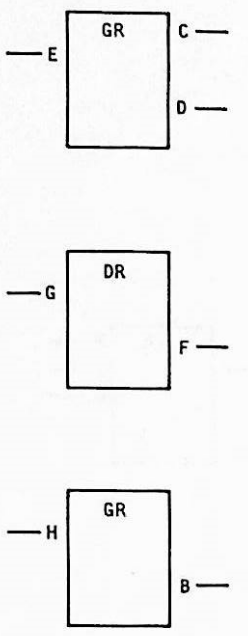
STANDARDS CODE

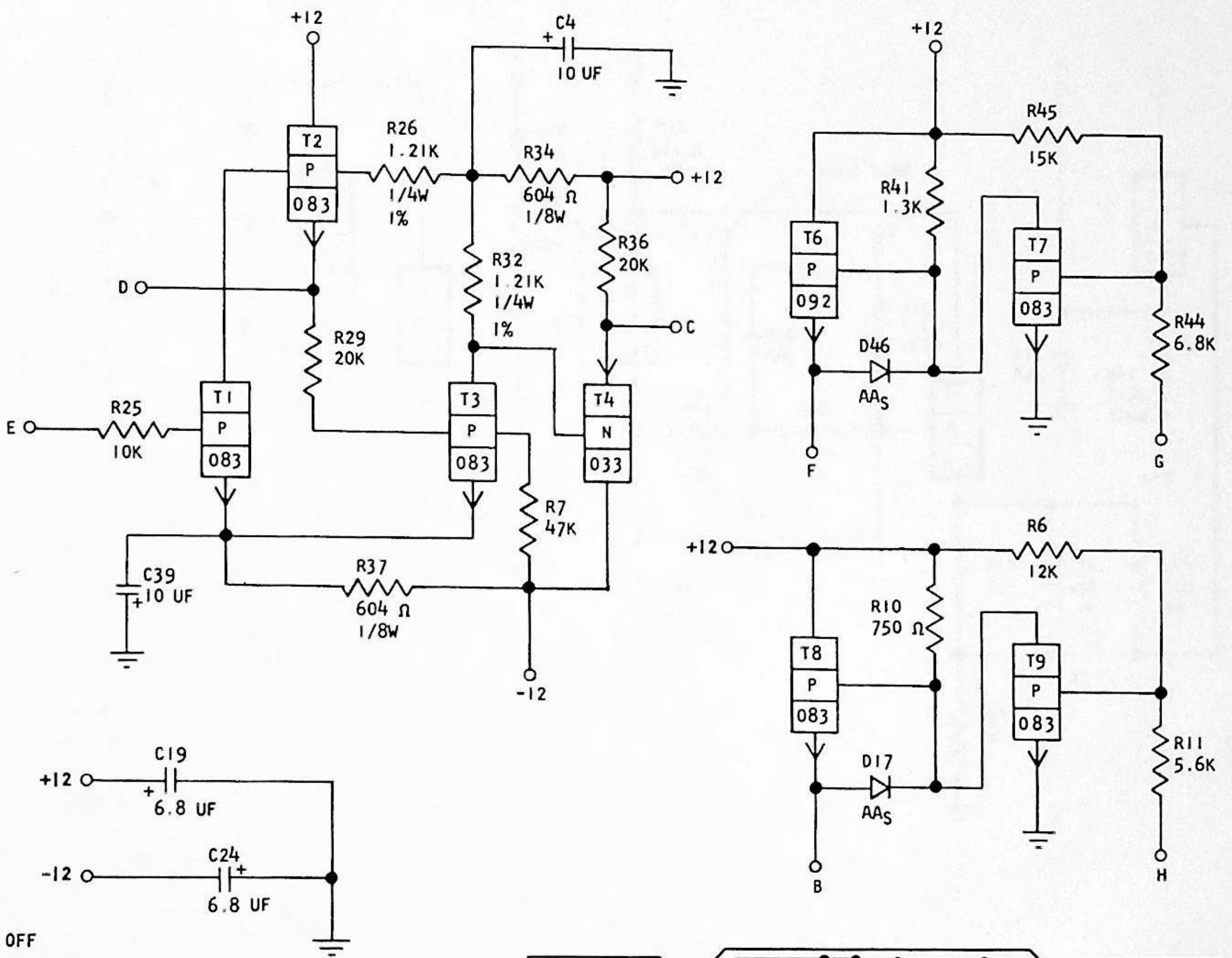
CARD CODE	729950
Y C B -	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370420

SENSE AMPLIFIER-SELECT GATE, READ GATE AND BAND PASS CTRL





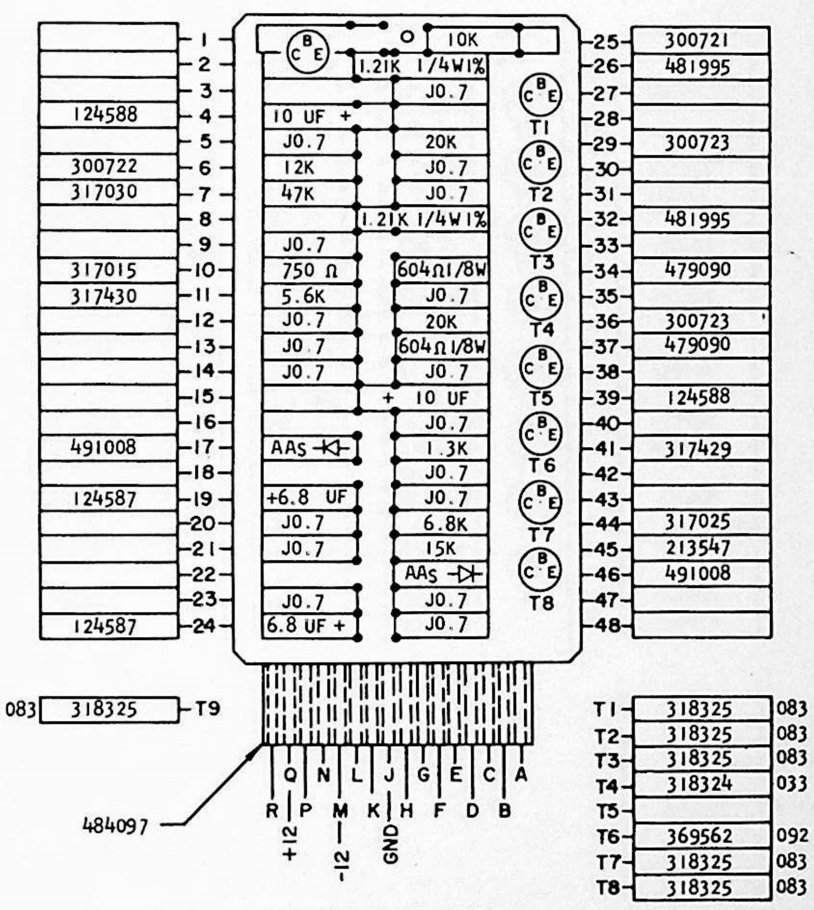
SEQUENCE OF OPERATION

A. SELECT GATE
1. WHEN INPUT AT PIN E IS UP, T1 IS ON, T2, T3, T4, ARE OFF THE OUTPUT IS UP AT PIN C AND DOWN AT PIN D
2. WHEN OUTPUT AT PIN E IS DOWN, T1 IS OFF, T2, T3, T4 ARE ON, THE OUTPUT IS DOWN AT PIN C AND UP AT PIN D

B. READ GATE
1. WHEN INPUT AT PIN G IS UP, T7 TURNS ON, T6 TURNS ON AN OUTPUT AT PIN F IS DOWN
2. WHEN INPUT AT PIN G IS DOWN, T7 IS OFF T6 IS ON, AND OUTPUT AT PIN F IS UP

C. NOISE REJECTION
1. WHEN INPUT AT H IS UP, T9 IS ON, T8 IS ON AND OUTPUT AT B IS DOWN
2. WHEN INPUT AT H IS DOWN, T9 IS OFF, T8 IS ON AND THE OUTPUT AT B IS UP

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
E	S	SELECT GATE INPUT		UP	-.5	-.1
				DOWN	-7.42	-12.48
C	S	SELECT GATE OUTPUT #1		UP	5.14	7.23
				DOWN	-4.43	-6.64
D	S	SELECT GATE OUTPUT #2		UP	4.52	6.88
				DOWN	-4.76	-6.84
G	S	READ GATE INPUT		UP	-.5	-.1
				DOWN	-6.87	-12.48
F	S	READ GATE OUTPUT		UP	+9.39	+12.48
				DOWN	+.7	0
H	S	NOISE REJECT INPUT		UP	-.5	-.1
				DOWN	-6.87	-12.48
B	S	NOISE REJECT OUTPUT		UP	10.41	12.48
				DOWN	.7	0



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-SEN AM-SEL				6-27-62	115599					729950
GT, RD GT AND BAND PASS CTRL										
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

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CARD CODE	729951
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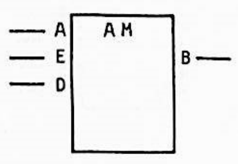
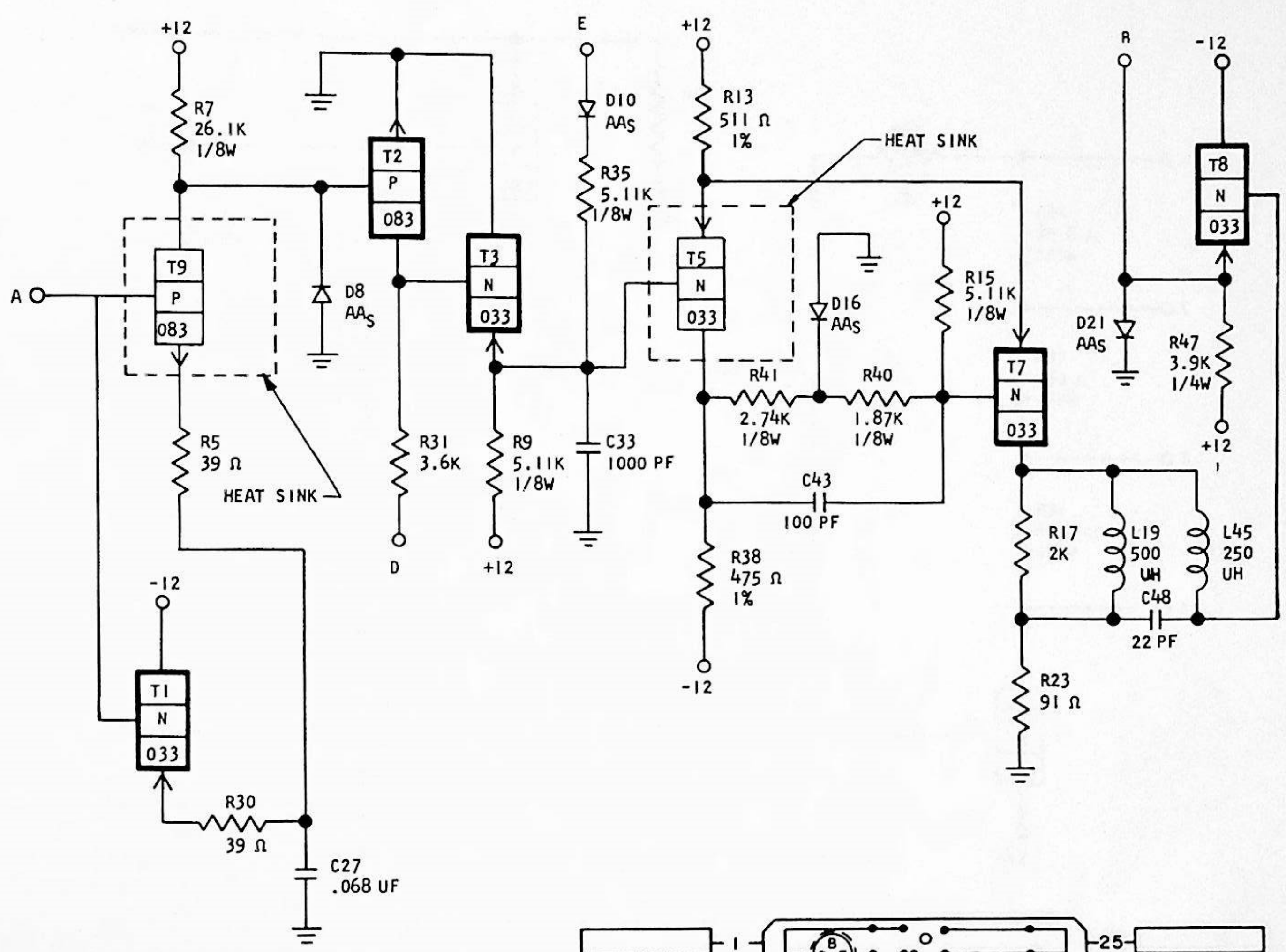
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370421

PEAK DETECTOR, INTEGRATOR & V.M. DRIVER



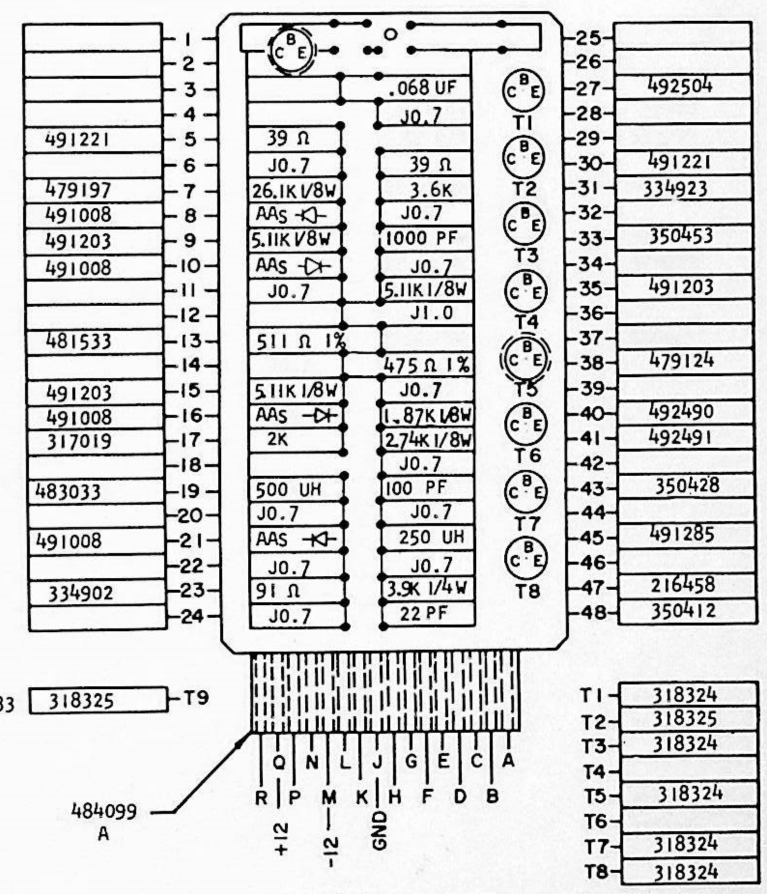


SEQUENCE OF OPERATION

1. THIS CIRCUIT IS USED TO SENSE A PEAK IN THE TAPE SIGNAL AFTER IT HAS BEEN AMPLIFIED BY THE TAPE PRE-AMPLIFIER. TRANSISTORS 1 AND 9 SENSE THE PEAK AND THIS SIGNAL IS AMPLIFIED BY T2 TO DRIVE T3 WHICH INTURN DRIVES THE INTEGRATOR AND THE SCHMITT TRIGGER. WHEN THE SCHMITT TRIGGER FIRES, THE FALL TRANSITION IS SHAPED INTO THE OUTPUT PULSE (-12V) AND THEN IT IS COUPLED TO THE LOAD BY T8, AN EMITTER FOLLOWER.
2. A READ CONTROL LINE IS USED TO GATE THE SIGNAL DURING SWITCHING BETWEEN READ AND READ-WHILE-WRITE CONDITIONS: PIN D. ANOTHER CONTROL LINE CHANGES THE NOISE REJECTION OF THE CIRCUIT DEPENDING UPON THE TYPE OF TAPE DRIVE WHICH IS USED: PIN E. FOR HIGH FREQUENCY OPERATION THE INPUT AT PIN E IS AT + 12 V. FOR LOW FREQUENCY OPERATION THE INPUT TO PIN E IS 0 V.

3. OUTPUT CAN DRIVE SDTDL OR SDTRL CIRCUITS.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A		INPUT		UP		9 PEAK
				DOWN		0
E		NOISE REJECTION GATE	HIGH FREQUENCY		+10.41	+12.48
			LOW FREQUENCY		0	+.7
B	S	OUTPUT		UP	0	+.4
				DOWN	-11.5	-13
D	Y	READ GATE		UP	+9.39	+12.48
				DOWN	0	+.7



☆ 083 | 318325 | T9

T1	318324	033
T2	318325	083
T3	318324	033
T4		
T5	318324	033☆
T6		
T7	318324	033
T8	318324	033

COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR - PEAK				4-?-62	115599					
DETECTOR INTEGRATOR & V.M. DRIVER										
DESIGN		MODEL	SMS							
DETAIL RQ	3-1-62	SCALE	NONE							
CHECK WH	3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729951

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CARD CODE	729952
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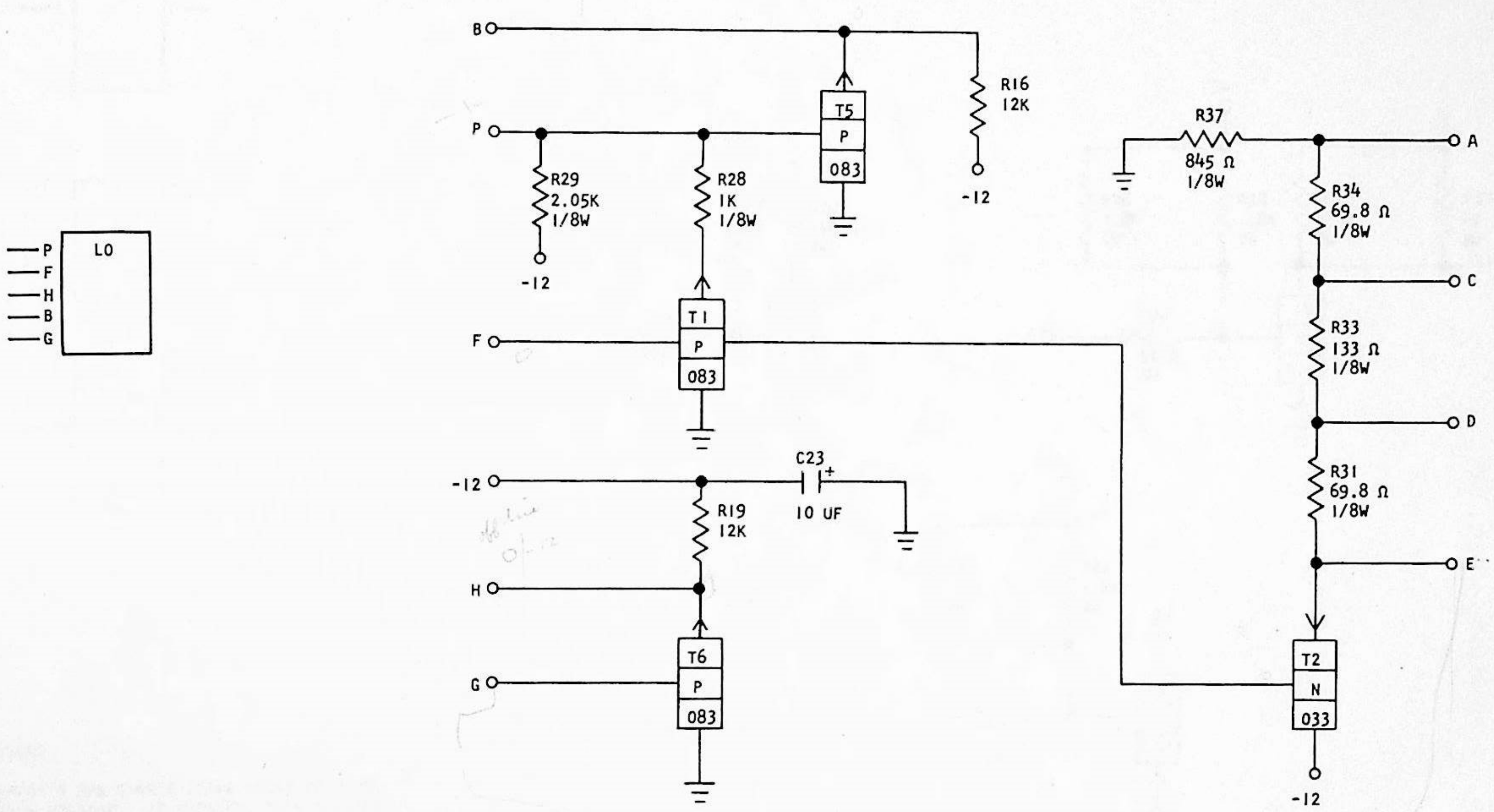
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370501

SENSE AMPLIFIER-CLIPPING LEVEL CONTROL



APPLICATION NOTES

HIGH ACCEPTANCE — READ WHILE WRITE CONDITION

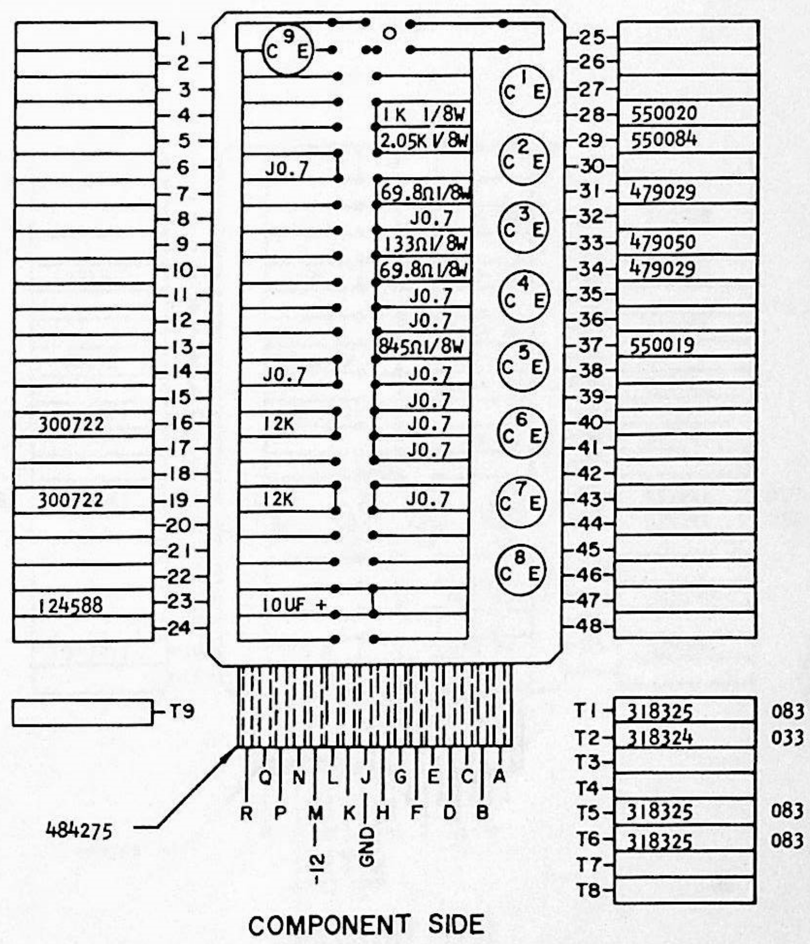
LOW SPEED TAPE
PIN F 0.0V, +S — PIN B -3.07V TO -5.09V
PIN P -12.5V

HIGH SPEED TAPE
PIN F 0.0V +S — PIN B -.2V TO -.5V
PIN P 0.0V

READ CONDITION

HIGH AND LOW SPEED DRIVES
PIN F -12V — PIN B -11.1V TO -12.5V

LOW ACCEPTANCE — PIN H 0.0V
PIN F 0.0 VOLTS — PIN H -8.03 TO -12.5 DEPENDS
PIN F -12 VOLTS — ON WHAT PIN (A,C,D,E) G IS TIED TO



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SENSE					6 -62	115599					
AMPLIFIER-CLIPPING LEVEL CONTROL												
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

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STANDARDS CODE

CARD CODE	729953
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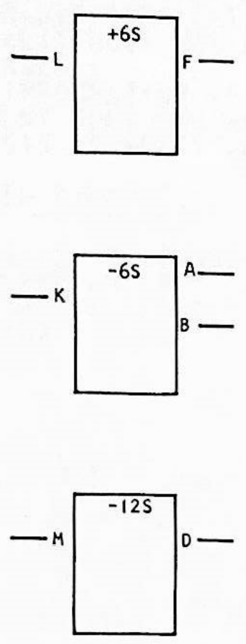
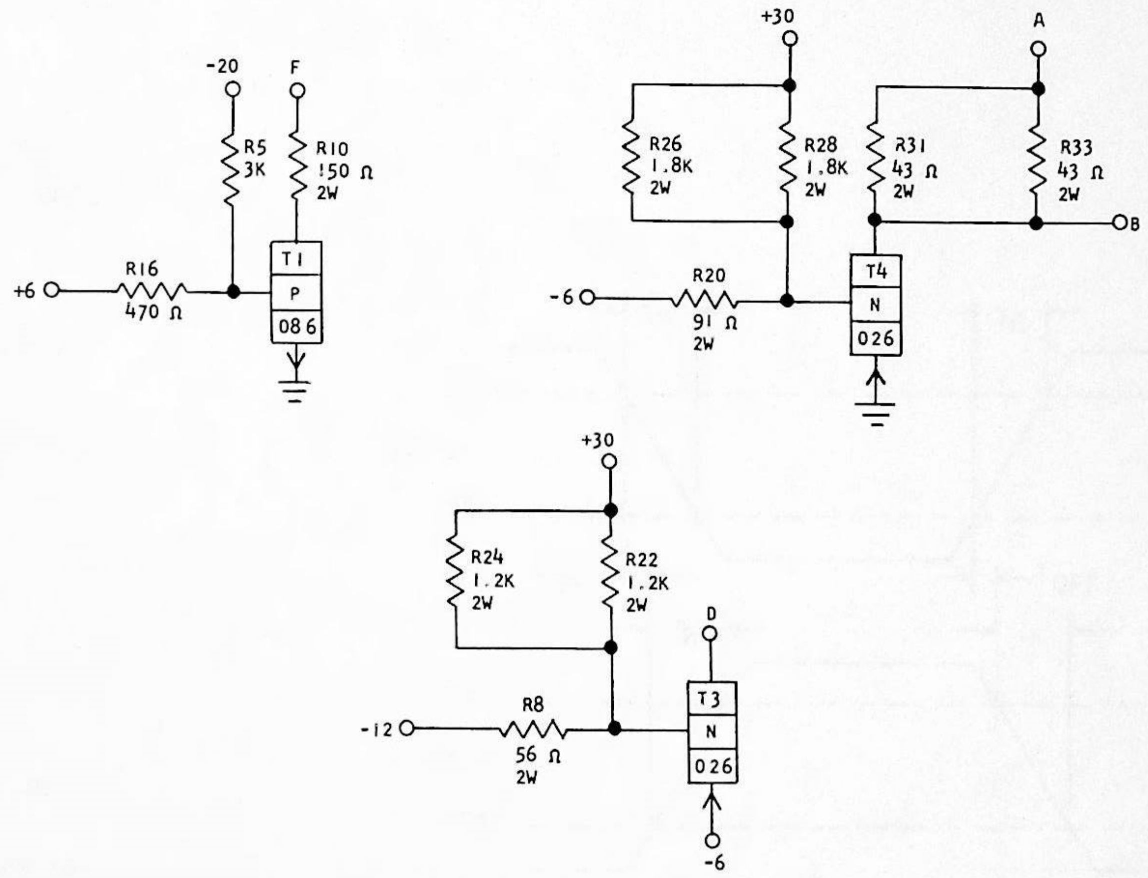
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370429

POWER SUPPLY SEQUENCING



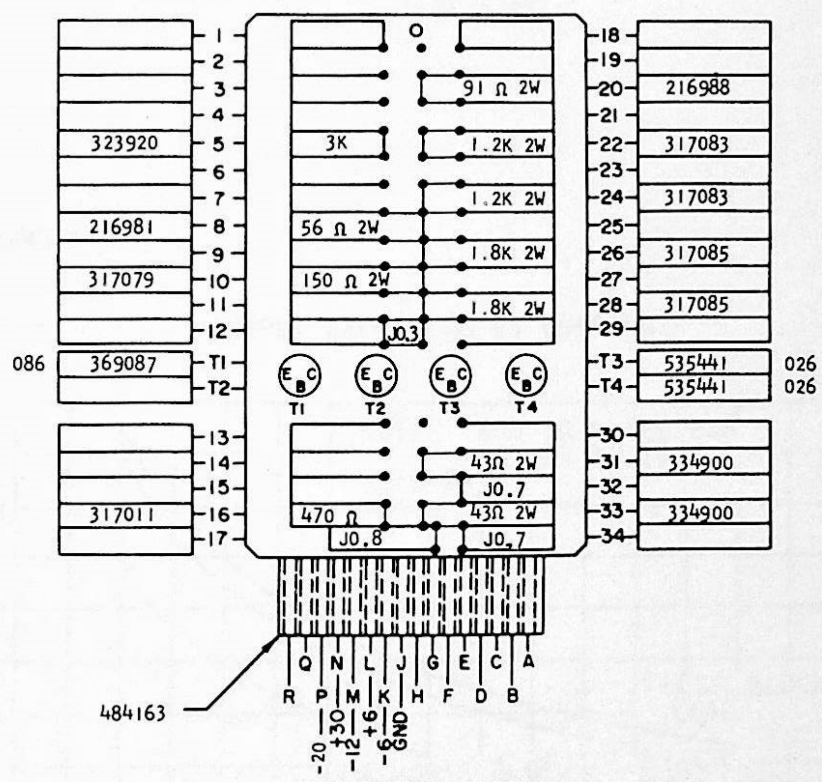


SEQUENCE OF OPERATIONS

1. THESE THREE CIRCUITS ARE SINGLE-STAGE RELAY DRIVERS, USED TO SENSE A GIVEN VOLTAGE. IF PRESENT, THIS VOLTAGE ALLOWS A TRANSISTOR TO CONDUCT AND OPERATE A RELAY IN THE COLLECTOR CIRCUIT. IF THIS VOLTAGE DROPS OUT DURING NORMAL OPERATIONS THE RELAY WILL ALSO DROP.

2. THE OUTPUT VOLTAGE LEVEL WHEN THE TRANSISTORS ARE OFF DEPENDS UPON THE RETURN VOLTAGE OF THE RELAY IN THE COLLECTOR CIRCUIT.

3. THE +6 VOLT SENSE (T1) MAY OPERATE A RELAY RETURNED TO NO MORE THAN 35 VOLTS, THE -6 VOLT SENSE (T4) 45 VOLTS, AND THE -12 VOLT SENSE (T3) 40 VOLTS.



COMPONENT SIDE

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
K	V	-6		UP	-1.1	+.24
				DOWN	-5.76	-6.24
B		OUTPUT	SEE NOTE 2	UP	-.24	+.24
				DOWN		
A		OUTPUT	SEE NOTE 2	UP	-.24	+.24
				DOWN		
L	V	+6		UP	+5.76	+6.24
				DOWN	+1.8	-.24
F		OUTPUT	SEE NOTE 2	UP		
				DOWN	+.24	-.24
M	V	-12		UP	-1.0	+.24
				DOWN	-11.52	-12.48
D		OUTPUT	SEE NOTE 2	UP	-6.24	-5.76
				DOWN		

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.

NAME	CARD ASM TSTR- POWER SUPPLY SEQUENCING			
DESIGN		MODEL	SMS	
DETAIL	RQ	3-1-62	SCALE	NONE
CHECK	WH	3-1-62	DRAW	LIG 3-17-62
APPRO			CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-11-62	115599					

729953

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SDTDL LOGIC FAMILY DELAY INFORMATION

GENERAL

THE TURN ON, TURN OFF DELAYS OF THE CIRCUITS USED IN A PARTICULAR MACHINE ARE COMPLEX FUNCTIONS OF MANY VARIABLES SUCH AS THE TRANSISTOR DELAY, INPUT-OUTPUT LOADING, FALL AND RISE TIME, ETC.

THE DELAY SPECIFICATIONS ARE GIVEN BELOW AND ARE CLASSIFIED BY CIRCUIT TYPE.

WHEN POSSIBLE, REPRESENTATIVE RANGES OF DELAYS ARE GIVEN ON EACH INDIVIDUAL CIRCUIT SHEET AND SHOULD BE USED AS A GUIDE. SPECIFIC CIRCUIT APPLICATION AND/OR CAPACITIVE LOAD (EXAMPLE: WIRE CAPACITANCE) MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES.

THE FOLLOWING INFORMATION IS PROVIDED FOR THOSE CASES WHERE CARD REPLACEMENT DOES NOT RESULT IN IMPROVEMENT AND A MORE DETAILED ANALYSIS IS NECESSARY.

HIGH SPEED, LOW SPEED CIRCUITS

THE SDTDL CIRCUITS ARE CLASSIFIED INTO TWO MAJOR FAMILIES, THE LOW SPEED AND THE HIGH SPEED CIRCUITS. THE DIFFERENCE BETWEEN THE TWO FAMILIES CONSISTS OF THE INPUT SPEED UP CAPACITOR THAT IS USED ONLY IN THE HIGH SPEED LOGIC BLOCKS.

DELAY CHARTS:

NUMEROUS CHARTS GIVING DELAY INFORMATION HAVE BEEN INCLUDED IN THIS DOCUMENT. BOTH MINIMUM AND MAXIMUM DELAYS ARE GIVEN AS A FUNCTION OF SOME VARIABLE OR VARIABLES. NOMINAL DELAYS HAVE BEEN AVOIDED DUE TO POSSIBLE MISINTERPRETATIONS. THE MAXIMUM DELAYS GIVEN ARE SLIGHTLY LESS THAN THE THEORETICAL MAXIMUM DELAY. THE MAXIMUM DELAYS GIVEN SHOULD NOT BE EXCEEDED IN PRACTICAL APPLICATIONS.

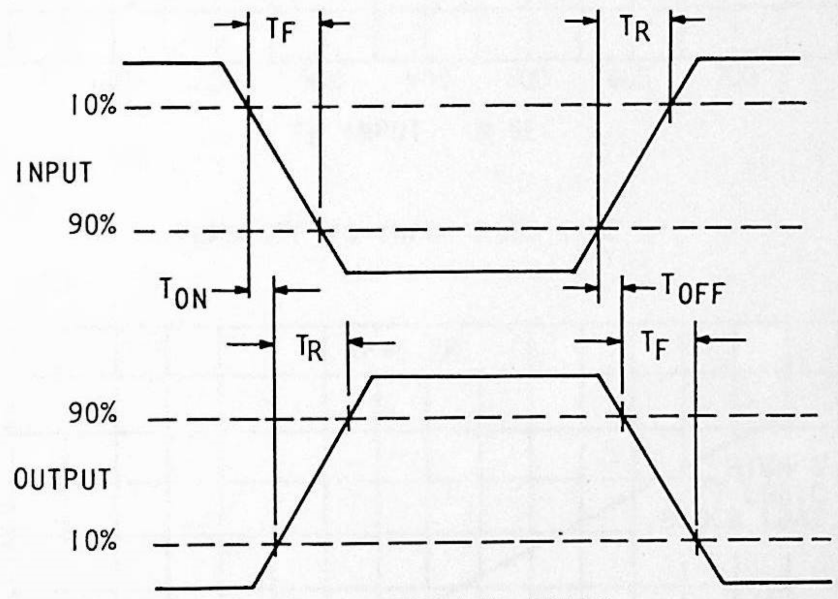
USE OF GRAPHS

THE FOLLOWING STEPS ARE RECOMMENDED FOR USING THE INFORMATION PROVIDED IN THE ACCOMPANYING GRAPHS.

1. GIVEN A LOAD CONFIGURATION REFER TO THE GRAPH OUTPUT FALL TIME VS. LOADING TO DETERMINE THE OUTPUT FALL TIME.
2. GIVEN THE INPUT FALL TIME, THE OUTPUT RISE IS DETERMINED FROM THE GRAPH OF OUTPUT RISE TIME VS. INPUT FALL TIME.
3. KNOWLEDGE OF THE RISE TIME AND USE OF THE GRAPH OF TURN-OFF DELAY VS. INPUT RISE TIME RESULTS IN TURN-OFF LIMITS.
4. KNOWLEDGE OF INPUT FALL TIME AND USE OF THE GRAPH OF TURN-ON DELAY VS. INPUT FALL TIME RESULTS IN TURN-ON LIMITS.

DEFINITIONS

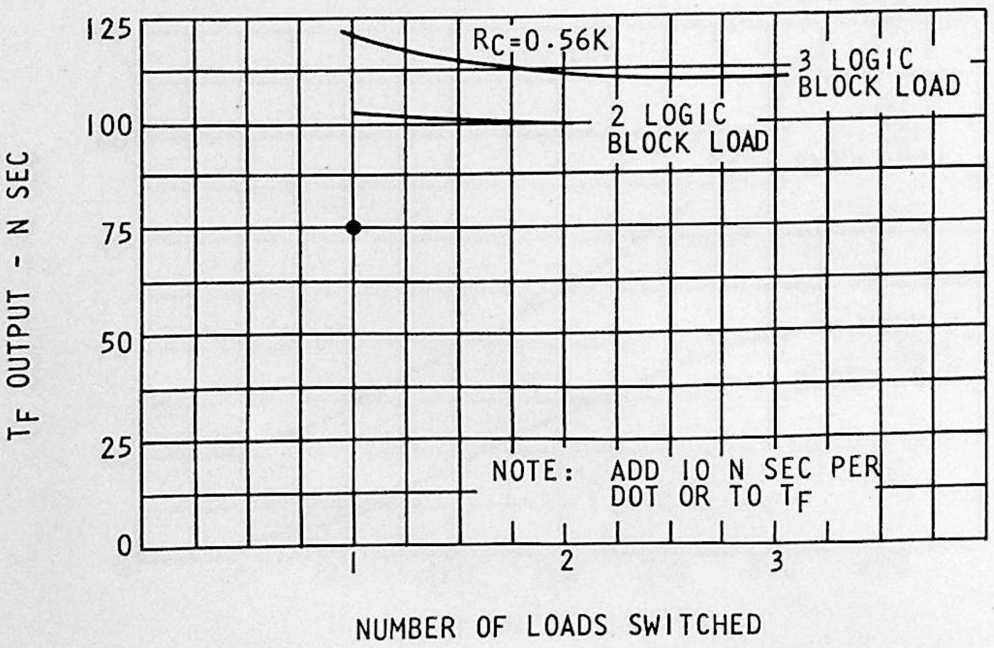
THE RISE AND FALL TIMES WERE MEASURED FROM THE 10% TO 90% POINTS OF THE INPUT AND OUTPUT WAVEFORM. THE TURN-ON DELAY WAS MEASURED AS THE TIME INTERVAL BETWEEN 10% DOWN AT THE INPUT TO 10% UP AT THE OUTPUT. THE TURN-OFF DELAY WAS MEASURED AS THE TIME INTERVAL BETWEEN 10% UP AT THE INPUT TO 10% DOWN AT THE OUTPUT. UNLESS OTHERWISE STATED THE RISE, FALL AND DELAY TIMES ARE GIVEN IN N SEC (NANOSECONDS).



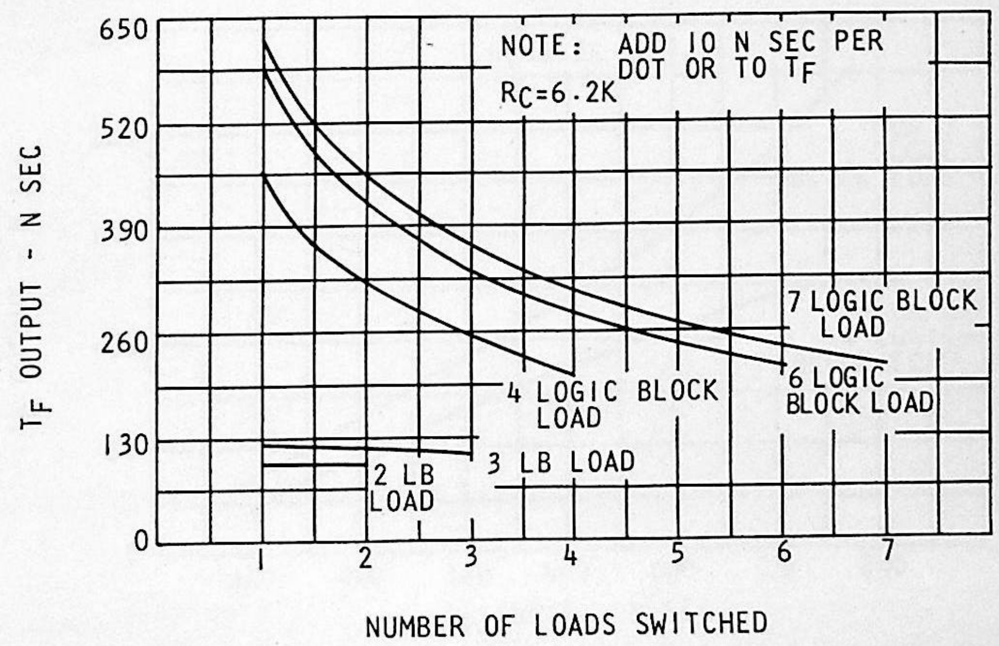
T_{ON} = TURN-ON DELAY
T_{OFF} = TURN-OFF DELAY
T_F = FALL TIME
T_R = RISE TIME

HIGH SPEED SINGLE LEVEL LOGIC BLOCK

OUTPUT FALL TIME VS LOADING



OUTPUT FALL TIME VS LOADING



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.			DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL LOGIC DELAY INFO. - REF DWG		6-29-62	115599					
DESIGN		MODEL							
DETAIL	WH 3-1-62	SCALE							
CHECK	RQ 3-1-62	DRAW							
APPRO		CHECK							

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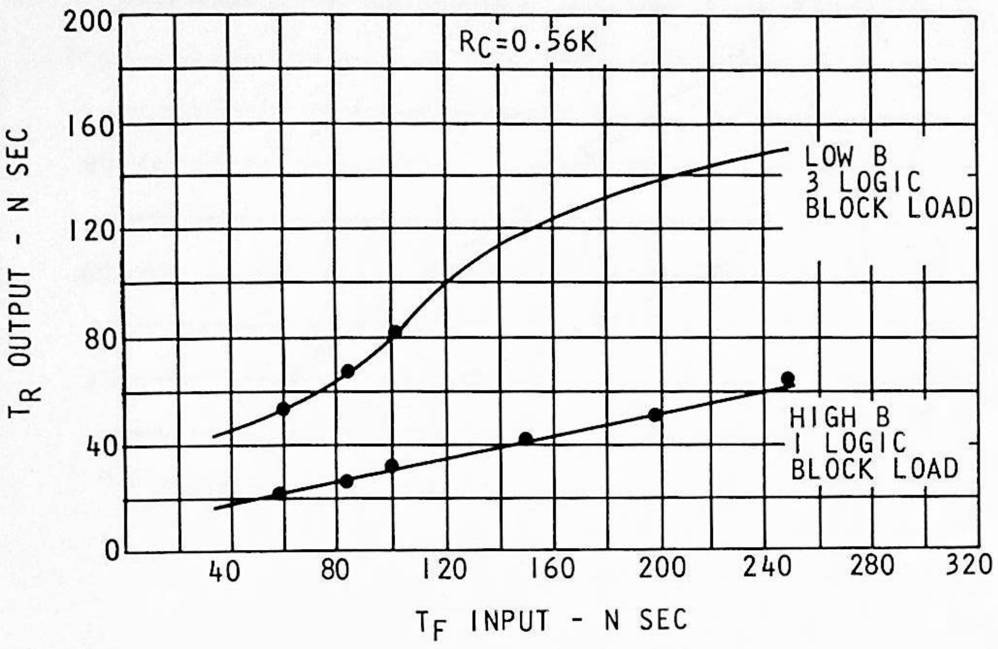
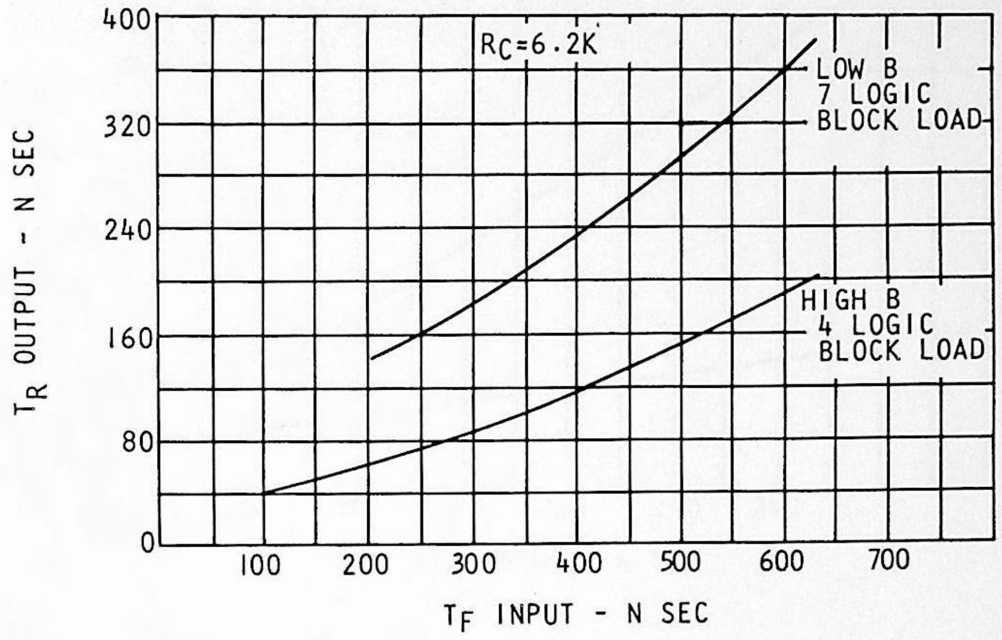
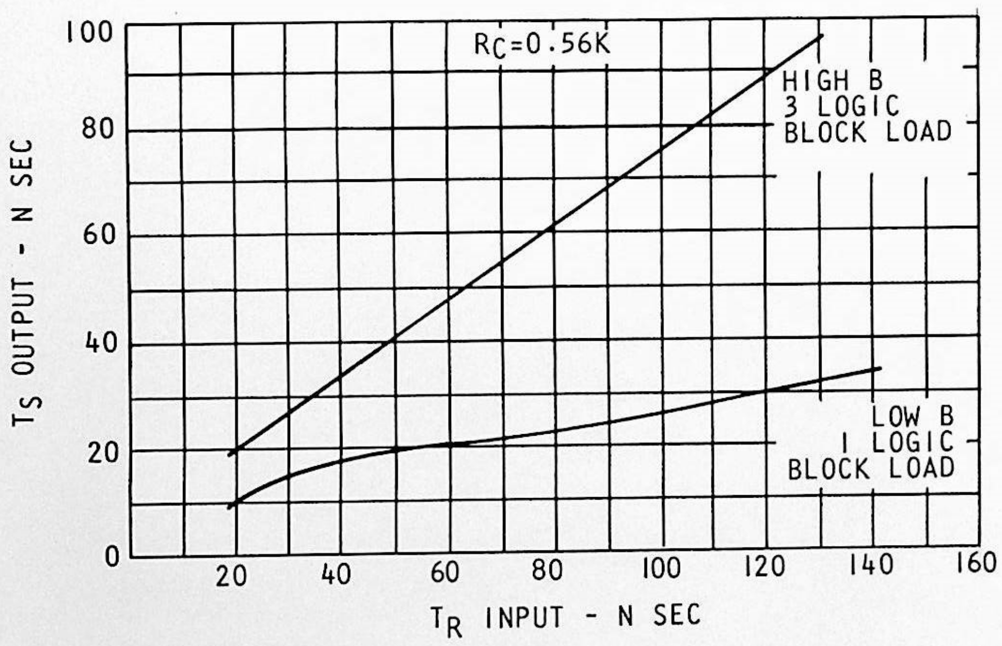
OUTPUT RISE TIME VS INPUT FALL TIME



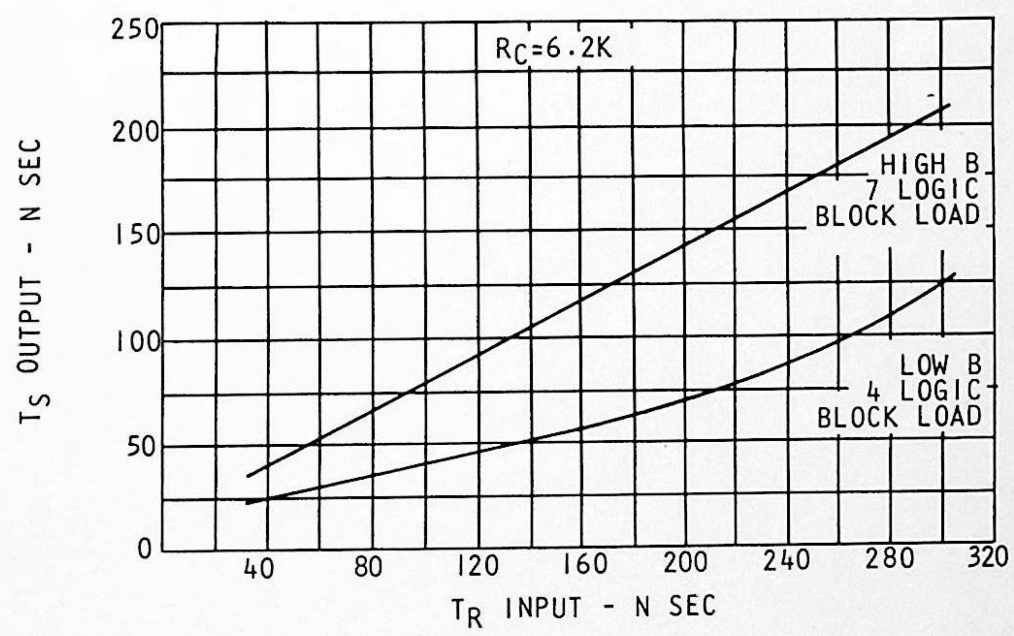
OUTPUT RISE TIME VS INPUT FALL TIME



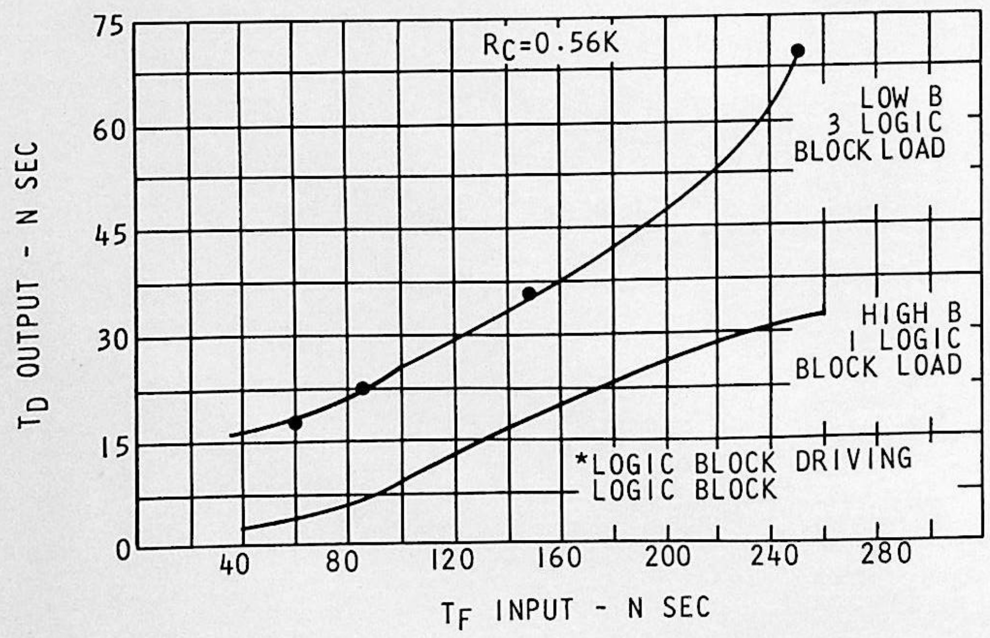
TURN-OFF VS INPUT RISE TIME



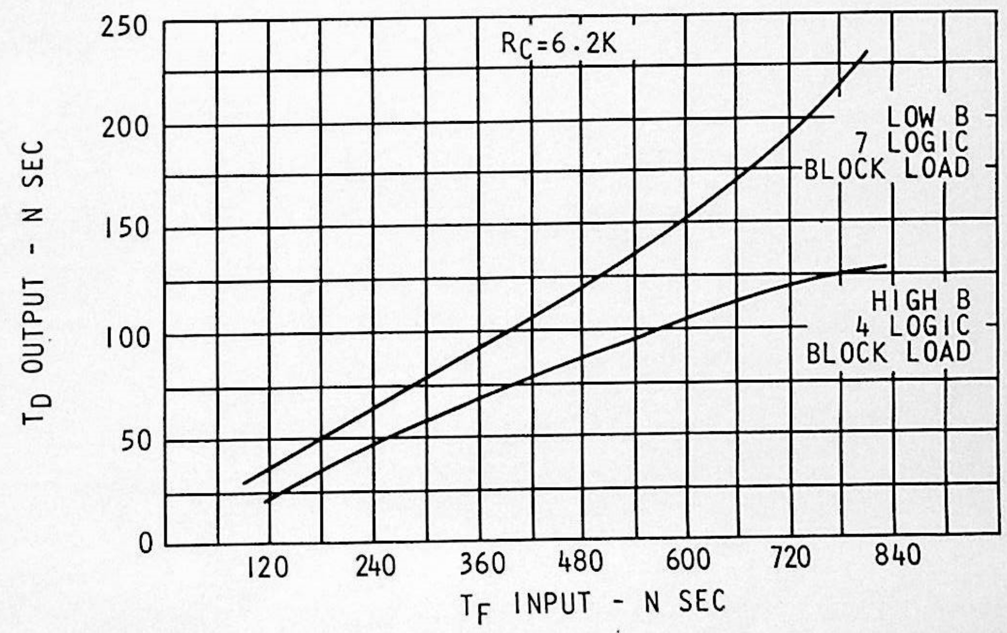
TURN-OFF VS INPUT RISE TIME



TURN-ON VS INPUT FALL TIME*



TURN-ON VS INPUT FALL TIME



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL LOGIC DELAY INFO. - REF DWG					6-29-62	115599					
DESIGN			MODEL									
DETAIL	WH	3-1-62	SCALE									
CHECK	RQ	3-1-62	DRAW									
APPRO			CHECK									

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STANDARDS CODE

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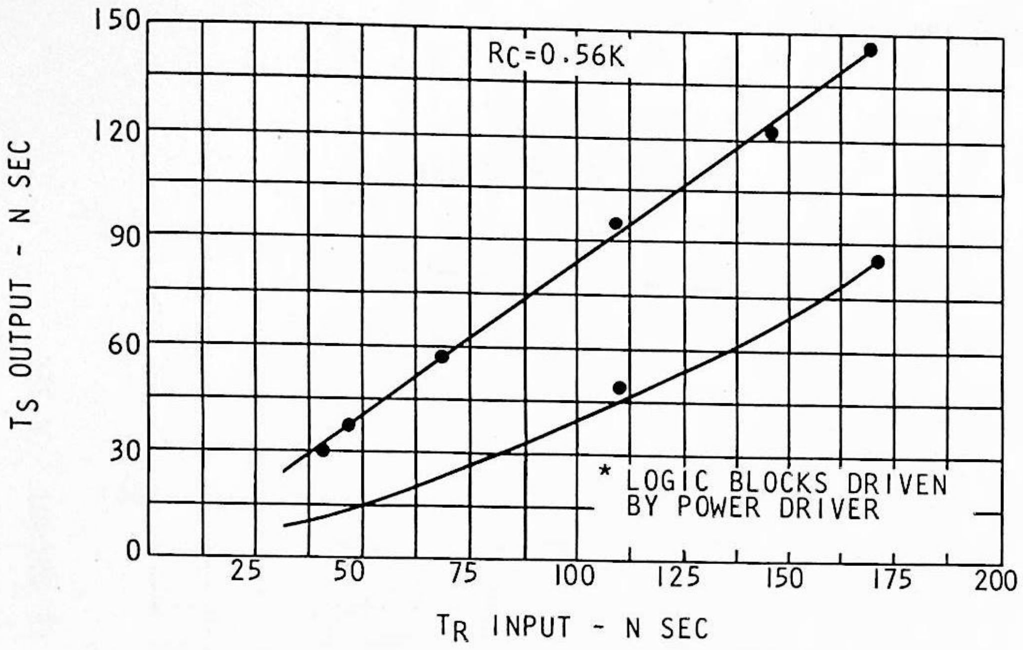
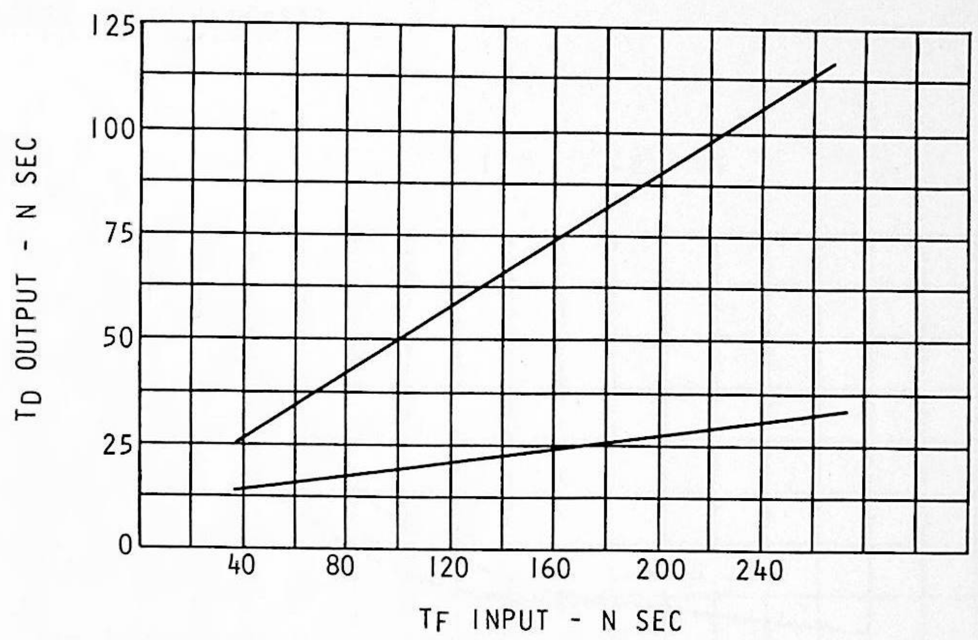
CARD CODE	729954

TURN-OFF VS RISE TIME INPUT*



TURN-ON VS FALL TIME INPUT (LOGIC BLOCK DRIVEN BY POWER DRIVERS)



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL LOGIC DELAY				6-29-62	115599					
I NFO. - REF. DWG.											
DESIGN			MODEL								
DETAIL	WH	3-1-62	SCALE								
CHECK	RQ	3-1-62	DRAW								
APPRO			CHECK								

729954

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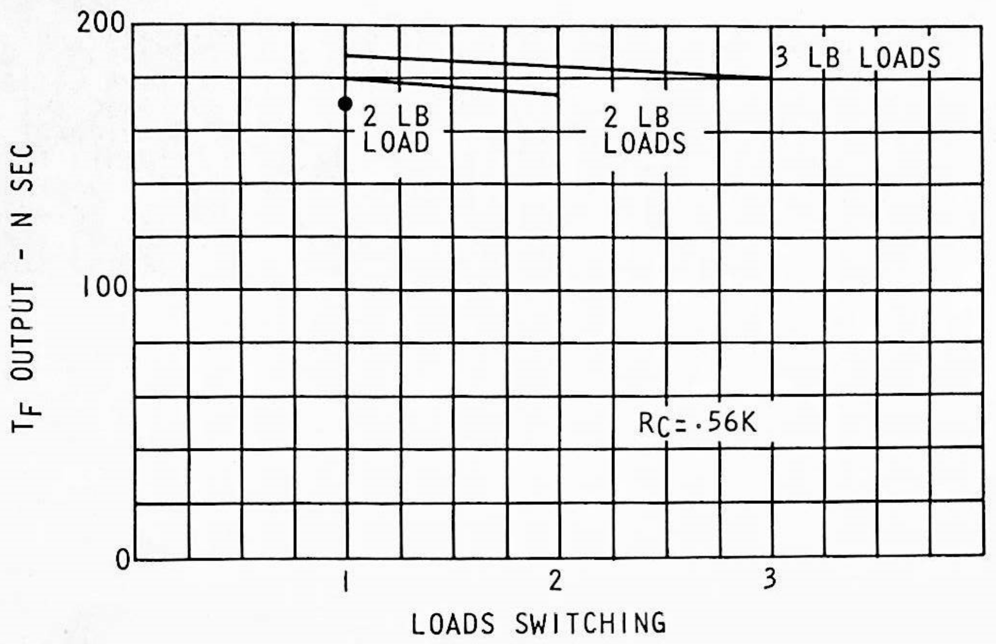
LIG 6-4-62

C. B. CO., NO. 574W 43088

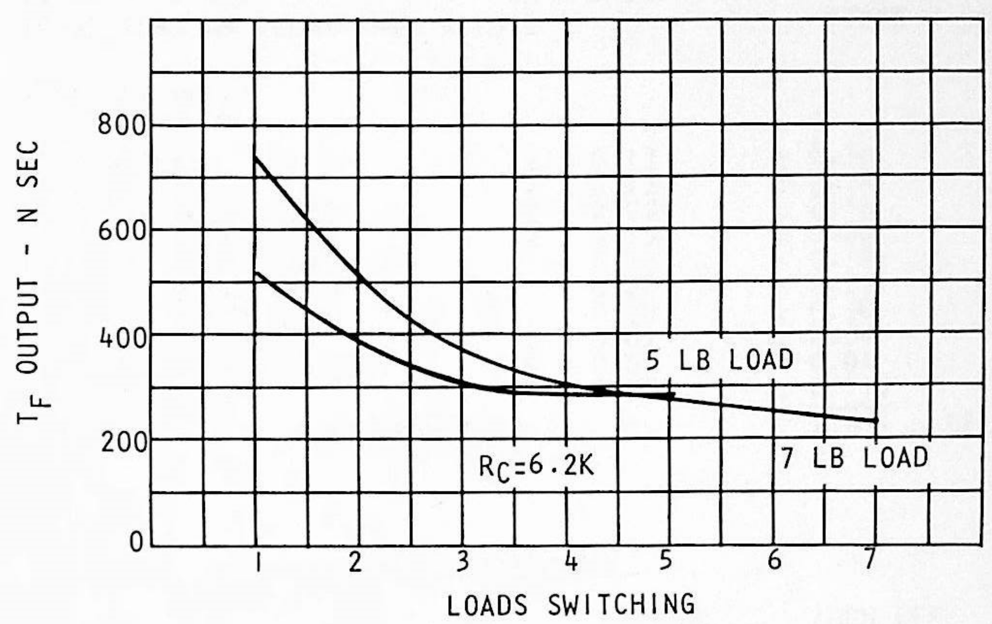
FORM 02-001

LOW SPEED SINGLE LEVEL LOGIC BLOCKS

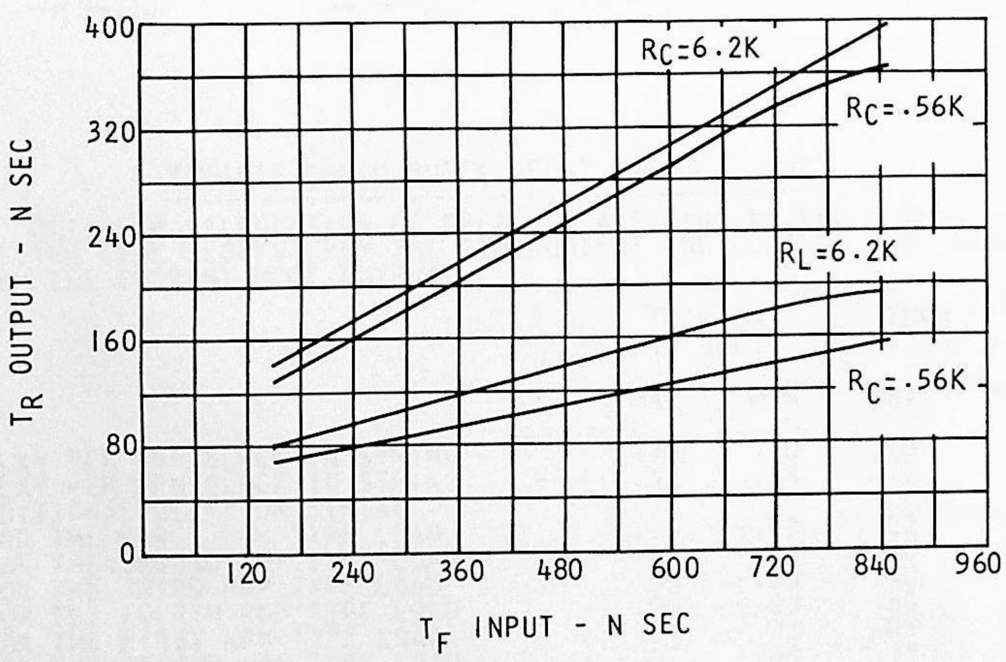
FALL TIME VS LOADING



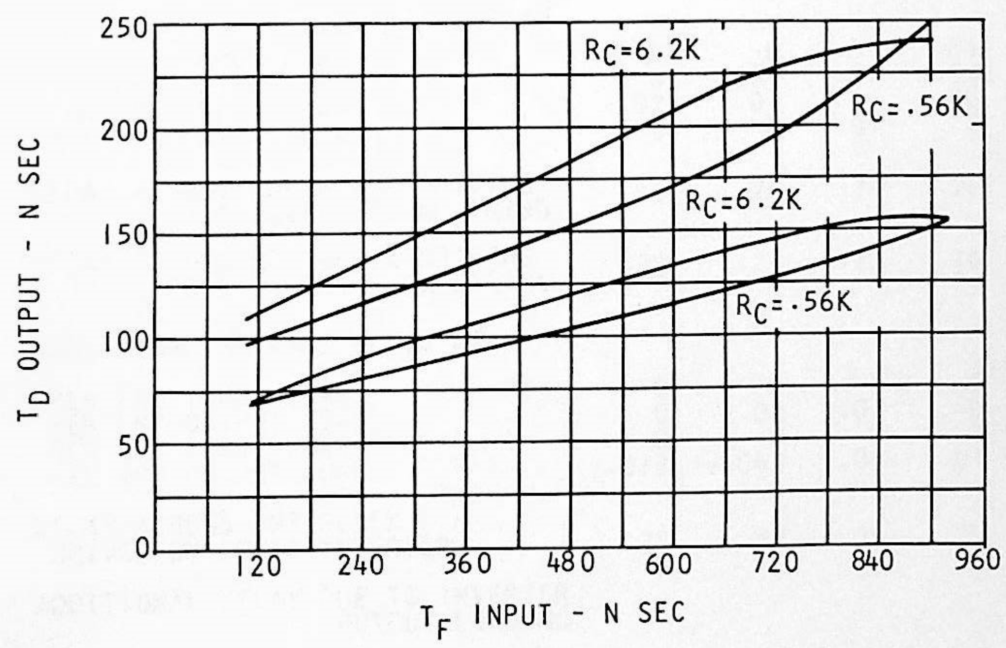
FALL TIME VS LOADING



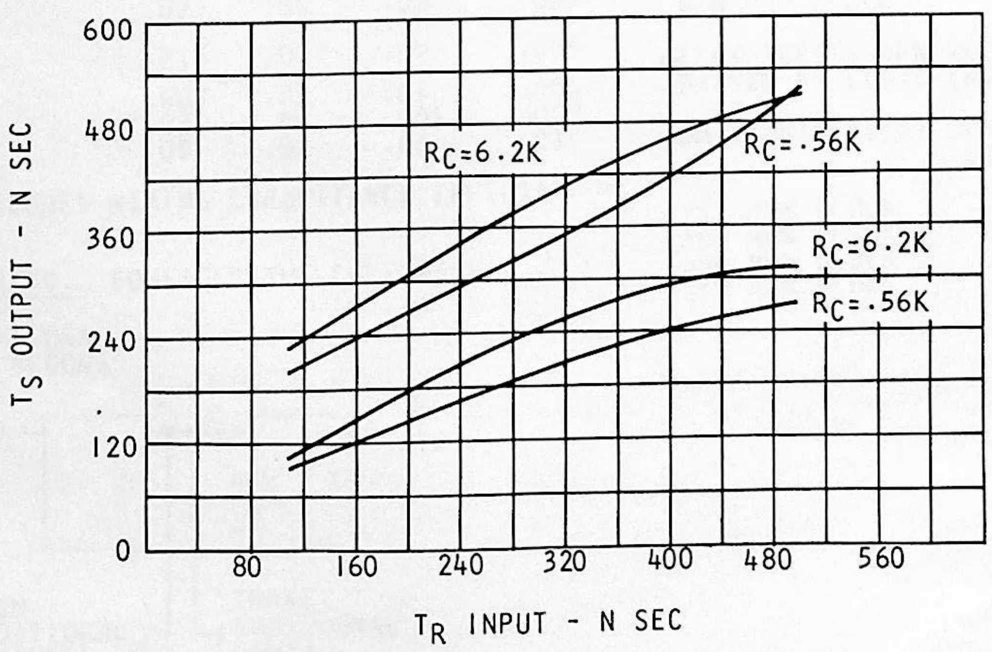
OUTPUT RISE TIME VS INPUT FALL TIME



TURN-OFF VS INPUT FALL TIME



TURN-OFF VS INPUT RISE TIME



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL LOGIC DELAY			·62	115599					729954
INFO. - REF DWG										
DESIGN			MODEL							
DETAIL	WH	3-1-62	SCALE							
CHECK	RQ	3-1-62	DRAW							
APPRO			CHECK							

C

LIG 6-4-62

STANDARDS CODE

729955

CTDL DELAY INFORMATION

CARD CODE 729955

SHEET 1 OF 3

GENERAL

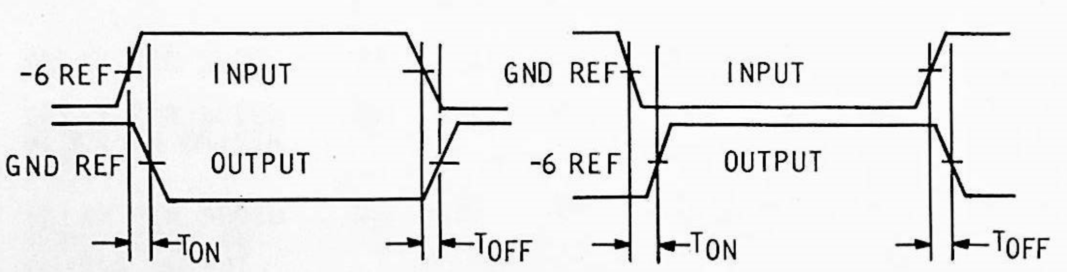
THE TURN ON, TURN OFF DELAYS OF THE CIRCUITS USED IN A PARTICULAR MACHINE ARE COMPLEX FUNCTIONS OF MANY VARIABLES SUCH AS THE TRANSISTOR DELAY, INPUT-OUTPUT LOADING, FALL AND RISE TIME, ETC.

THE DELAY SPECIFICATIONS ARE GIVEN BELOW AND ARE CLASSIFIED BY CIRCUIT TYPE.

WHEN POSSIBLE, REPRESENTATIVE RANGES OF DELAY ARE GIVEN ON EACH INDIVIDUAL CIRCUIT SHEET AND SHOULD BE USED AS A GUIDE. SPECIFIC CIRCUIT APPLICATION AND/OR CAPACITIVE LOAD (EXAMPLE: WIRE CAPACITANCE) MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES.

THE FOLLOWING INFORMATION IS PROVIDED FOR THOSE CASES WHERE CARD REPLACEMENT DOES NOT RESULT IN IMPROVEMENT AND A MORE DETAILED ANALYSIS IS NECESSARY.

THE DELAY OF THE SIGNAL IN THE CTDL BLOCKS IS A FUNCTION OF THE TRANSISTOR DELAYS PLUS THE LOADING EFFECTS OF THE INPUT AND OUTPUT CIRCUITS. DELAYS FOR SEVERAL STAGES IN CASCADE ARE NUMERICALLY EQUAL TO THE SUM OF INDIVIDUAL STAGES. UNLESS OTHERWISE STATED, DELAYS ARE MEASURED FROM THE TIME THE INPUT SIGNAL CROSSES ITS REFERENCE VOLTAGE TO THE TIME THE OUTPUT SIGNAL CROSSES ITS REFERENCE VOLTAGE, AS SHOWN.



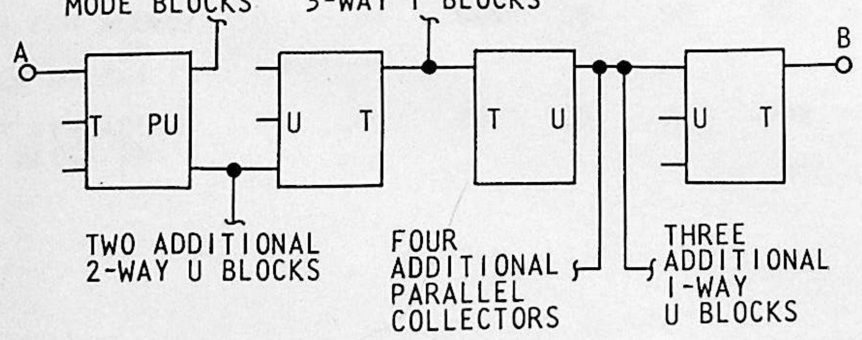
BASIC LOGIC BLOCK DELAY INFORMATION

DATA FOR CALCULATION OF DELAY IN A STRING OF LOGIC WHEN DRIVING CTDL BLOCKS FROM THE CTDL OUTPUT AND CURRENT MODE BLOCKS FROM THE CURRENT MODE OUTPUT.

	TURN ON (U SEC)		TURN OFF (U SEC)	
	MAX	MIN	MAX	MIN
DELAY PER PNP BLOCK IN STRING	.70	.20	.18	.06
DELAY PER NPN BLOCK IN STRING	.52	.18	.12	.05
ADDITIONAL DELAY ON STRING				
FOR THE FIRST PNP TYPE LOAD	.00	-.03	.22	.06
FOR THE SECOND PNP TYPE LOAD	.00	-.03	.30	.07
FOR THE THIRD PNP TYPE LOAD	.00	-.03	.40	.08
FOR THE FOURTH PNP TYPE LOAD	.00	-.03	.50	.10
FOR THE FIRST NPN TYPE LOAD	-.01	-.03	.09	.01
FOR THE SECOND NPN TYPE LOAD	-.01	-.03	.13	.02.
FOR THE THIRD NPN TYPE LOAD	-.01	-.03	.18	.03
FOR THE FOURTH NPN TYPE LOAD	-.01	-.03	.22	.04
DELAY PER PNP TYPE CS LOADS ON STRING	.02	.00	.02	.005
DELAY PER NPN TYPE CS LOADS ON STRING	.015	.00	.02	.005
DELAY PER PARALLEL COLLECTOR	.007	.00	.01	.004
DELAY PER DIODE INPUT	*.02	.00	.005	.000
DELAY PER 100 PF	.05	.02	.06	.03

* WIRES ASSUMED ON GATES -- INCLUDES WIRING CAPACITANCE EFFECT BETWEEN ADJACENT CARDS.

EXAMPLE OF CTDL DELAY LOGIC STRING. CONSIDER THE FOLLOWING LOGIC STRING:



IN THIS EXAMPLE ALL MAXIMUM DELAYS WILL BE USED:

TURN ON DELAY

2 T BLOCKS	2 X 0.7	= 1.4
2 U BLOCKS	2 X 0.52	= 1.04
5 ADDITIONAL U BLOCKS	5 X(-0.01)	= -0.05
2 ADDITIONAL T BLOCKS	0	0
2 P-TYPE CS BLOCK	2 X 0.015	= 0.03
4 PARALLEL COLLECTORS	4 X 0.007	= 0.028
23 INPUT DIODES	23 X 0.02	= 0.46
TOTAL TURN ON DELAY FROM A TO B		2.908 U SEC

TURN OFF DELAY

2 T BLOCKS	2 X 0.18	= 0.36
2 U BLOCKS	2 X 0.12	= 0.24
2 1ST U BLOCK LOAD	2 X 0.09	= 0.18
2 2ND U BLOCK LOAD	2 X 0.13	= 0.26
1 3RD U BLOCK LOAD	0.18	= 0.18
1 1ST T BLOCK LOAD	0.22	= 0.22
1 2ND T BLOCK LOAD	0.30	= 0.30
2 P-TYPE CS BLOCK	2 X 0.02	= 0.04
4 PARALLEL COLLECTORS	4 X 0.01	= 0.04
23 INPUT DIODES	23 X 0.005	= 0.115
TOTAL TURN OFF DELAY FROM A TO B		1.935 U SEC

LOGIC INVERTER

	TURN ON (U SEC)		TURN OFF (U SEC)	
	MAX	MIN	MAX	MIN
DELAY PER PNP INVERTER IN STRING	-.08	-.14	.55	.06
DELAY PER NPN INVERTER IN STRING	0	-.06	.41	-.02
ADDER LOGIC INVERTER DELAY:				
PER PNP INPUT LOAD	0	0	.015	.01
PER PNP OUTPUT LOAD	0	-.005	.01	.006
PER NPN INPUT LOAD	-.02	-.01	.04	.02
PER NPN OUTPUT LOAD	0	0	.01	0
DELAY ACROSS PNP BLOCK DRIVING LOGIC INVERTER IN STRING	.81	.26	.30	.26
DELAY ACROSS NPN BLOCK DRIVING LOGIC INVERTER IN STRING	.38	.28	.20	.14
ADDITIONAL DRIVING BLOCK DELAY				
PER PNP INPUT LOAD	0	0	0	0
PER PNP OUTPUT LOAD	0	-.02	.01	0
PER NPN INPUT LOAD	0	0	0	0
PER NPN OUTPUT LOAD	-.013	-.043	.01	.01
DELAY ACROSS PNP BLOCK DRIVEN BY LOGIC INVERTER	.74	.32	.22	.20
ADDITIONAL DELAY DUE TO INVERTER OUTPUT LOADING				
1ST PNP BLOCK	0	0	.16	.07
2ND PNP BLOCK	0	-.02	.22	.08
3RD PNP BLOCK	0	-.02	.33	.09
4TH PNP BLOCK	0	-.01	.39	.11
DELAY ACROSS NPN BLOCK DRIVEN BY LOGIC INVERTER	.35	.28	.17	.09
ADDITIONAL DELAY DUE TO INVERTER OUTPUT LOADING				
1ST NPN BLOCK	-.02	-.02	.18	.08
2ND NPN BLOCK	-.01	-.01	.21	.10
3RD NPN BLOCK	-.01	-.02	.22	.10
4TH NPN BLOCK	-.01	-.02	.42	.15

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CTDL DELAY INFO. REF. DWG.			7-19-62	115599					729955
DESIGN		MODEL								
DETAIL	WH 3-1-62	SCALE								
CHECK	RQ 3-1-62	DRAW								
APPRO		CHECK								

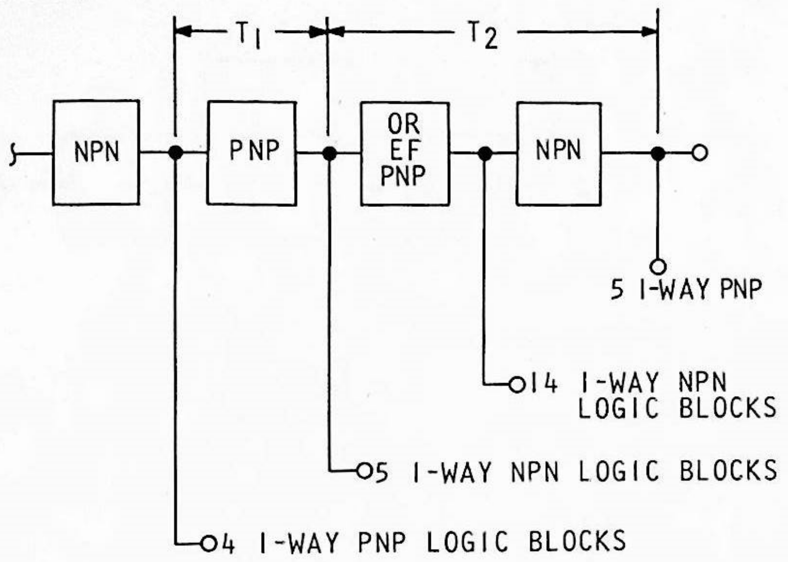
C

LIG 6-4-62

E, F "OR" CIRCUITS

DELAY INFORMATION

TEST CIRCUIT



PNP EMITTER "OR" DELAY (U SEC)

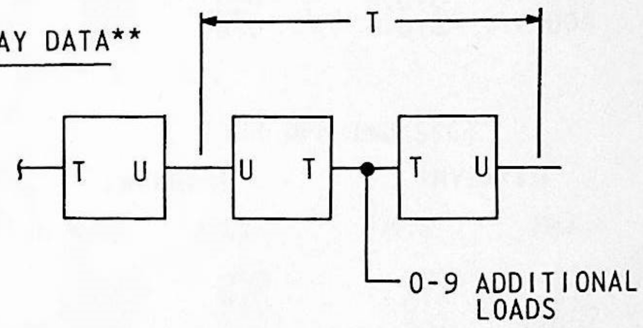
	T_1				T_2			
	T_{ON}		T_{OFF}		T_{ON}		T_{OFF}	
	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.
DELAY PER BLOCK	.92	.28	.15	.10	.50	.12	.12	.12
DELAY PER ADDED BLOCK ON DRIVER INPUT	.00	.00	.06	.03	.00	.01	.02	.00
DELAY PER ADDED CTDL BLOCK ON DRIVER OUTPUT	.00	-.01	.00	.00	.01	-.02	.04	.06
DELAY PER ADDED CTDL BLOCK ON E.F.	.01	-.008	.00	.00	.00	-.01	.006	.01
DELAY PER ADDED CTDL BLOCK ON DRIVER BLOCK	.01	.00	.00	.00	-.03	-.01	.00	.00
DELAY W/3 E.F. ON DRIVER - NO LOAD R IN DRIVER	.29	.28	.30	.10	.50	.25	.24	.12
DELAY PER ADDED E.F.	.00	-.02	.02	.00	.00	.00	-.01	.00
DELAY PER ADDED CTDL BLOCK ON DRIVER INPUT	.00	-.01	.02	.00	.00	-.005	-.005	.00
DELAY PER ADDED BLOCK ON E.F. OUTPUT	.00	.002	.002	.00	.00	-.01	.015	.00
DELAY PER ADDED BLOCK ON DRIVER BLOCK	.00	.00	.004	.00	.00	-.02	.00	.00

NPN EMITTER "OR" DELAY (U SEC)

	T_1				T_2			
	T_{ON}		T_{OFF}		T_{ON}		T_{OFF}	
	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.
DELAY PER BLOCK	.42	.36	.15	.14	.70	.19	.10	.06
DELAY PER ADDED BLOCK ON DRIVER	-.02	.01	.05	.08	.00	.00	.01	.02
DELAY PER ADDED CTDL BLOCK ON DRIVER OUTPUT	-.01	-.01	.005	.00	.00	.00	.03	.01
DELAY PER ADDED CTDL BLOCK ON E.F.	.00	.00	.00	.00	.00	.002	.005	.005
DELAY PER ADDED CTDL BLOCK ON DRIVER BLOCK	.00	.00	.00	.00	-.04	.00	.00	.00
DELAY W/3 E.F. ON DRIVER - NO LOAD R IN DRIVER	.32	.36	.15	.14	.70	.20	.16	.06
DELAY PER ADDED E.F.	.02	.00	-.02	.00	.00	.00	.00	.00
DELAY PER ADDED CTDL BLOCK ON DRIVER INPUT	.00	-.02	.02	.00	.00	.00	.01	.00
DELAY PER ADDED BLOCK ON E.F. OUTPUT	.005	.00	.00	.00	-.005	.00	.01	.00
DELAY PER ADDED BLOCK ON DRIVER BLOCK	.01	.00	.00	.00	-.01	-.00	.00	.00

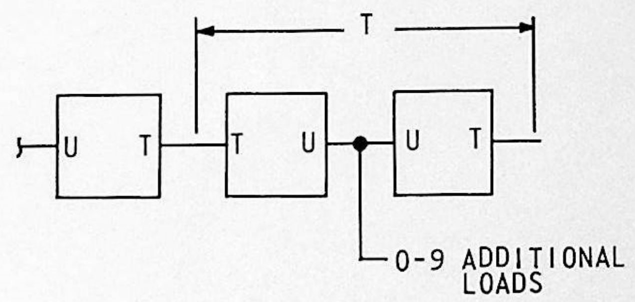
TRANSLATE BLOCK DELAY DATA

NPN BLOCK



TOTAL NUMBER OF LOADS	TURN ON (U SEC) MAX.	TURN ON (U SEC) MIN.	TURN OFF (U SEC) MAX.	TURN OFF (U SEC) MIN.
1	.70	.16	.34	.12
2	.70	.16	.36	.13
3	.70	.16	.40	.14
4	.70	.17	.43	.15
5	.70	.17	.46	.16
6	.70	.18	.48	.17
7	.70	.18	.50	.18
8	.70	.18	.51	.19
9	.70	.19	.57	.20
10	.70	.20	.60	.21

PNP BLOCK



TOTAL NUMBER OF LOADS	TURN ON (U SEC) MAX.	TURN ON (U SEC) MIN.	TURN OFF (U SEC) MAX.	TURN OFF (U SEC) MIN.
1	.52	.17	.26	.14
2	.52	.17	.31	.16
3	.52	.17	.35	.17
4	.52	.18	.38	.19
5	.53	.18	.41	.20
6	.53	.18	.44	.21
7	.53	.19	.47	.22
8	.53	.19	.50	.23
9	.53	.19	.54	.24
10	.53	.20	.56	.25

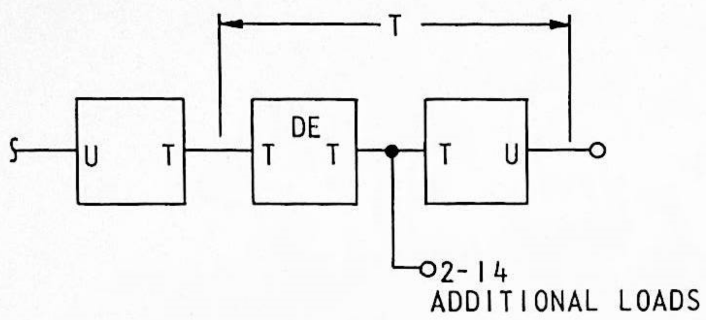
CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CTDL DELAY INFO. REF. DOC.			1-?-62	115599					729955
DESIGN		MODEL								
DETAIL	WH 3-1-62	SCALE								
CHECK	RQ 3-1-62	DRAW								
APPRO		CHECK								

C

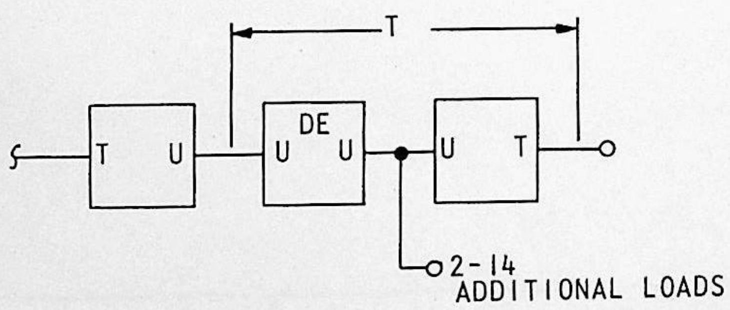
EMITTER FOLLOWER DELAY

NPN



TOTAL NUMBER OF LOADS	TURN ON (U SEC) MAX.	TURN ON (U SEC) MIN.	TURN OFF (U SEC) MAX.	TURN OFF (U SEC) MIN.
3	.68	.14	.25	.05
4	.68	.15	.26	.06
5	.68	.16	.27	.06
6	.68	.17	.27	.07
7	.68	.18	.29	.07
8	.68	.19	.30	.08
9	.68	.20	.31	.08
10	.68	.21	.32	.08
11	.68	.21	.33	.08
12	.68	.21	.34	.08
13	.68	.22	.35	.09
14	.68	.22	.36	.09
15	.68	.23	.37	.09

PNP



TOTAL NUMBER OF LOADS	TURN ON (U SEC) MAX.	TURN ON (U SEC) MIN.	TURN OFF (U SEC) MAX.	TURN OFF (U SEC) MIN.
3	.48	.18	.17	.06
4	.50	.19	.18	.06
5	.52	.20	.19	.07
6	.54	.21	.21	.07
7	.56	.22	.22	.08
8	.58	.23	.23	.08
9	.59	.24	.24	.09
10	.59	.24	.26	.09
11	.60	.25	.28	.09
12	.60	.26	.29	.10
13	.61	.26	.30	.10
14	.61	.27	.31	.10
15	.62	.27	.33	.10

CURRENT MODE BLOCK WITH CTDL COUPLING NETWORK

DELAY DATA

TURN ON (U SEC)

	IN PHASE MIN	IN PHASE MAX	INVERTED MIN	INVERTED MAX
BASIC N BLOCK DELAY	.100	.100	.150	.200
PER CTDL BLOCK LOAD	-.010	-.005	-.020	-.005
PER ADDED FAN-IN DIODE	-.002	-.002	-.001	-.001
BASIC P BLOCK DELAY	.080	.110	.210	.240
PER CTDL BLOCK LOAD	.000	.010	-.020	-.005
PER ADDED FAN-IN DIODE	-.001	-.001	-.002	-.002
BASIC CTDL PNP DELAY	.230	.560	.200	.500
PER CTDL BLOCK LOAD	.000	.020	.000	.020
PER ADDED FAN-IN DIODE	-.020	-.020	-.022	-.012
BASIC CTDL NPN DELAY	.200	.450	.180	.400
PER CTDL BLOCK LOAD	.020	.020	-.010	-.010
PER ADDED FAN-IN DIODE	.015	.030	-.018	-.006

TURN OFF (MU SEC)

	IN PHASE MIN	IN PHASE MAX	INVERTED MIN	INVERTED MAX
BASIC N BLOCK DELAY	.090	.090	.090	.130
PER CTDL BLOCK LOAD	.010	.010	.010	.010
PER ADDED FAN-IN DIODE	.001	.001	.001	.001
BASIC P BLOCK DELAY	.060	.130	.100	.120
PER CTDL BLOCK LOAD	.000	.020	.010	.010
PER ADDED FAN-IN DIODE	.002	.002	-.001	-.001
BASIC CTDL PNP DELAY	.060	.340	.140	.350
PER CTDL BLOCK LOAD	.020	.100	.000	.100
PER ADDED FAN-IN DIODE	.002	.021	.012	.020
BASIC CTDL NPN DELAY	.160	.220	.140	.170
PER CTDL BLOCK LOAD	.100	.260	.060	.290
PER ADDED FAN-IN DIODE	.005	.010	.005	.010

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.
NAME CTDL DELAY
INFO. -- REF. DWG

DESIGN		
DETAIL	WH	3-1-62
CHECK	RQ	3-1-62
APPRO		

MODEL
SCALE
DRAW
CHECK

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
6-29-62	115599					

729955

C

STANDARDS CODE

729956

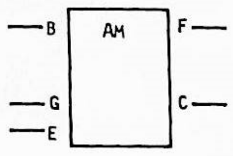
CARD CODE	729956
A S U -	

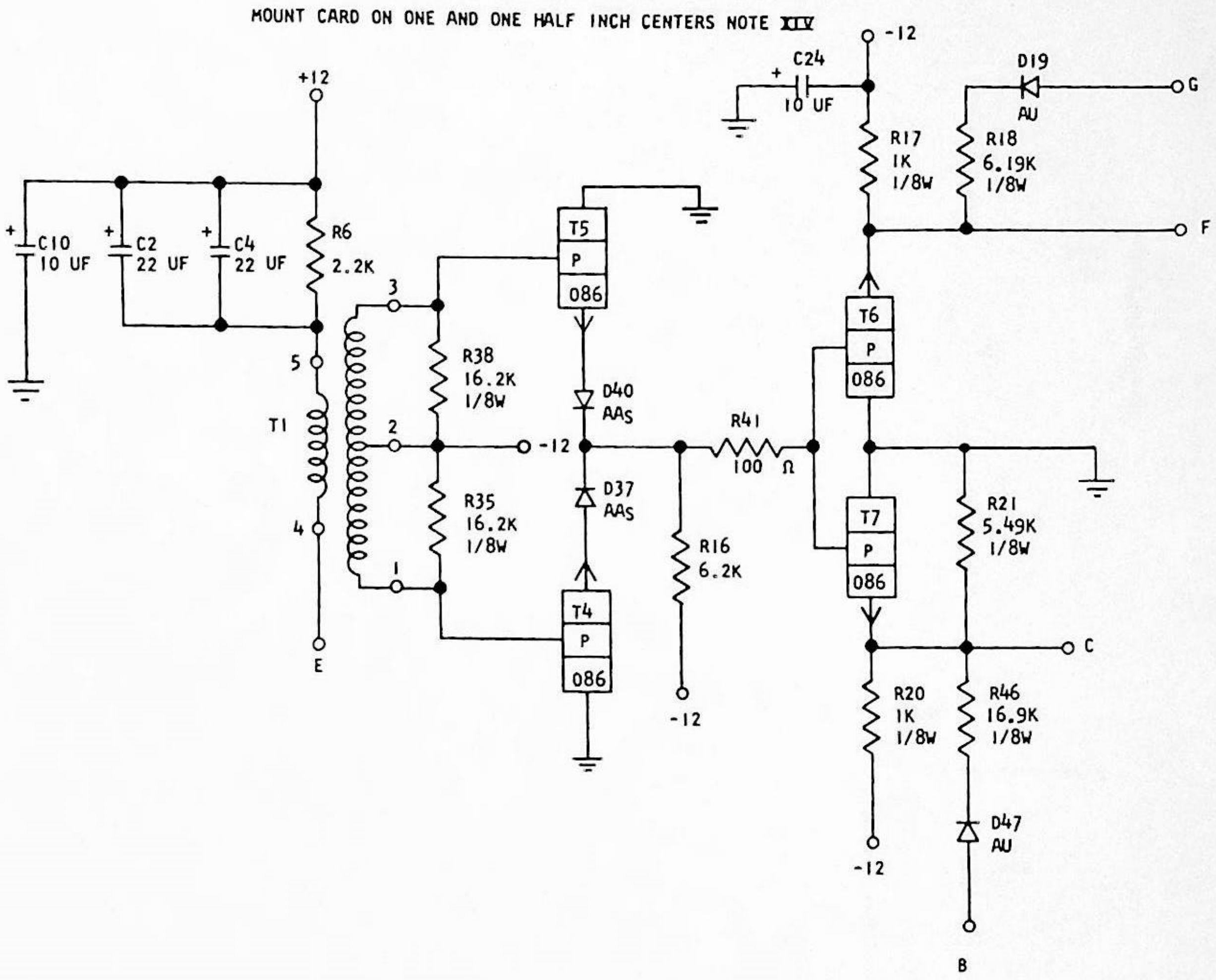
REFERENCE DRAWING

SEE PRODUCTION DRAWING 372285

SENSE AMPLIFIER-RECTIFIER AND CLIPPER

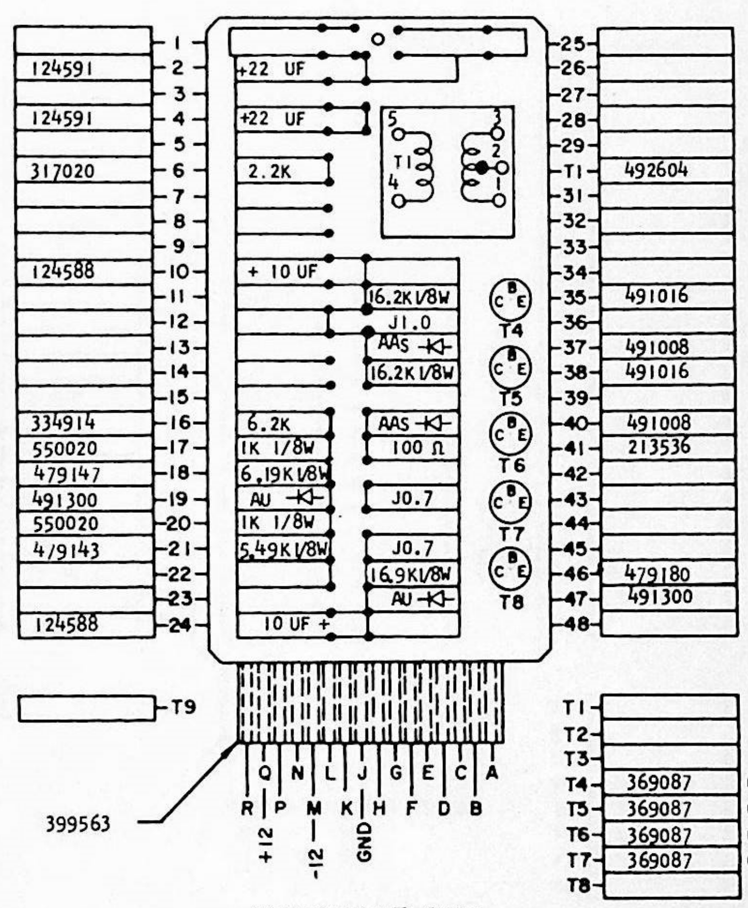
MOUNT CARD ON ONE AND ONE HALF INCH CENTERS NOTE XIV



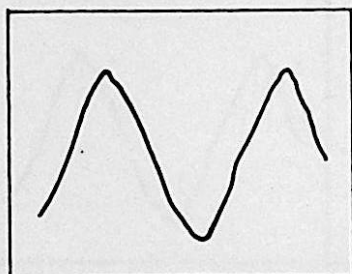
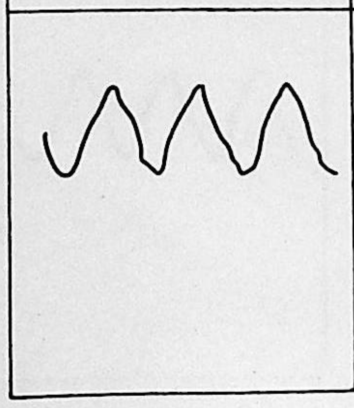


APPLICATION NOTES

VOLTAGES AT PIN G AND B FROM CLIPPING CARD



COMPONENT SIDE

	INPUT WAVE FORM AT PIN E 8.0VP-P NOMINAL 11.5VP-P MAXIMUM REFERENCE LEVEL +1.59V TO -3.88V
	OUTPUT WAVE FORM AT PIN C OR F 1. LOW ACCEPTANCE CHANNEL 0V TO 13V P-P READ CONDITIONS 0V TO 11.1V P-P READ WHILE WRITE CONDITIONS 2. HIGH ACCEPTANCE CHANNEL 0V TO 10.7V P-P READ CONDITIONS 0V TO 11.5V P-P READ WHILE WRITE CONDITION

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				
NAME	CARD ASM TSTR - SENSE AMPLIFIER-RECTIFIER AND CLIPPER			
DESIGN			MODEL	SMS
DETAIL	RQ	3-1-62	SCALE	NONE
CHECK	WH	3-1-62	DRAW	LIG 3-17-62
APPRO			CHECK	

DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
4 - 62	115599					729956

C

STANDARDS CODE

729957

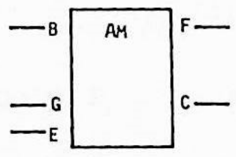
CARD CODE	729957
D Z A -	

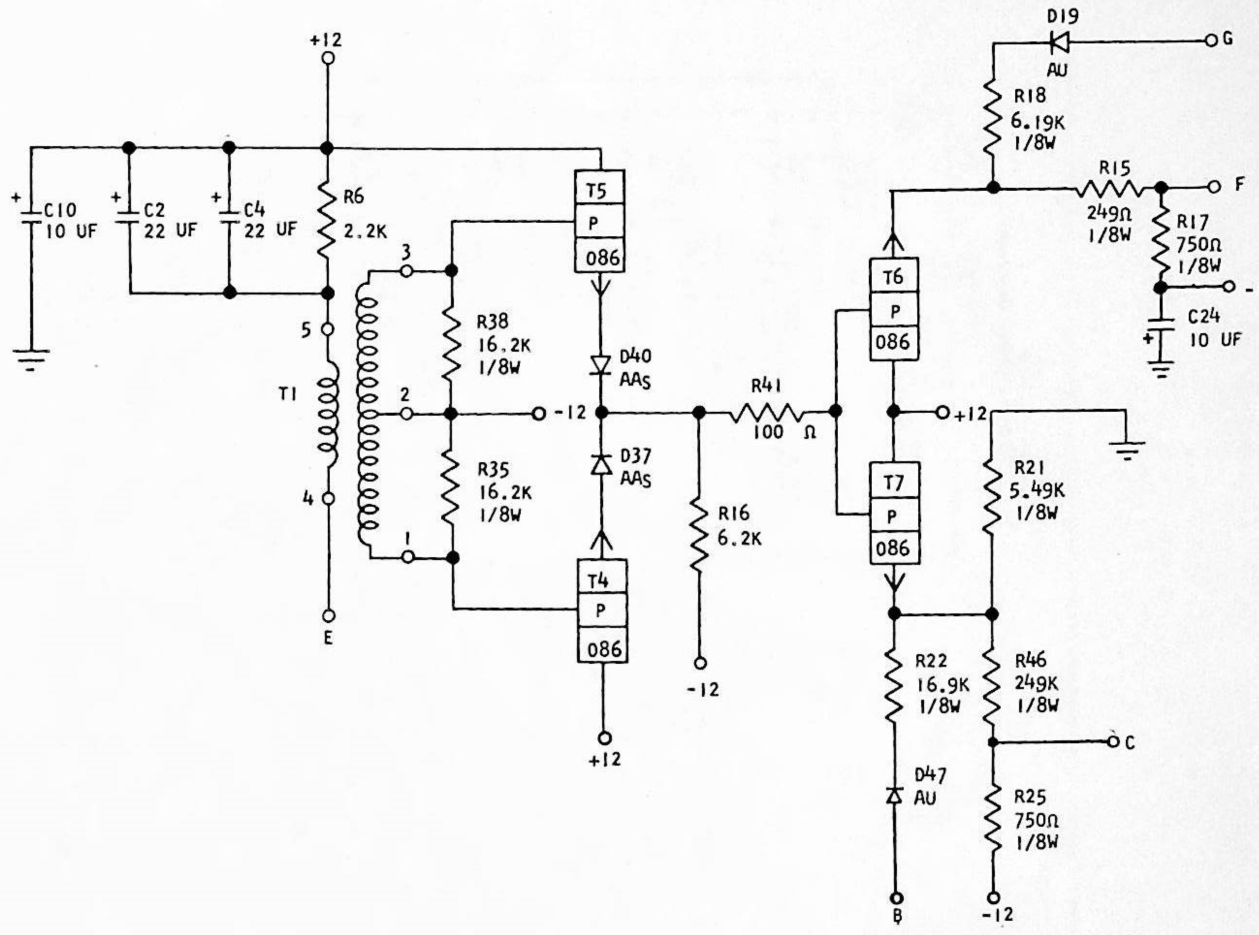
REFERENCE DRAWING

SEE PRODUCTION DRAWING 372359

SENSE AMPLIFIER-RECTIFIER AND CLIPPER

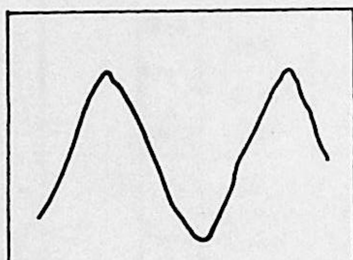
MOUNT CARD ON ONE AND ONE HALF INCH CENTERS NOTE XIV

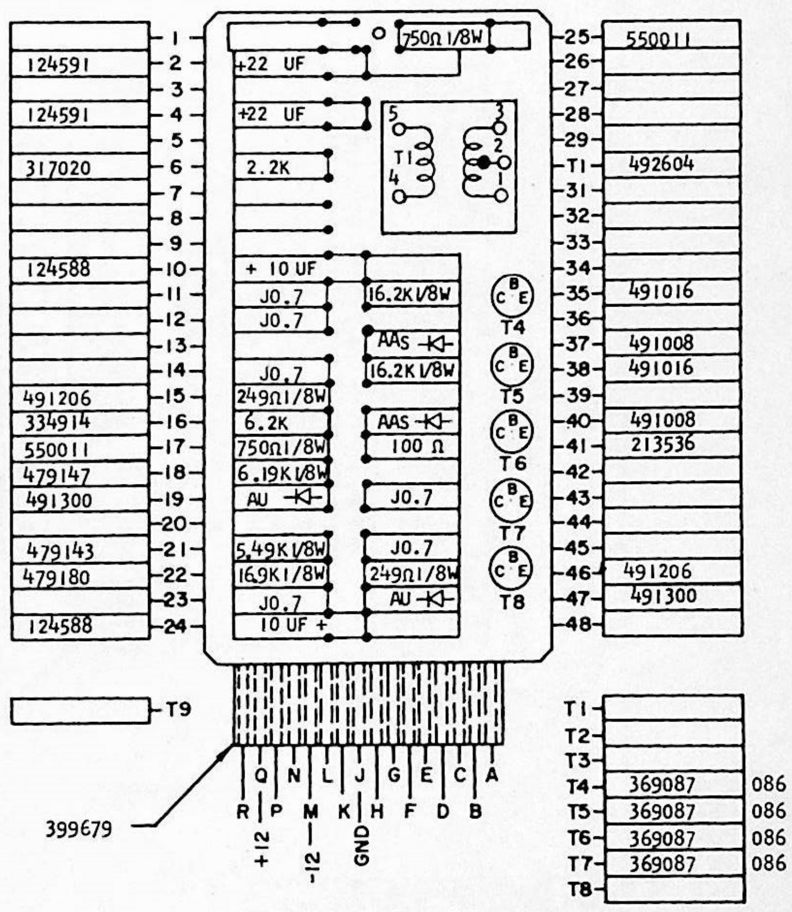




APPLICATION NOTES

VOLTAGES AT PIN G AND B FROM CLIPPING CARD

	INPUT WAVE FORM AT PIN E 10.1VP-P NOMINAL 11.2VP-P MAXIMUM REFERENCE LEVEL +1.59V TO -3.88V
	OUTPUT WAVE FORM AT PIN C OR F 1. LOW ACCEPTANCE CHANNEL OV TO .05V REF TO -12V. READ COND. 1.55V TO 1.91V REF TO -12V. READ WHILE WRITE CONDITION. 2. HIGH ACCEPTANCE CHANNEL 1.92V TO 2.18V REF TO -12V. READ CONDITION. 2.53V TO 2.90V REF TO -12V. READ WHILE WRITE CONDITION.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR - SENSE AMPLIFIER-RECTIFIER AND CLIPPER				/ 62	115599					
DESIGN		MODEL	SMS							
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

729957

C

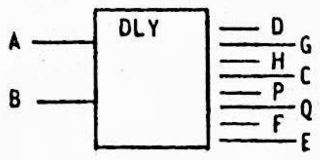
STANDARDS CODE	

740601

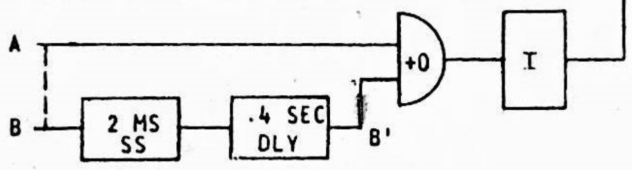
CARD CODE	740601
ZKV-	

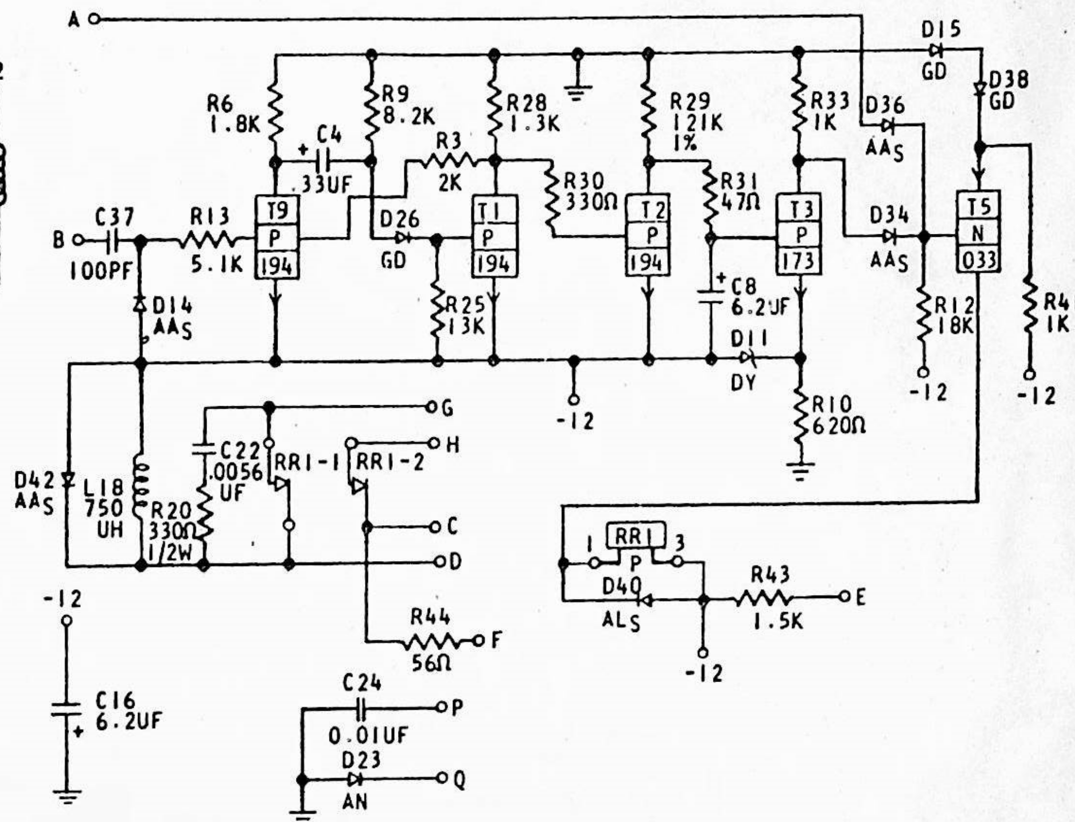
REFERENCE DRAWING

SEE PRODUCTION DRAWING 372687



FUNCTIONAL OPERATION





SEQUENCE OF OPERATION

1. NORMAL OPERATION PINS A AND B TIED TOGETHER (DRIVE ETMS FROM PIN G).
2. POSITIVE GOING INPUT ON PIN B CAUSES B' TO TIME OUT 400 MILLSEC. (SEE TIMING CHART).
3. THE N.C. REED RELAY IS DE-ENERGIZED (POINTS CLOSED) FOR A OR B' UP (METER RUN CONDITION).
4. FOR A ONLY. IN THE UP LEVEL THE NC REED RELAY IS DE-ENERGIZED (POINTS CLOSED). FOR A ONLY. IN THE DOWN N.C. REED RELAY IS ENERGIZED (POINTS OPEN).
5. THE LEVEL OF THE WAVE FORM APPEARING AT RR1-2 IS DEPENDENT ON TYPE OF LOGIC BEING DRIVEN.

   A. FOR DRIVING INTO CTRL, CTDL, SDTDL AND SDTRL CONNECT THE FOLLOWING:

FROM	TO
E	F
F	P
H	J

   DRIVE FROM PIN E

   B. FOR DRIVING CURRENT MODE, CONNECT THE FOLLOWING:

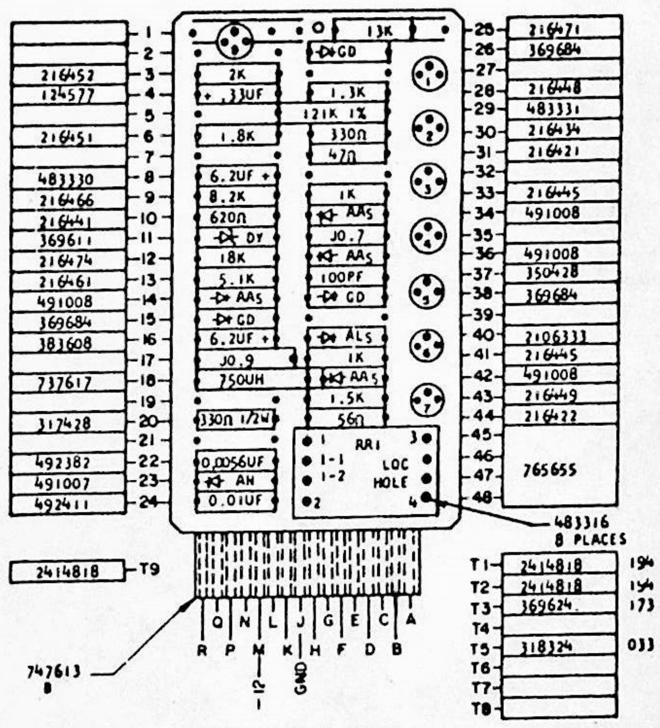
FROM	TO
C	-36 OR -48
H	UNIV INTEGRATOR WITH "P" OR "N" OUTPUT

   C. FOR DRIVING INTO DDTL LOGIC, CONNECT THE FOLLOWING:

FROM	TO
E	C
H	Q
Q	P

   DRIVE FROM PIN H

PIN	SIGNAL NAME	WAVE SHAPE	LEVELS		
				MIN	MAX
A ONLY	DIODE INPUT		UP	-.81	+6.27
			DOWN	-3.0	-15
G	RR1-1 OUTPUT		UP	--	--
			DOWN	-11.00	-12.48
A TO B	INPUT	T>.4 SEC T<.4 SEC	POS. GOING SHIFT	5.1	13.20
B'-G	RR1-1 OUTPUT	.4 SEC .4 SEC .4 SEC	DOWN	-11.00	-12.48



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE

INTERNATIONAL BUSINESS MACHINES CORP.			DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASSEMBLY TSTR - ETM DELAY CIRCUIT		9-20-63	11/898					
DESIGN	FVL	8-8-63 MODEL							
DETAIL	FVL	8-8-63 SCALE							
CHECK		DRAW							
APPRO	GWS	8-9-63 CHECK							

740601

C